CISCO SYSTEMS

Cisco VCO/4K Card Technical Descriptions

Software Release 5.1
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Customer Order Number: VCO4K-CARD-TD-DOC
Part Number: 78-10751-03

VCO/4K Card Overview

Alarm Arbiter Card (AAC)with Alarm Interface Card (AIC)

Central Processing Unit (CPU - 16 MB)

Combined Controller Assembly (CCA)

Network Bus Controller 3 Card (NBC3)

Direct Inward Dial Card (DID-2)

Drop and Insert Card (D+I)

E+M Trunk Card (E+M)

Four Span Programmable T1 Interface Card (4xT1)

Interface Controller Card (ICC)

Interface Controller Card T1 I/O Module

Line Test Card-8 (LTC-8)

MVDC Programmable T1 Interface Card (MVDC)

Primary Rate Interface/NFAS Card (PRI/N)

Subscriber Line Interface Card (SLIC-2)

T1 Interface Card (T1)

Universal Trunk Card (UTC-2)

Call Progress Analyzer Card (CPA)

Digital Conference Card (DCC)

Digital Tone Generator Card (DTG)

Digital Tone Generator 2 Card (DTG-2)

DTMF Receiver Card (DRC-8)

INTEGRATED PROMPT/RECORD CARD (IPRC)

MF Receiver Card (MRC)

DTMF Receiver Cards (DRC-24 and DRC-48)

Subrate Switching Card (SSC)

Service Platform Card (SPC)

Direct Dial Inward Card (DDI)

E1-Channel Associated Signalling Card (E1-CAS)

Earth/Loop Connect Trunk Card (ECT/LCT)

International E+M Trunk Card (E+M/DC5)

E1-Primary Rate Interface Card (E1-PRI)

Four Span Programmable E1 Interface Card (4xE1)

Interface Controller Card E1 I/O Module

Interface Controller Card J1 I/O Module

Multifrequency R2 Transceiver Card (MFC-R2)

Subscriber Line Interface Card for International (SLIC-INT)

T1-E Interface Card (T1-E)

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T1-E Interface Card (T1-E)

Section 1
VCO/4K Card Overview

1.0 INTRODUCTION

The *VCO/4K Card Technical Descriptions* consist of a set of technical descriptions which describe the following types of cards used in a VCO/4K system:

- Control circuit cards are used in system controllers. System controllers provide database management, program load and start-up, basic call processing functions, maintenance and administration access, host control and peripheral device interfaces.
- Port interface cards provide incoming and outgoing interfaces between the system and the switched network.
- Service circuit cards provide special facilities that can be accessed by network interface ports.

Each technical description in this series reflects the most current information available about the product. The information contained in a technical description is specific to a single component within a VCO/4K system. Other system documents point to technical descriptions as containing the most detailed information available for a component.

A technical description contains information to service and maintain the component. For system-level servicing, refer to the *VCO/4K System Maintenance Manual*. The maintenance manual assists in isolating the cause of a system malfunction and serves as a pathfinder to the more detailed information contained in technical descriptions.

2.0 CARD REMOVAL/REPLACEMENT PROCEDURES

All port interface, service circuit and international cards can be safely removed and replaced with the system powered-up and operating normally.

> *NOTE: See appropriate technical descriptions for instructions on removing and replacing control circuit and DTG-2 cards.*

The card should be in an out-of-service (OOS) status, however, to assure that in-progress calls are not affected when the card is removed from the port subrack.

> **CAUTION: Read all instructions before attempting to remove or replace a card.**
>
> **To minimize the risk of injury from hazardous voltages, avoid contact with the backplane when removing or replacing system cards.**
>
> **Observe antistatic precautions when handling a card to avoid damaging sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing cards or I/O modules.**

2.1 CARD REMOVAL PROCEDURE

Perform the following steps to remove a system card from a card slot:

1. Go to the Maintenance menu and then select Card Maintenance to change the status of the card to OOS. Wait for the green LED on the card's front panel to illuminate before removing the card from the card slot.
2. Use a #1 Phillips-head screwdriver to remove the mounting screws/washers from the top and bottom PCB card retainer bars (see Figure 1.1) on the system. Keep the retainers and screws together in a safe place for replacement later.

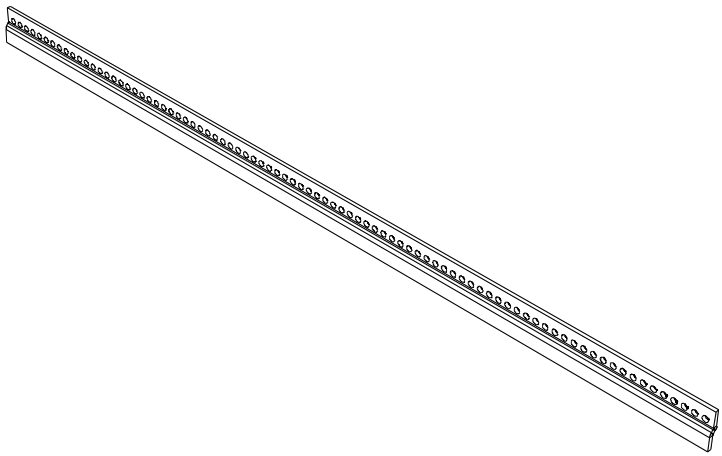


Figure 1.1: PCB Card Retainer Bar

3. Use your thumbs to push the upper and lower ejectors away from the desired card front panel. This action will pop the card from the backplane connectors.

   NOTE: Cards should be removed and replaced using only enough force to disengage or engage the card from or into backplane connectors. Yanking cards from, or jamming cards into, the backplane can seriously damage connectors and result in operating problems which will be very difficult to isolate.

4. With both hands, grasp the card on its top and bottom edges as you remove it from the card slot. Pull the card from the card slot.
5. When you have removed the card from the card slot, place it on an antistatic mat or envelope.

   CAUTION: If your system arrived with blank card assemblies (blank faceplate and blank metal blade) installed, these assemblies must remain in their original locations, unless you replace them with a functional system card. These blank card assemblies are carefully configured to compartmentalize the system for safety reasons and are critical to maintain NEBS GR-63-CORE compliance.

2.2 CARD REPLACEMENT PROCEDURE

Perform the following steps to replace a system card in a card slot:

1. Place the replacement card next to the removed card on the antistatic mat or envelope.
2. Verify that all the switch and jumper settings on the replacement card correspond with those on the removed card.

   NOTE: Refer to your release notes and verify that the revision levels of the PROMs match the requirements of the generic software currently loaded in your VCO/4K system.
3. With both hands, grasp the replacement card on its top and bottom edges and align it with the top and bottom card guides of the card slot.
4. Push the card inward until it makes initial contact with the backplane.

   Make sure the ejector levers are perpendicular to the front panel. Continue pushing the card inward until it makes firm contact with the backplane. The hooks on the ejectors must be behind the front rail of the card slot. Use your thumbs to push the ejectors inward toward the front panel. The card should be fully seated into the backplane connectors when the levers are flush against the front panel.
5. Most cards are automatically brought into service when you replace them in the port subrack; an appropriate system message is displayed on the master console and logged in the system error log. Cards can take up to five minutes, however, to initialize and become active. If a card fails to come into service within an appropriate amount of time, use the Card Maintenance submenu and the Change Status command to place the card in Active status.
6. Reinstall the top and bottom PCB card retainer bars (see Figure 1.1). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers.

   CAUTION: The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

   NOTE: If you are experiencing difficulties with ICC or SPC installation, the following helpful tip may improve installation:

   When sliding the ICC or SPC into position along the card guide, gently touch the card to the midplane connector. Push lightly on the right side of the card's faceplate and apply slight pressure until you feel the connectors engage. This will ensure a proper fit and midplane interconnection.

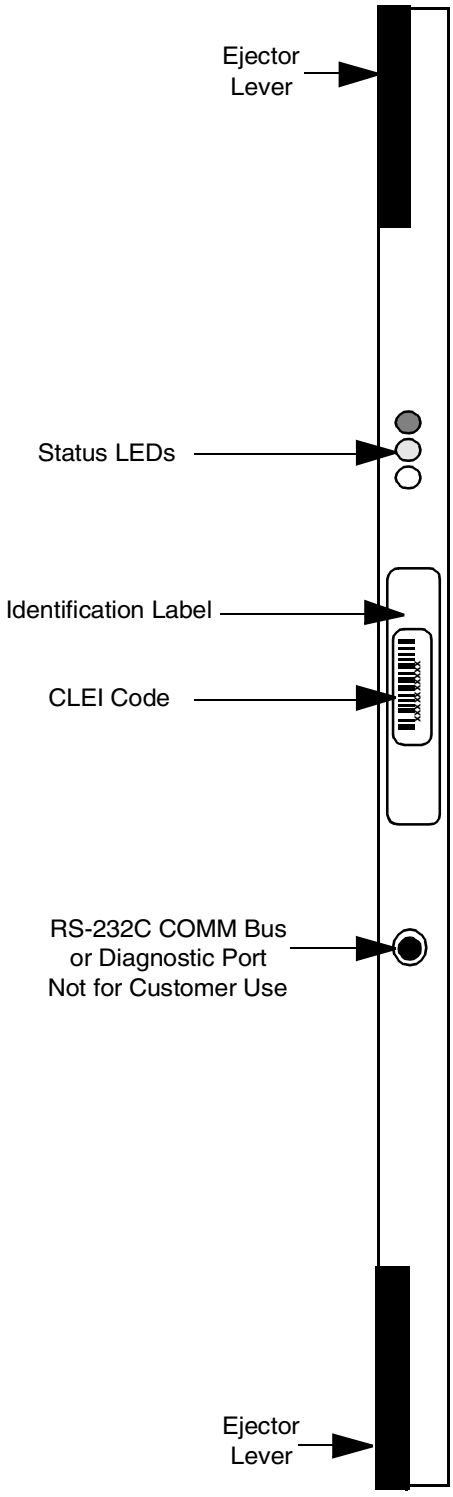


Figure 1.2: Analog Card Front Panel

2.3 ICC I/O MODULE REMOVAL PROCEDURE

Perform the following steps to remove an I/O Module card from a card slot:

1. Take all spans OOS from the Card Maintenance submenu.
2. Disconnect the corresponding ICC card from the front of the switch.
3. From the back of the system, unscrew the top and bottom fasteners for the I/O Module.

   NOTE: Cards should be removed and replaced using only enough force to disengage or engage the card from or into backplane connectors. Yanking cards from, or jamming cards into, the backplane can seriously damage connectors and result in operating problems which will be very difficult to isolate.
4. Remove the I/O Module and place it on an antistatic mat or envelope.

   NOTE: Network connections may be disconnected before or after card removal.

2.4 ICC I/O MODULE REPLACEMENT PROCEDURE

NOTE: The I/O Module must be inserted in the system before the ICC card.

Perform the following steps to replace an I/O Module in a card slot:

1. Set the replacement card on the antistatic mat or envelope.
2. If there is one in the system, remove the associated ICC card.
3. With both hands, grasp the replacement I/O Module card on its top and bottom edges and (at the back of the system) align it with the top and bottom card guides of the subrack.
4. Push the card inward until it touches the back side of the port subrack backplane. Apply additional pressure to the card to ensure that it is seated. Tighten the mounting screws.
5. Replace the ICC card at the front of the system.

   NOTE: The network connections on the I/O Module can be made prior to or following the ICC card insertion.

3.0 CARD SPECIFICATIONS

Part Number	Contact your Cisco Systems sales representative	
Operating Temperature	10°C to 40°C (50°F to 104°F)	
Relative Humidity	20% to 80% (non-condensing); temperature rise or fall should not exceed 10°C (18°F) per hour	
Physical Dimensions: Port Interface, Service Circuit, and International Cards (except DTG-2)	**Standard Card** Height – 15.6 in. (396mm) Depth – 12.1 in. (305mm) Width – 0.79 in. (20mm) (9U Eurocard form factor)	**ICC I/O Module** Height – 14.5 in. (368mm) Depth – 5.8125 in. (148mm) Width – 0.79 in. (20mm)

4.0 TROUBLESHOOTING

This section describes how to detect and correct common problems associated with port interface and service circuit cards.

4.1 SYSTEM LOG—ERROR AND STATUS MESSAGES

System and card error messages appear on the System Alarm Display and Card Alarm Display screens, respectively, when a major or minor alarm condition occurs. The message provides the rack-level-slot address of the suspect card.

In addition to illuminating appropriate status LEDs, all system and card alarm conditions are appropriately identified in the log, such as `CARD ALRM SET, CARD ALRM CLRD, MIN ALARM SET, MIN ALRM CLRD`.

Messages are written to the system error log and output to the system printer. Messages are time stamped by day of week (according to the setting of the system clock/calendar), and identified according to which system controller generated the message. Refer to the *VCO/4K System Administrator's Guide* for a list of error messages and their meanings.

> *NOTE: Refer to the* VCO/4K System Maintenance Manual *for information on how to use system logs to isolate issues within a system.*

4.2 DETECTING AND CORRECTING ANALOG CARD PROBLEMS

Analog interface card status LEDs observe the following patterns (except T1, E1, E1-PRI, and PRI/N cards):

- All LEDs OFF – the card is operational.
- Red LED illuminated (Major Alarm indication through AAC) – the card has failed its self-test and is out-of-service (suspect that the card is bad).
- Yellow LED illuminated (Minor Alarm indication through AAC) – the card is operational but may be experiencing interface or software problems (communication bus failure; data overrun between the NBC-3 and the system controller).
- Green LED illuminated – the card is not active and can be removed from the system.

  NOTE: The green LED illuminates whenever a card is inserted in the backplane. This occurs even when the card has been inserted in the wrong slot or card data has not been entered in the system database. Always double check slot location and database entries when replacing an analog interface card.

  NOTE: When an analog card is reset, either by the NBC-3 following a system controller reboot or because the card has been marked Active via the Master Console, all three front panel LEDs simultaneously turn on and then off. If the LEDs remain illuminated, a hardware fault has been detected. Check the card PROM chip for revision level and proper seating in its socket.

Failure of internal communications bus testing (card self test) causes a major alarm indication (red LED illuminated).

A minor alarm indication (yellow LED illuminated) occurs when the NBC-3 has stopped polling the card. If the NBC-3 has detected errors in the card, the card is placed in an out-of-service state and the green LED is illuminated.

If a two or more lines/trunks interfaced with a particular card are unavailable for call processing but status LEDs are all off, suspect a database error, a faulty I/O module cable, an undocumented wiring plan change, or loss of CO services. Verify the I/O module connections and CO services. If the fault is not with the connections, remove and replace the card. Verify the database entries for the card, including card configuration, inpulse and outpulse rules.

The green LED is illuminated for a card which has been mounted in the wrong slot or has not been configured in the database; however, the system log contains error messages indicating a bad card.

If the green or red LED illuminates on a card during normal system operation, use the Card Maintenance Menu to reset the card using a Change Status command (refer to the *VCO/4K System Administrator's Guide*). If the Change Status command fails, remove the card from the backplane and reseat it. If the red LED illuminates, remove and replace the card.

NOTE: DRCs, MRCs, and MFC-R2s must be placed in system Resource Groups.

4.3 SERVICE CIRCUIT TEST UTILITY

The Generic administrative software includes a Service Circuit Test Utility you can use to test individual circuits on service circuit cards. Any or all receiver ports on the same card can be tested with a single command. Ports are tested in sequential order from the start port specified to the end port specified. You can also set this test to loop repeatedly, testing ports sequentially over and over.

When testing a service circuit card, dial tone, ringback, ringback cessation, busy, and reorder tone events are presented by the Digital Tone Generator (DTG) card to the card port(s) for detection. Any discrepancy between the presented tone and the reported detection results in the port(s) failing the test. Logfile and system printer error messages specify the port's address and the type of tone it failed to detect.

You can use a port on a line/trunk or receiver port to monitor the test. This port monitors the link between the service circuit being tested and the resource providing test digits or tones. Monitoring the digits and tones being passed allows you to determine the exact point of test failure.

You must place the card on which the receiver ports reside in Diagnostic mode before it can be tested. If any ports are active when the card is placed in Diagnostic mode, the card automatically switches to Camped On mode. The Service Circuit Test function can be run on a service circuit card in Camped On mode; the test skips any non-idle ports on the card.

Refer to the *VCO/4K System Administrator's Guide* for further information on accessing and using the Service Circuit Test Utility.

4.4 TEST MF RECEIVERS

From the Diagnostics Menu, you can select the DTMF /MF Receiver Tests screen to perform port tests on specified DRCs, MRCs, and *MFC-R2s*.

> *NOTE: Use the Card Maintenance Menu under the Maintenance Menu to place the desired receiver card(s) in Diagnostic (D) mode. This Test Receiver function will not work unless the card has been placed in Diagnostic mode.*

Observe the cautionary note on the screen about specifying start and end ports for the tests. When you have entered the start and end ports, press **Enter** to begin the tests.

A message indicating which port is being tested appears on the bottom of the screen. As testing of each port is completed, a status message indicating the result of the test is displayed on the screen and sent to the system printer.

4.5 DETECTING AND CORRECTING T1,T1-E, E1, E1-PRI, AND PRI/N CARD PROBLEMS

Factors which cause major alarm indications include:

- Loss of carrier
- Failure of internal communications bus test (card self-test)
- Card out-of-service (manually via master console or due to a communication bus error)
- T309 expiring (default = 90 seconds) – D-channel failure (E1-PRI or PRI/N)

Factors which cause minor alarm indications include:

- Remote alarm
- Slip maintenance threshold reached
- Out-Of-Frame (OOF) condition
- Out-Of-Frame (OOF) maintenance threshold reached
- Loss-of-frame (LOF) condition
- LOF maintenance threshold reached

Loss of carrier can be attributed to a fault in the span line or a failure of the digital side of the channel bank. Loss of synchronization can either be related to problems with the T1, T1-E, E1, E1-PRI, or PRI span line providing external sync with the system, an external sync pulse source connected to the NBC-3, or NBC-3/T1, T1-E, E1, E1-PRI, or PRI phase lock timing.

Verify channel bank operation and the span line connection before removing and replacing any cards.Loss of a channel(s) may be the result of problems on the originating side of the channel bank/digital switch.

4.6 T1,T1-E, E1, E1-PRI, AND PRI/N CARD MAINTENANCE STATES

T1, T1-E, E1, E1-PRI, or PRI/N cards may be operating in any of four states – Active, Maintenance, Out-Of-Service, or Diagnostic. These maintenance states differ from those of analog interface cards as defined below.

Active State

This is the normal operational state for digital cards. No alarms are being sent outward on the T1, T1-E, E1, E1-PRI, or PRI stream and no front panel LEDs are illuminated. However, individual ports on the card may be manually placed in the Out-Of-Service state using system Maintenance Menus (refer to the *VCO/4K System Administrator's Guide* for more information).

Maintenance State

In this state, the system has stopped call processing because of an alarm received from the far end or from internal processing and may be presenting alarms to the far end of the T1, T1-E, E1, E1-PRI, or PRI stream. This state is automatically triggered by the system when an inward T1, T1-E, E1, E1-PRI, or PRI alarm is present.

A card placed into the Maintenance state by alarm processing will continue calls in progress. No new calls will be accepted. All idle channels will be put into the Maintenance Near End state. As channels become idle, they are put into the Maintenance Near End state.

The card is also automatically placed into Maintenance state while the E1-PRI or PRI/N application software is downloaded. Cards can be placed into Maintenance mode manually via the system administration console.

Out-Of-Service State (OOS)

In this state, call processing is stopped. E1-CAS cards send A/B bits indicating a Blocked condition on all channels. T1, T1-E, E1-PRI, and PRI/N cards send an unframed, all-ones (1s) signal (Yellow Alarm) to the far end, triggering an Out Of Frame (OOF) alarm. The yellow and green LEDs are illuminated on the front panel of the T1, T1-E, E1, E1-PRI, or PRI/N card.

Diagnostic State

In this manually enabled state, the system stops call processing of all ports on the T1, T1-E, E1, E1-PRI, or PRI/N card to allow the Test Port Card function to be run. The card is set to local loopback (Diagnostic state). The E1-CAS card sends Blocked signals on all channels. The T1, T1-E, E1-PRI, and PRI/N cards send an unframed, all-ones (1s) signal to the far end, triggering an OOF alarm. These LOF or OOF conditions cause the far end to remove the trunk from service. The cards can also be set to remote loopback (Remote Loopback state). Refer to the *VCO/4K System Administrator's Guide* for more information on using diagnostics and changing card states.

> *NOTE: When the NFAS option is used, additional processing states for the Primary/Backup D-channels are supported. These states can be changed using the NFAS Group Configuration screen. Refer to the* ISDN Supplement *for complete information on NFAS support.*

4.7 ERROR CONDITIONS DETECTED ON INCOMING STREAM

The T1, T1-E, E1, E1-PRI, and PRI/N cards can detect several types of error conditions on incoming streams. All cause a major or minor alarm on the Alarm Arbiter Card (AAC).

Yellow Alarm (Remote Alarm Condition [RAI])

A Yellow Alarm occurs when zeros appear in the Bit 2 position of all channels in the T1 or T1-E received bit stream, a Remote Alarm Indication (RAI) signal is found in the E1 received bit stream, or 8 ones [1s] are followed by 8 zeros in the E1-PRI or PRI received bit stream. This condition usually indicates a loss of carrier or OOF at the far end. The yellow LED on the card illuminates, a minor alarm is triggered, and the T1, T1-E, E1, E1-PRI, or PRI/N card transitions to the Maintenance state. The card automatically returns to Active when the remote carrier alarm clears.

Remote Multiframe Alarm Condition

A Remote Multiframe Alarm condition (also known as a Distant Multiframe Alarm [DMA]) occurs when the Loss of Multiframe Alignment signalling bit in timeslot 16 is set to 1 in the received bit stream. This condition indicates the distant end cannot detect a proper multiframe alignment pattern. The yellow LED on the E1 card illuminates, a minor alarm is triggered, and the card transitions to the maintenance state. The card automatically returns to Active when the DMA clears.

Signaling Bit Alarm

Onhook/offhook information is passed within the T1 stream via “robbed” bit signaling. Every sixth frame, the least significant bit (LSB) of all 24 PCM samples is replaced by a bit representing either the A- or B-signaling bit for that channel. The representation of signaling Bit A and signaling Bit B information alternates every sixth frame. A superframe consists of 12 frames of PCM data containing one Bit A signaling bit and one Bit B signaling bit.

The system monitors the T1 stream looking for repetitive A/B bit patterns. The F_t (terminal framing) and F_s (signaling framing) patterns are defined in *Bell PUB 43801 Digital Channel Bank Requirements And Objectives*. When the F_s pattern is not detected, the system triggers a signaling bit alarm. This is an unusual condition in that an OOF condition and signaling bit alarm will most likely occur together, and an OOF alarm takes precedence over a signaling bit alarm.

The red LED on the T1 card is illuminated, a minor system alarm is triggered, and the card goes into maintenance state. It returns to Active automatically when the condition clears.

Slip

A slip occurs whenever the system clock source frequency differs from the clock recovered from the inward stream. A slip report (either receive or transmit) increments an internal counter which is monitored by the Generic software. When a programmable threshold of slip reports (default=255) are received within a 24-hour period, the system sets a minor alarm. The system automatically places the card in the maintenance state if the `MANUAL INTERVENTION FOR SLIP/OOF` feature flag is set to **Y**. The card stays in the maintenance state until you take the card Out-of-Service and then place it back into Active service through the Card Maintenance menu. In either case, the Maintenance Threshold alarm stays on until you manually clear it.

Loss Of Carrier

A carrier loss is detected when there are an insufficient number of stream bit transitions from which a clock can be recovered. The error condition automatically places the card in the maintenance state and sends a Yellow Alarm (zeros in Bit 2 of all channels for T1 or T1-E, or 8 ones [1s] followed by 8 zeros for E1-PRI or PRI/N) to the far end of the stream and busies out all trunks. The red LED is illuminated on the front panel of the T1, T1-E, E1, E1-PRI, or PRI/N card and a major system alarm is triggered.

Out-Of -Frame (OOF)

An OOF condition is reported when the Frame bit (Bit 193) is lost for a period longer than 2.5 seconds. An OOF report increments an internal counter which is monitored by the system Generic software. The red LED on the card is illuminated (Red Alarm), a minor system alarm is triggered, the card goes to the maintenance state; a Yellow alarm is sent to the far end.

When a programmable threshold of OOF reports are received (T1=4) within a 24-hour period, the system sets an OOF Maintenance Threshold alarm. If the `MANUAL INTERVENTION FOR SLIP/OOF` feature flag is set to **Y**, the card stays in the maintenance state until you place the card back into Active service (using the Card Maintenance Menu). The red LED remains on until the OOF condition clears. If the `MANUAL INTERVENTION FOR SLIP/OOF` feature flag is set to **N**, the card remains in the maintenance state only until the OOF condition clears, then returns to Active automatically. In either case, the Maintenance Threshold alarm stays on until cleared manually.

Loss-Of-Frame (LOF)

A LOF condition is reported when an individual frame alignment pattern is not detected within 12 to 14 milliseconds. A LOF report increments an internal counter which is monitored by the Generic software. The red LED on the E1-CAS is illuminated, a minor system alarm is triggered, and the card goes to the maintenance state; a Remote Alarm Indication (RAI) is signalled to the far end.

When four LOF reports are received within a 24-hour period, the system sets a LOF Maintenance Threshold alarm. If the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to Y, the card stays in the maintenance state until you use the Card Maintenance Menu to place the card back into Active service. The red LED remains on until the LOF condition clears. If the MANUAL INTERVENTION FOR SLIP/OOF feature flag is set to N, the card remains in the maintenance state only until the LOF condition clears; then returns to Active automatically. In either case, the Maintenance Threshold alarm stays on until cleared manually.

5.0 CISCO CONNECTION ONLINE

Cisco Connection Online (CCO) is Cisco Systems' primary, real-time support channel. Maintenance customers and partners can self-register on CCO to obtain additional information and services.

Available 24 hours a day, 7 days a week, CCO provides a wealth of standard and value-added services to Cisco's customers and business partners. CCO services include product information, product documentation, software updates, release notes, technical tips, the Bug Navigator, configuration notes, brochures, descriptions of service offerings, and download access to public and authorized files.

CCO serves a variety of users through two interfaces that update and enhance simultaneously: a character-based version and a multimedia version that resides on the World Wide Web (WWW). The character-based CCO supports Zmodem, Kermit, Xmodem, FTP, and Internet e-mail, and it is excellent for quick access to information over lower bandwidths. The WWW version of CCO provides richly formatted documents with photographs, figures, graphics, and video, as well as hyperlinks to related information.

You can access CCO in the following ways:

- WWW: http://www.cisco.com
- WWW: http://www-europe.cisco.com
- WWW: http://www-china.cisco.com
- Telnet: cco.cisco.com
- Modem: From North America, 408 526-8070; from Europe, 33 1 6446 40 82. Use the following terminal settings: VT100 emulation; databits: 8; parity: none; stop bits: 1; and connection rates up to 28.8 kbps.

For a copy of CCO's Frequently Asked Questions (FAQ), contact cco-help@cisco.com. For additional information, contact cco-team@cisco.com.

> *NOTE: If you need personal technical assistance with a Cisco product that is under warranty or covered by a maintenance contract, contact Cisco's Technical Assistance Center (TAC) at 800 553-2447, 408 526-7209, or tac@cisco.com. To obtain general information about Cisco Systems, Cisco products, or upgrades, contact 800 553-6387, 408 526-7208, or cs-rep@cisco.com.*

See the front matter of this document for details about the standard Cisco product warranties.

Alarm Arbiter Card (AAC)with Alarm Interface Card (AIC)

1.0 GENERAL

The Alarm Arbiter Card (AAC) serves as the central control point for system resets and alarm indication. The AAC is mounted at the top of the VCO/4K as shown in Figure 1. Switches on the front panel enable system controller resets and select which system controller is to be master. Status LEDs indicate the currently enabled system controller and major/minor alarms.

The AAC is attached to the Alarm Interface Card (AIC). The AIC accepts fault signals from the VCO/4K Power Subsystem, Fan Unit, and Ring Generator, and generates a single fault signal to the AAC. The AIC also conditions the fault signals for the AAC. Figure 2 shows the location of the Alarm Arbiter Card and Alarm Interface Card.

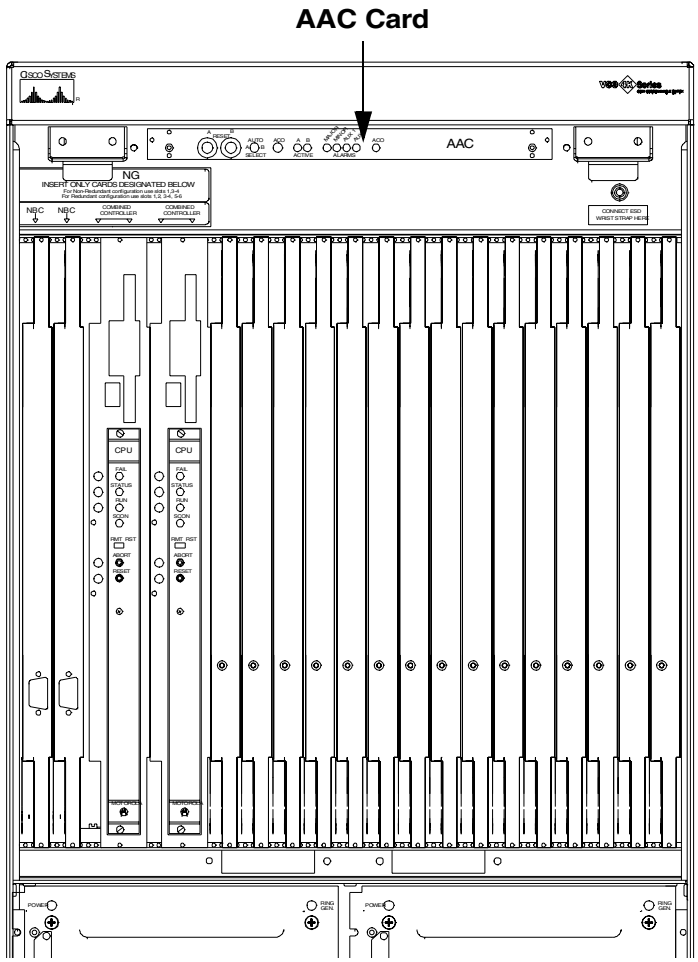


Figure 1: AAC Location

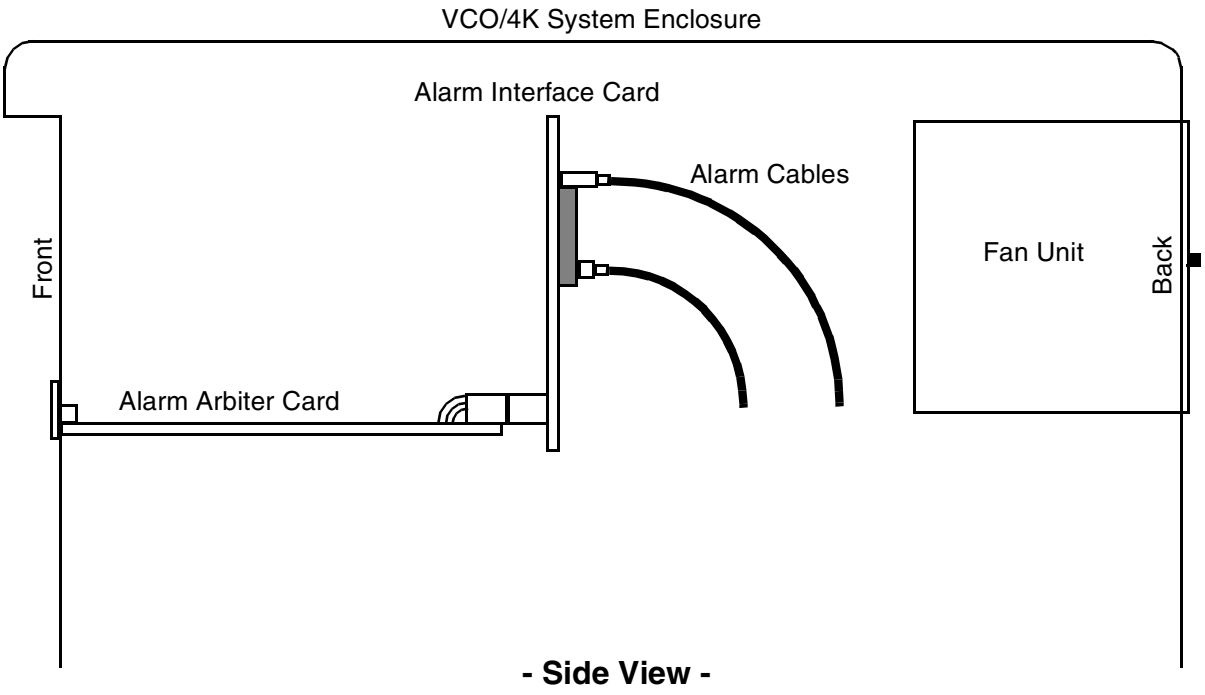


Figure 2: Location of the AAC and AIC

2.0 SPECIFICATIONS

Alarm Arbiter Card

Watchdog Timer Parameters:

After Reset/Power Up:	5 – 7 minutes
Normal operation:	5 – 10 seconds

Alarms:

Types	MAJOR, MINOR, AUX 1, AUX 2
	Visual indicators on AAC front panel
	External NO and NC relay contacts provided for each alarm
External Contacts	Type = 2 Form C Rating = 0.5A @ 24Vdc, 0.25A @ 120Vac (Resistive load only)
Power Requirements:	+12Vdc @ 1 A
Physical Dimensions	Height: 6.3 in (160mm)
	Width: 9.2 in (234mm)
	Depth: 0.631 in (16mm)

Alarm Interface Card

Power Requirements:	+5Vdc @ 0.2A (redundant)	
Physical Dimensions	Height -	70mm (2.75 in)
	Width -	374mm (14.75 in)
	Depth -	16mm (.0631 in)

3.0 AAC CIRCUIT DESCRIPTION

The AAC is the hardware interface point for manual and automatic bus resets and alarms. It also functions as a control point for the selection of system controllers in systems equipped with redundant control. Power reset and watchdog timer circuitry is duplicated for A-side and B-side system controllers in VCO/4K systems to minimize possible system effects of AAC failures. Figure 3 is a simplified block diagram of the AAC.

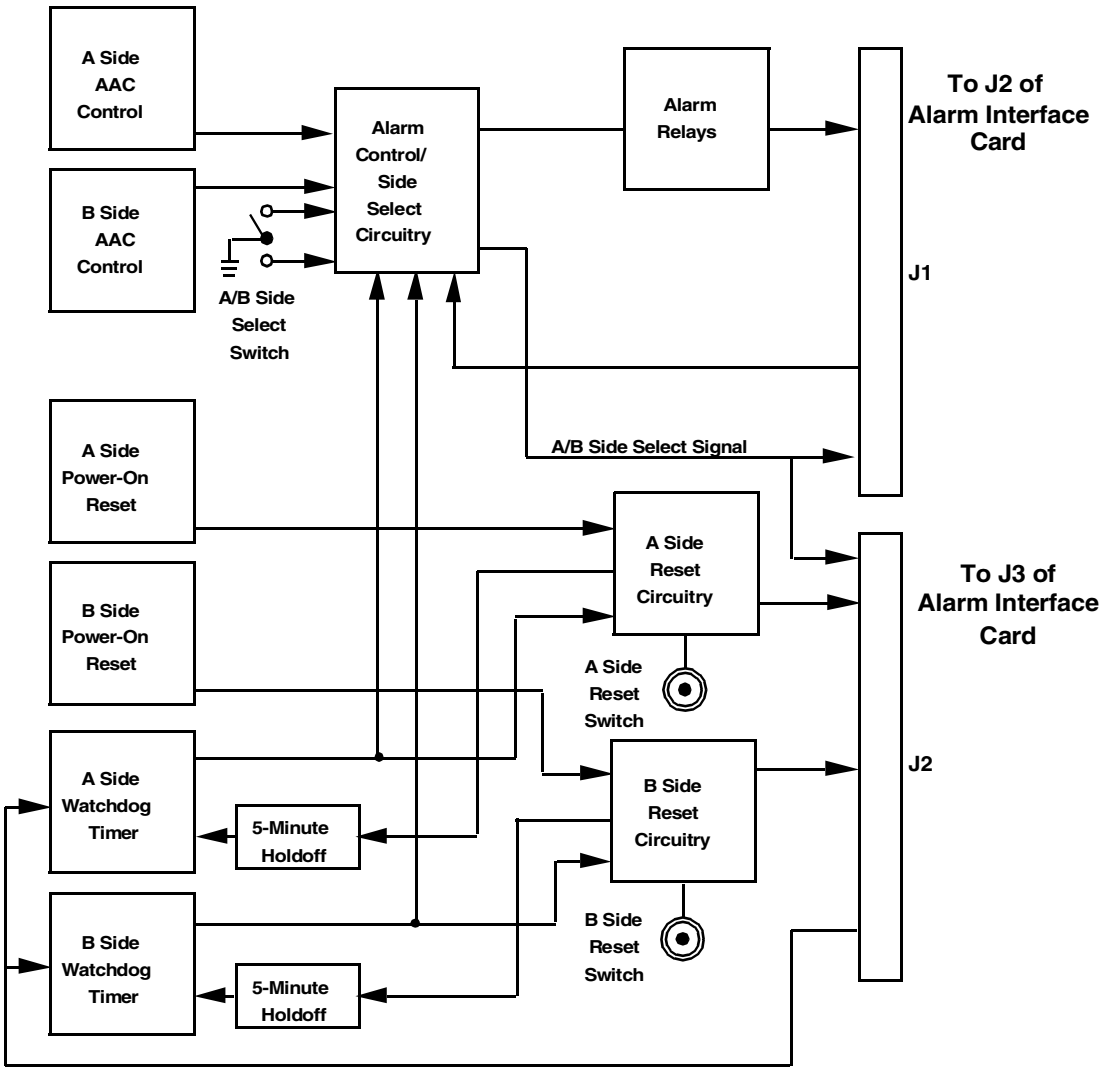


Figure 3: Block Diagram of Alarm Arbiter Card

3.1 WATCHDOG TIMER CIRCUIT

The AAC includes independent watchdog timer circuits for both A-side and B-side system controllers. These timers reset a controller's side within five seconds if the controller does not provide a tick every five seconds.

The watchdog timer for a particular system controller is disabled for approximately five minutes after that side is reset with the AAC. The watchdog timer is also disabled for a particular controller side if the other system controller is selected with the SELECT switch on the AAC front panel.

3.2 SWITCHING FROM ACTIVE TO STANDBY

The AAC monitors the status of both system controllers and switches active controllers if one of the following conditions occurs:

- Combined Controller Assembly on the Active controller is not available
- Active side watchdog timer expires
- Active side sets an internal AAC signal to indicate that it is off-line
- Active controller software requests a switch from Active to Standby

For the switchover to occur, the following conditions must be true:

- Front Panel SELECT switch is in the AUTO position
- NBC-3 on the Standby controller is present
- Watchdog timer on the Standby controller has not expired
- Standby controller has set the internal AAC signal to on-line (file synchronization has successfully completed)

It may take up to one second for the actual switchover to occur. Use the front panel SELECT switch to immediately force a switchover, regardless of the state of the Standby controller. However, make sure you use this type of switchover only in an emergency; data base sanity checks are *not* performed.

> *NOTE: Cisco Systems, Inc. strongly recommends using the Maintenance Menu to force a switchover. Refer to the* System Administrator's Guide *for more information.*

3.3 FRONT PANEL SWITCHES

On the left side of the front panel are two push-button switches labeled A RESET and B RESET (refer to Figure 4.) Press A RESET to reinitialize the A-side (left) controller; press B RESET to reinitialize the B-side (right) controller.

The SELECT switch is a three-position toggle switch that determines which controller in a redundant control system is currently active. The AUTO setting works for non-redundant and redundant control systems. In non-redundant control systems, the A-side is always active. SELECT A makes the system controller on the left (front view) active; SELECT B makes the right system controller active.

Manually selecting one side disables the watchdog timer of the other side. However, if the manually selected controller should fail, automatic switchover will not be performed. With redundant control systems, always return the SELECT switch to the AUTO position after manually selecting A-side. When a redundant system powers up, the AAC uses Side A as the active controller (if operational) when the switch is set to AUTO.

> *NOTE: In a redundant system in which the A-side is powered off and the system is to be brought up with the B-side active, the AAC switch must be set to* SELECT B. *If the AAC switch is in* AUTO, *the system will come up in Standby.*

The Alarm Cut-Off (ACO) switch is disabled. Changing the ACO switch has no effect on the audible alarm.

3.4 STATUS LEDS

Two green LEDs labeled ACTIVE indicate whether the A-side or B-side system controller is currently the master. Only one of these LEDs is illuminated during normal system operation. The active system controller is also indicated on the bottom message line of the master console display screen.

A red LED illuminates when a MAJOR alarm is signalled by hardware or software. Yellow LEDs indicate MINOR and AUX 1 or AUX 2 alarms. MAJOR and AUX 1 LEDs illuminate when a Power Subsystem or Fan Unit failure occurs. A separate yellow LED illuminates when ACO is enabled.

> *NOTE: Alarm LEDs on the AAC are disabled when the Audible Cutoff option on the System Alarms Display administration screen is chosen from the Maintenance menu. Refer to the* System Administrator's Guide *for more information on this option.*

Refer to the *VCO/4K System Maintenance Manual* for more information on alarm LEDs.

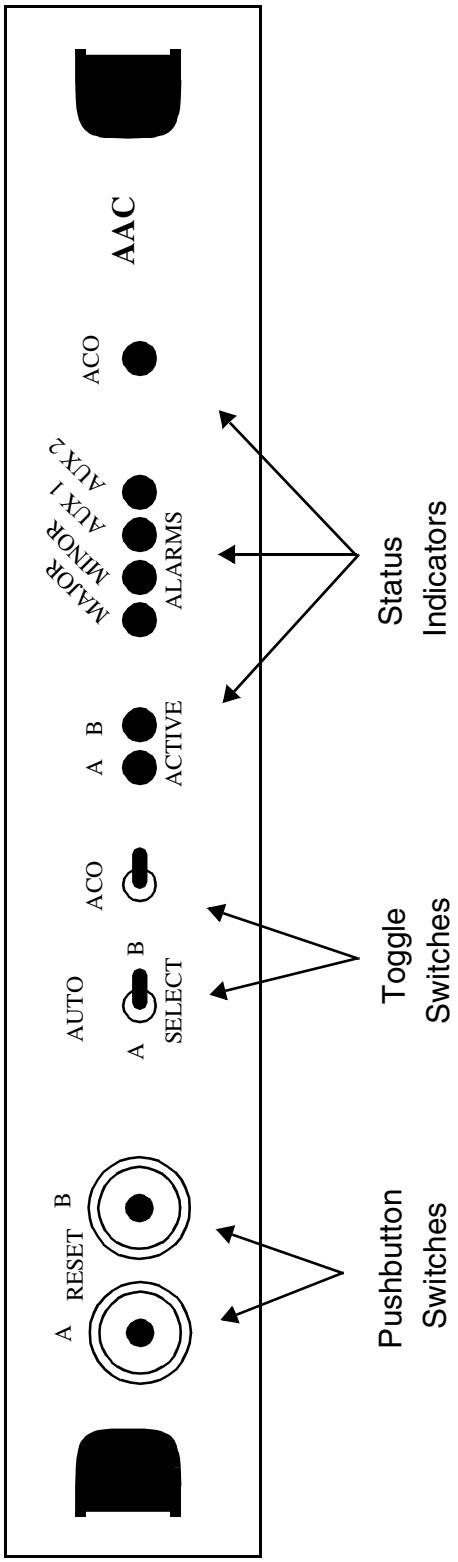


Figure 4: AAC Front Panel

3.5 AAC ALARMS

The AAC autonomously sets MAJOR, MINOR, and AUX 1 alarms based on the following criteria:

3.5.1 MAJOR ALARM

- Active Side time-out occurs
- Active Side is off-line
- NBC-3 is not installed on Active side
- A power alarm failure occurs

3.5.2 MINOR ALARM

- Standby Side time-out occurs
- Standby Side is off-line

3.5.3 AUX 1

- A power alarm failure occurs

  NOTES: The system may also support components which feature programmable alarm severity.

  For a complete listing of system alarms supported by Generic software, refer to the System Administrator's Guide.

  In VCO/4K applications, the host computer can set any of the alarms by software command.

3.6 CONNECTORS

The J1 connector carries the signals related to one of four peripherals functions to the External Alarms terminal strip, automatic A/B transfer switches, or the Power Subsystem. Table 1 lists the pin assignments for the J1 connector.

The J1 connector is attached to connectors JP1, JP3, JP4, and JP5 of the Alarm Interface Card, which provides routing for the signals to and from the AAC.

The J2 connector plugs into the AIC J3 connector. The AAC receives alarm commands from the active system controller, and the watchdog timer "kicks" from both system controllers via the J2 connector. The signals at J2 are proprietary and, therefore, no listing of pin assignments is provided.

The AAC derives power from J2. At least one Combined Controller Assembly must be installed and powered up for the AAC to power up.

Table 1: AAC J1 Pinouts

Pin	Signal	Pin	Signal
SLOT 1 – External Alarms			
1	Unused	33	Unused
2	Major Alarm COM	34	Major Alarm CLSD
3	Major Alarm COM	35	Major Alarm OPEN
4	Minor Alarm COM	36	Minor Alarm CLSD
5	Minor Alarm COM	37	Minor Alarm OPEN
6	AUX 1 Alarm CLSD	38	AUX 1 Alarm COM
7	AUX 1Alarm OPEN	39	AUX 2 Alarm COM
8	AUX 2 Alarm CLSD	40	AUX 2 Alarm OPEN
SLOT 2 – A/B Transfer Switch			
9	Unused	41	Unused
10	Side Select	42	Reserved
11	Reserved	43	DGND
12	Reserved	44	DGND
13	Reserved	45	DGND
14	Reserved	46	DGND
15	Reserved	47	DGND
16	Reserved	48	DGND
SLOT 3 – Power Subsystem			
PROPRIETARY			
SLOT 4 – Backplane			
PROPRIETARY			

4.0 AIC CIRCUIT DESCRIPTION

The J1 and J2 connectors of the AAC are mated to the J2 and J3 connectors of the AIC. The AIC cables are locked on to the connectors. The J2 connector is a 64-pin DIN connector.

The J2 connector breaks out the AAC signals into four connectors: JP1, JP3, JP4, and JP5. Table 2 lists the AAC signals for these connectors.

Table 2: AAC J2 Signals

Connector	Alarm
JP1	Backplane Alarms
JP3	Remote Alarm Output
JP4	A-B Switch for Peripherals
JP5	Selects Active NBC-3

The J1 connector is for the Fan Alarm Input. It connects to the Fan Unit through the Fan Unit J4 connector.

Table 3 lists the electrical characteristics of the fault-indicator input to the AIC. The AIC combines and conditions the signals for input to the AAC.

Table 3: VCO/4K Fault Indicator Characteristics

Signal	Voltage	Reference Voltage
DC FAIL - Input Power	+0.5 to +5.0V	DC ground
DC FAIL - Power	+0.5 to +5.0V	DC ground
DC OK - Fan	+2.5 to +5.0V	DC ground
DC OK - Ring Generator	100 VAC	-48 VDC
DC OK - Out	+0.5 to +3.0V (200 ohm)	DC ground

Figure 5 is a simplified block diagram of the AAC.

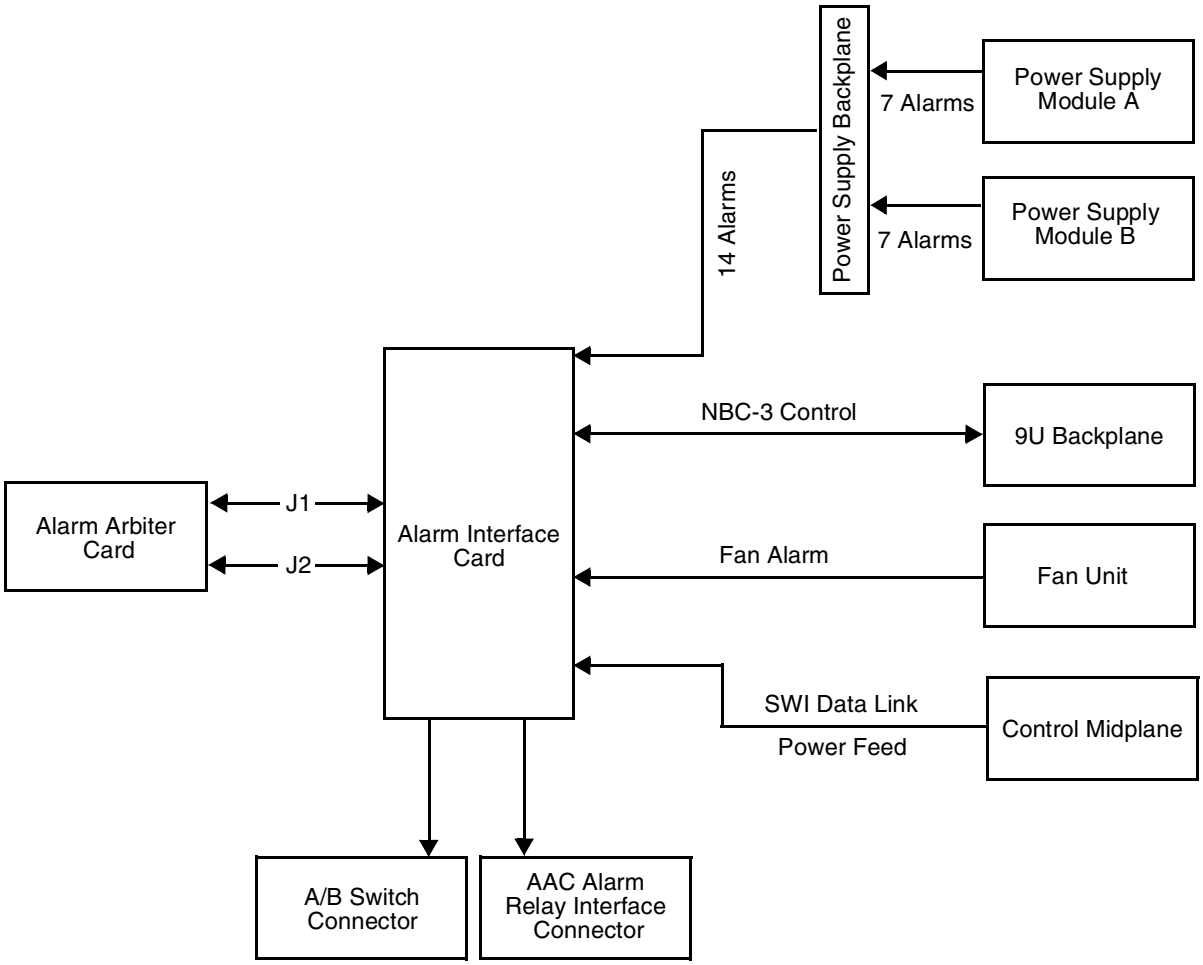


Figure 5: Block Diagram of Alarm Interface Card

The output signals from the AAC are used to control remote functions. These signals are not modified by the AIC and are transferred directly from the AAC J1 connector to the AIC JP3 connector.

The DC OK signal on J1-10C is the merged signal of all incoming faults (PWR, FAN, and RING).

5.0 CONFIGURATION NOTES

5.1 ALARM ARBITER CARD

The AAC is manufactured by Cisco Systems, Inc. Jumper plugs on the AAC are factory set to the defaults listed below. Figure 6 shows the location and correct installation of jumper plugs on the AAC.

5.1.1 JUMPER LOCATIONS

NOTE 1

Jumper location J3 allows the customer to selectively enable the on-board audible alarm device to sound for all alarm conditions or for major alarms only. The Alarm Cut-Off (ACO) switch is disabled. Changing the ACO switch has no effect on the audible alarm.

NOTE 2

Position the jumper plug at J4 near R31 for all applications.

5.2 ALARM INTERFACE CARD

The AIC is manufactured by Cisco Systems, Inc. Figure 7 shows the location and labeling of the cable connections on the AIC.

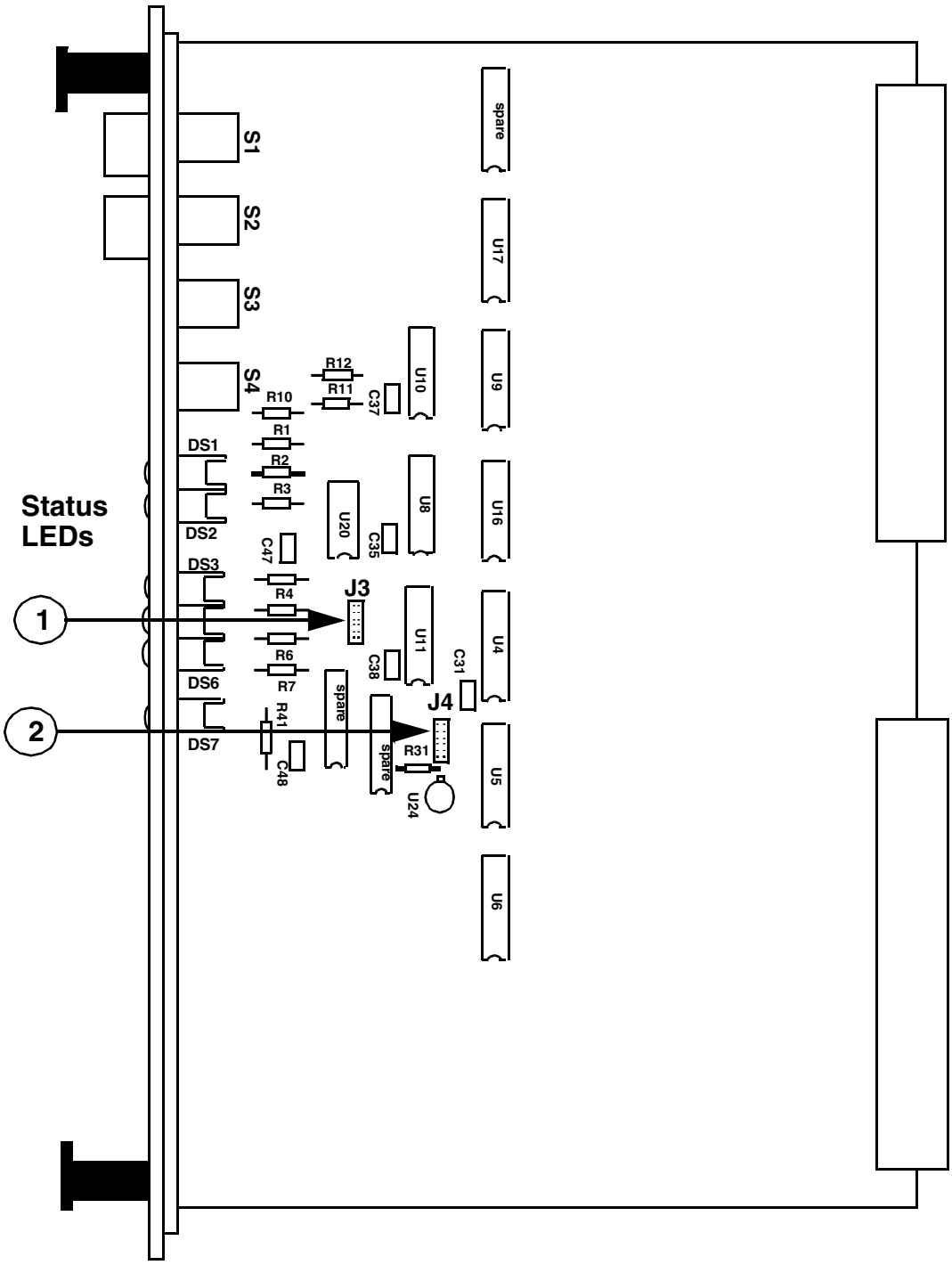


Figure 6: AAC Jumper Locations

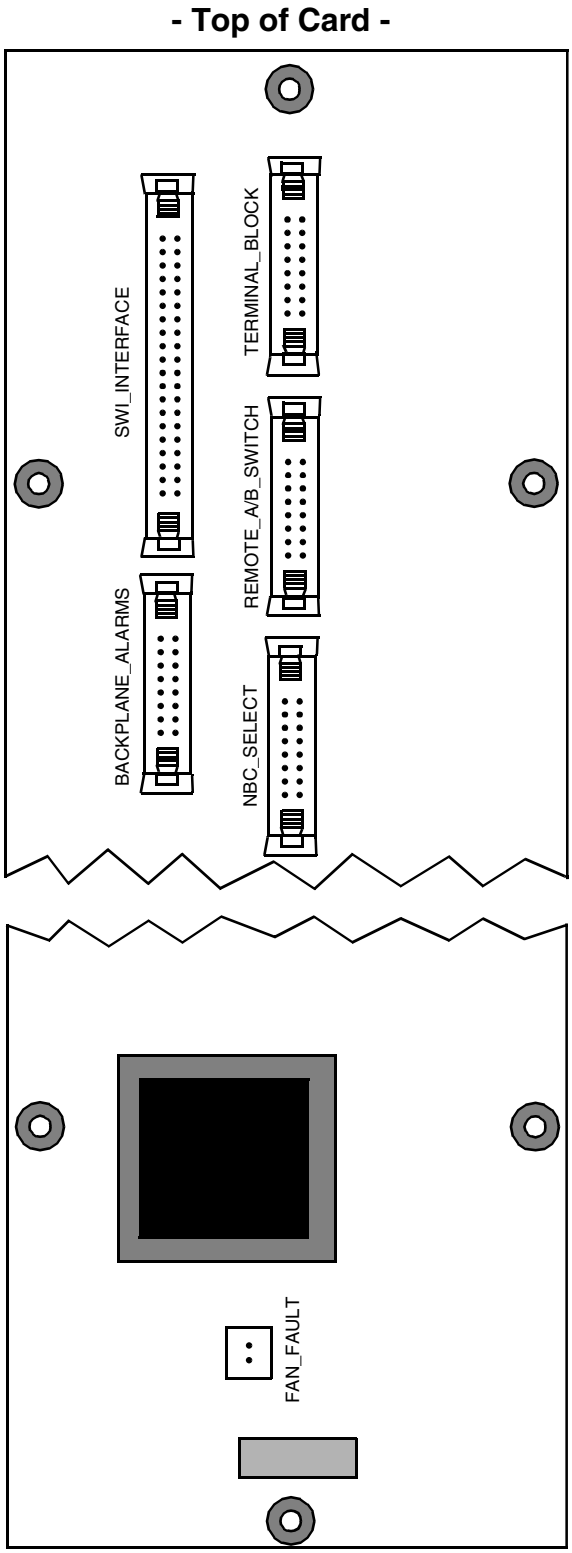


Figure 7: AIC Cable Connectors

6.0 REMOVAL/REPLACEMENT INFORMATION

CAUTION: Removing and replacing the AAC or AIC causes the system controller(s) to reset. Calls in progress will be lost and the system will be out of service for several minutes. To reduce disruptions to service, Cisco Systems, Inc. recommends replacing these cards when the least amount of traffic is anticipated through the switch.

Power down the system and observe antistatic precautions whenever handling the AAC and AIC to avoid damage to sensitive CMOS devices. Wear a ground strap connected to the VCO/4K equipment frame whenever removing or replacing these control circuit cards.

6.1 ALARM ARBITER CARD

6.1.1 REMOVAL PROCEDURES

To remove an AAC:

1. Wear a ground strap connected to the VCO/4K equipment frame.
2. Disable the external alarm system.
3. Use a 1/8-inch bladed screwdriver to loosen the captive mounting screws at the top and bottom of the AAC. Do not remove the screws from the card.
4. Set the POWER switch on the Power Entry Module to OFF. The entire system is powered off.
5. Firmly grasp the handles at the sides of the card and pull the card away from the backplane (AIC). The card fits tightly into the AIC connectors and some force is required to pull it.

   NOTE: Use only enough force to disengage the AAC. Yanking an AAC card from the AIC can seriously damage connectors and result in operating problems which will be very difficult to isolate.
6. When you have removed the card from the card slot, place it on an antistatic mat or envelope.

6.1.2 REPLACEMENT PROCEDURES

To replace an AAC:

1. Wear a ground strap connected to the VCO/4K equipment frame.
2. Grasp the replacement AAC by the handles and align it with the card guides.
3. Push the AAC inward until it makes contact with the AIC.
4. Firmly grasp the handles of the AAC and push the card toward the AIC. The card fits tightly into the AIC connectors and some force is required to seat the card back firmly into the AIC connectors.

   NOTE: Use only enough force to engage the card into the connectors. Jamming an AAC card into the AIC can seriously damage connectors and result in operating problems which will be very difficult to isolate.

5. Place the SELECT switch on the AAC in the A, B, or AUTO position as desired.
6. Set the POWER switch on the Power Entry Module to ON. The system should boot from the hard disk; if it does not, press the Reset A button on the AAC. Normal operation should resume after the system is fully initialized.
7. Use a 1/8-inch bladed screwdriver to tighten the mounting screws at the sides of the card into the tapped holes on the mounting rails.
8. Enable the external alarm system.

6.2 ALARM INTERFACE CARD

WARNING: Only certified Cisco Systems technicians may remove or replace an AIC. Please contact Cisco Systems Technical Support if your AIC needs service.

7.0 TROUBLESHOOTING

The AAC is a rather simple device that will not usually fail during normal operation. However, the AAC interfaces with system controllers and external alarm systems which may cause alarm indications.

Always investigate the operational status of the system controller(s) and the external alarm contacts for faults, and review system logs before suspecting the AAC needs replacement. Remember that Generic software allows the host computer to trigger AUX 1 and AUX 2 alarms.

If the problem is not with the system controller(s) or external alarm circuits, try rebooting the system (both controllers in a redundant system). If a reset fails, then the AAC should be removed and replaced.

In the unlikely event of a software exception (e.g., a bus or address exception) on the active system controller, the AAC may not detect the problem for up to 5 seconds resulting in the a loss in the voice path. During the 5 second delay, stable calls remain on the Standby controller.

CAUTION: Initiating a reset at the AAC of an Active system controller will result in disruption of VCO/4K service. Set the system controller to Standby (redundant control) or be sure that such an interruption is acceptable prior to performing any of the troubleshooting procedures described above.

If replacing the AAC does not correct the problem, the AIC may be at fault and should be removed and replaced by an authorized Cisco Systems technician.

8.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation, and maintenance of the AAC and the Alarm Interface Card, refer to the following Cisco Systems, Inc. publications:

- VCO/4K Product Overview
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- VCO/4K System Administrator's Guide

Central Processing Unit (CPU - 16 MB)

1.0 GENERAL

The Central Processing Unit (CPU) is a high performance, VME bus compatible, single board computer that serves as the heart of a system controller. The CPU performs the following system functions:

- Directs read/write data transfers to and from cards on the VME bus
- Uses Transmission Control Protocol/Internet Protocol (TCP/IP) for host-to-system communication over an Ethernet interface
- Controls high speed data transfers to and from the hard and floppy disk drives in the system's Storage Subsystem
- Allows transparent access/transfer of system log and trace files between the system and an external device connected via the Ethernet interface
- Provides connections for system peripheral devices (master console, remote maintenance modem, and system printer)

The CPU card incorporates a 68030 type 32-bit microprocessor, 16 MB of dynamic RAM, with 512 Kbytes of ROM. A battery-backed up clock supports time-stamped applications.

2.0 SPECIFICATIONS

Microprocessor:	MC68030 (33 MHz)		
Real Time Clock:	Programmable real time clock with battery back-up		
Memory:	16 MB of DRAM		
Firmware:	512 MB of PROM		
Power Requirements:		typical	max
	+5Vdc	3.5 A	4.5 A
	+12Vdc		100mA
	-12Vdc		100mA
Physical Dimensions:	Height:	9.2 in (234mm)	
	Depth:	6.3 in (160mm)	
	Width:	0.8 in (19.8mm)	

3.0 CPU CARD CIRCUIT DESCRIPTION

The 68030 microprocessor supports VMEbus arbitration, memory addressing and refreshing, and multiple I/O ports. The real time clock is set though a system administration menu (refer to the *VCO/4K System Administrator's Guide* for more information). Figure 1 is a simplified block diagram of the CPU card.

The 68030 microprocessor (MPU) operates at 33MHz, and includes an asynchronous 32-bit data bus and 32-bit address bus. Memory and I/O devices communicate with the CPU card over its local system bus.

Information on I/O ports is provided in the CPU-TM description in *Section 4*.

3.1 VMEBUS ARBITRATION

The VMEbus is designed for multi-processor application. A CPU card functions as bus master in a system controller with the capability of forcing read or write transfers to and from other cards on the VMEbus. To perform this function, the CPU must be in Slot 1 of the upper 9-slot VME backplane. Bus arbitration is daisy-chained to the remaining slots in the backplane.

If the system is equipped with a redundant control subsystem, there are two system controllers. A CPU card is mounted in Slot 1 of the redundant upper VME backplanes.

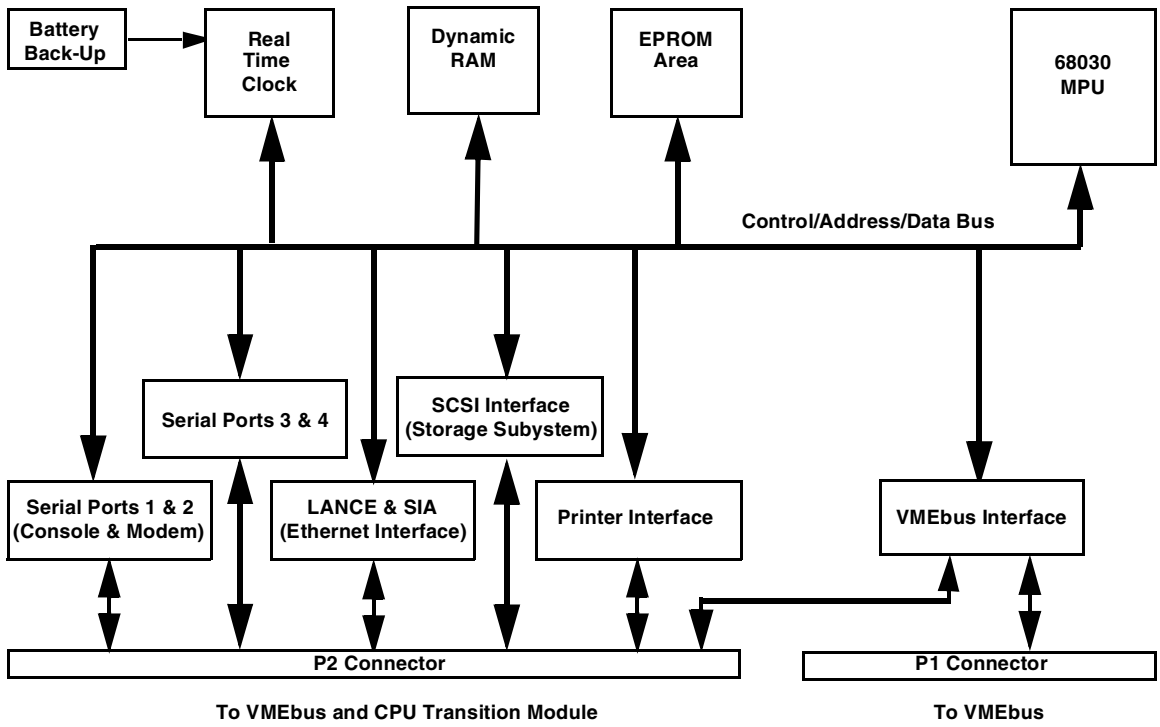


Figure 1: Block Diagram of the CPU Card

3.2 ON-BOARD DYNAMIC RAM

The on-board RAM (16MB) is accessible by the 68030 main processing unit (MPU), Local Area Network Controller for Ethernet (LANCE) and VMEbus. Dynamic, RAS-only, RAM refresh is done every 8ms by performing a memory cycle at each of the 512 row addresses. To accomplish this, once every 15ms, the refresh timer requests that the RAM sequencer performs a column address strobe.

3.3 FIRMWARE

There are four 32-pin EPROM sockets on the CPU cards. Two different PROM memory banks (two PROMs per bank) are used, one for boot-up and the other for the system application programs. During power-up, the microprocessor reads two vectors from the PROM area: the initial stack pointer and the initial program counter.

3.4 REAL TIME CLOCK

The real time clock provides seconds, minutes, hours, day, date, month, and year, in BCD 24-hour format. System administrators can reset the system clock through the Clock/Calendar Configuration screen under the System Configuration menu (refer to the *VCO/4K System Administrators Guide* for more information). Automatic corrections are made for 28, 29 (leap year) and 30 day months. The internal backup battery for the clock has a typical life span of from three to five years.

4.0 FUNCTIONAL DESCRIPTION OF THE CPU CARD

This section contains a functional description of the major components of the CPU card.

4.1 FRONT PANEL SWITCHES AND INDICATORS

Figure 2 shows the front panel layout of the CPU card. Two switches, RESET and ABORT, and four LED indicators (FAIL, STATUS, RUN and SCON) are located on the front panel of the card. The RESET switch forces a reset of all on-board devices and the VMEbus, but does not reset the system.

NOTE: To reset the system, use the RESET button(s) on the AAC.

The CPU front panel also contains a connector for a remote reset switch and cable assembly that performs the same function as the RESET switch. Cisco Systems, Inc. does not provide this switch/cable assembly and does not recommend its use.

The ABORT switch generates a Level 7 interrupt to the 68030 microprocessor. However, the VME bus is *not* reset.

The red FAIL LED illuminates when the 68030 microprocessor stops processing due to a board failure condition. Users should compare this LED to the yellow STATUS LED to diagnose the failure condition. The STATUS LED indicates a halt condition on the microprocessor. A halt indication following a successful system reset indicates a software problem or a possible DRAM error. A halt on reset may indicate a firmware problem. The PROMs on the CPU card could be improperly installed (wrong location or not in socket), or the firmware may not be at the proper revision level.

CAUTION: A FAIL condition indicates a severe problem that must be dealt with immediately to avoid prolonged loss of service. Reset the system controller from the AAC as a first course of action. If the FAIL condition continues, contact Cisco Systems Technical Support.

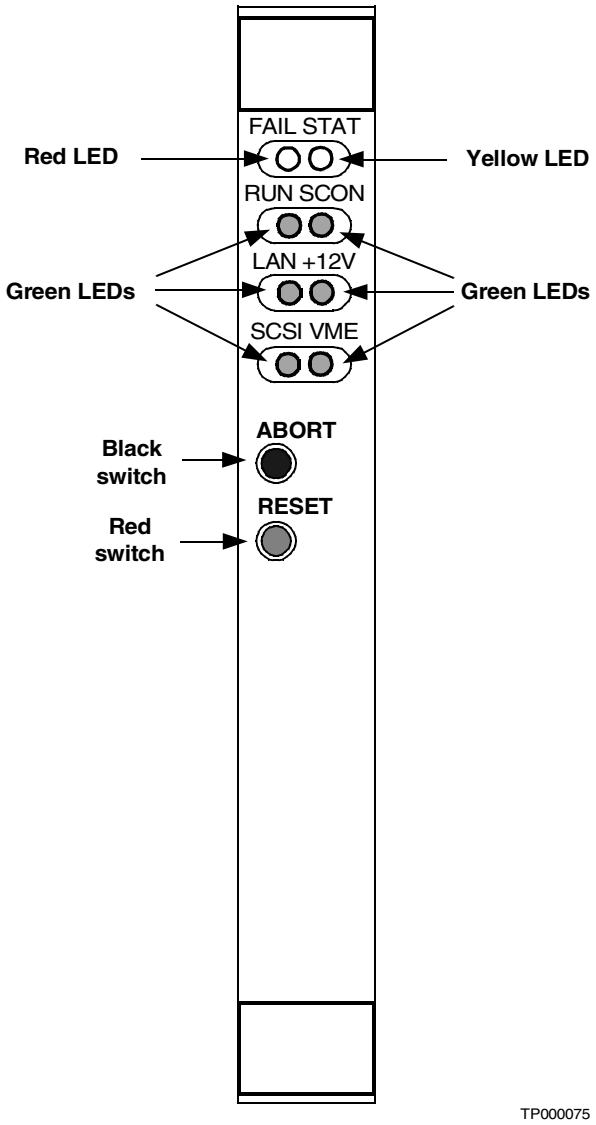


Figure 2: CPU Card Front Panel

The green RUN and SCON LEDs remain illuminated during normal operation. The RUN LED shows that the 68030 microprocessor is executing a normal bus cycle. The SCON LED shows that the CPU is the system controller. A summary table of front panel indicators is provided below.

Table 1: CPU Card LED Indicators and Meanings

FAIL Red	STATUS Yellow	RUN Green	CPU STATUS
OFF	OFF	OFF	No power applied to CPU or CPU is not the current local bus master.
OFF	OFF	ON	CPU waiting for cycle to complete.
OFF	ON	OFF	CPU is halted.
OFF	ON	ON	Normal operation.
ON	OFF	OFF	CPU is not current local bus master and board failure condition exists.
ON	OFF	ON	Board failure condition exists and CPU is waiting for cycle to complete.
ON	ON	OFF	CPU is halted and board failure condition exists.
ON	ON	ON	Complete board failure.

4.2 CONNECTORS

The CPU card plugs into the Combined Controller Assembly through two standard DIN 41612 triple-row, 96-pin male connectors.

5.0 CONFIGURATION NOTES

The CPU is a multipurpose OEM-supplied package modified by Cisco Systems, Inc. for operation in a system. Modifications include the insertion of custom PROM chips in the firmware sockets. Figure 3 uses gray scaling to show PROM locations on the CPU card.

5.1 PROM LOCATIONS – CPU CARD

CAUTION: Do not remove or reposition the jumpers on the CPU card. To do so may result in system failures and possible damage to the CPU card or to devices connected to it. Jumpers should remain in the factory-set position on the CPU card.

5.1.1 PROM 1

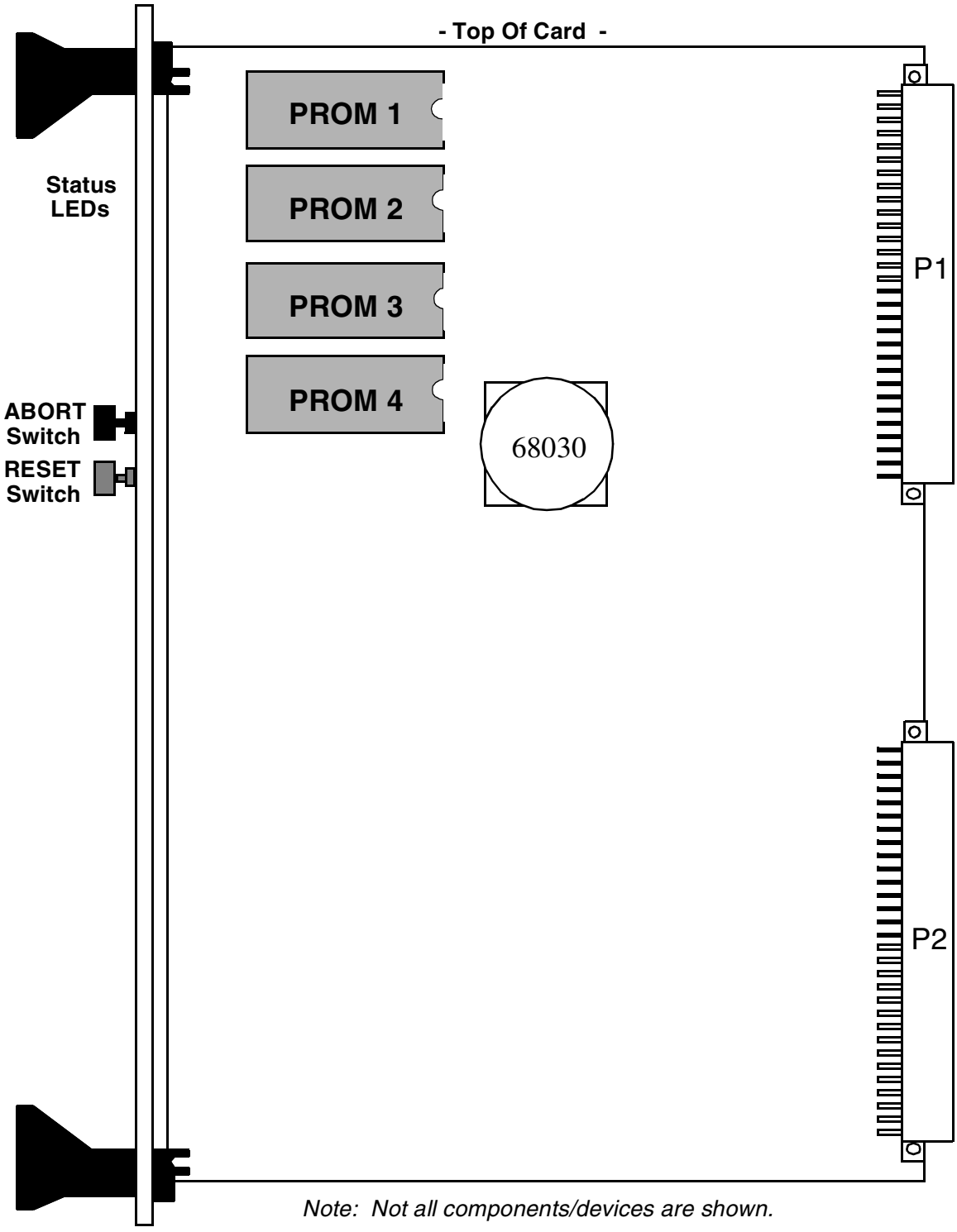
The 128Kx8 PROM1 contains firmware with the Low Kernel of the VRTX operating system.

5.1.2 PROM 2

The 128Kx8 PROM2 contains firmware labelled *High Kernel*.

5.1.3 PROM 3 AND PROM 4

PROMs 3 and 4 contain standard EPROM for CPU operation.



Note: Not all components/devices are shown.

Figure 3: CPU Card Jumper and PROM Locations

6.0 REMOVAL/REPLACEMENT INFORMATION

The CPU card must be the first card plugged into the upper VME backplane of both the primary and redundant system controllers for proper VMEbus control.

6.1 REMOVING & REPLACING SYSTEM CONTROLLER CARDS – GENERAL

CAUTION: Read all instructions before attempting to remove or replace a card.

To minimize the risk of injury from hazardous voltages, avoid contact with the backplane when removing or replacing system cards.

Observe antistatic precautions when handling a card to avoid damaging sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing cards or I/O modules.

Control Circuit cards require slightly different procedures for removal and replacement. However, there are some common procedures to be followed before removing and after replacing a circuit card.

6.1.1 ALL SYSTEMS

The CPU card contains the serial number required for the system's Time-Slot Allocation License. This serial number was encoded in the card at the factory and cannot be altered. After the CPU card is replaced, the Time-Slot Allocation License must be updated before the system will operate normally. For information on how to update the license, refer to the *VCO/4K System Administrator's Guide*.

6.1.2 NON-REDUNDANT CONTROL SYSTEM

For a system with one Combined Controller Assembly, the system will be out of service until the failed Combined Controller Assembly is replaced. To remove and replace a Combined Controller Assembly in a non-redundant control system:

1. Power off the system, following the instructions in your *VCO/4K System Maintenance Manual*.
2. Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 4) on the system. Keep the retainers and screws together in a safe place for replacement later.

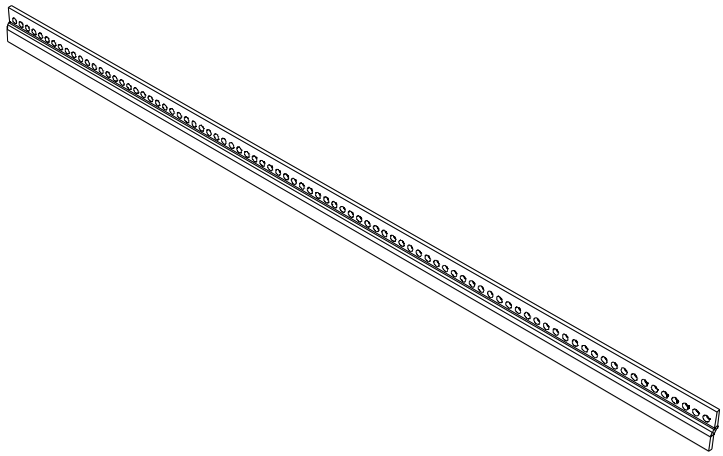


Figure 4: PCB Card Retainer Bar

3. Remove and replace the failed Combined Controller Assembly(s).
4. Power on the system, following the instructions in your V*CO/4K System Maintenance Manual*. The system should boot from hard disk; if it does not, press the Reset A button on the AAC. Normal operation should resume after the system has been fully initialized.

6.1.3 REDUNDANT CONTROL SYSTEM

To remove and replace a CPU card in a system with redundant control:

1. Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 4) on the system. Keep the retainers and screws together in a safe place for replacement later.
2. Place the Combined Controller Assembly to be serviced in Standby mode; use the Select Switch on the Alarm Arbiter Card (AAC) to designate the other Combined Controller Assembly as Active.
3. When the transition to Standby is complete, remove the entire Combined Controller Assembly. Calls will be processed through the Active controller.
4. When the service activity has been completed, restore power to the standby side.
5. Press the RESET button of the serviced side on the AAC. The serviced Combined Controller Assembly should boot from hard disk. The update channel will be established and automatic file synchronization will be initiated.
6. When file synchronization is completed, the serviced Combined Controller Assembly should be in Standby mode. Return the Side Select on the AAC to Auto, if desired.

6.2 REMOVAL PROCEDURES

To remove a CPU card:

1. Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 4) on the system. Keep the retainers and screws together in a safe place for replacement later.
2. Remove the entire Combined Controller Assembly from active service (refer to *Section 6.1*).

   CAUTION: Always remove the Combined Controller Assembly before removing the CPU card. Never remove a CPU card from a Combined Controller Assembly that is mounted in a system.
3. Use your thumbs to push the upper and lower ejectors away from the Combined Controller Assembly front panel. This action will pop the card from the SWI connectors.

   NOTE: Cards should be removed and replaced using only enough force to disengage or engage the card from or into backplane connectors. Yanking cards from, or jamming cards into, the backplane can seriously damage connectors and result in operating problems which will be very difficult to isolate.
4. With both hands, grasp the Combined Controller Assembly on its top and bottom edges as you remove it from the card slot. Pull the Combined Controller Assembly from the card slot.
5. When you have removed the Combined Controller Assembly from the card slot, place it on an antistatic mat or envelope.
6. Use a 1/8-inch bladed screwdriver to loosen the captive mounting screws at the top and bottom of the CPU card. Do not remove the screws from the cards.
7. Use your thumbs to push the upper and lower extractors away from the CPU card front panel. This action disconnects the card from the SWI connectors.
8. Pull the CPU card away from the Combined Controller Assembly.
9. Place the CPU card on an antistatic mat or an antistatic envelope.

6.3 REPLACEMENT PROCEDURES

To replace the CPU card:

1. Place the replacement CPU card on the antistatic mat or envelope.

   NOTE: Refer to your release notes and verify that the revision levels of the PROMs match the requirements of the generic software currently loaded in your VCO/4K system.

   CAUTION: Always remove the Combined Controller Assembly before replacing the CPU card. Never replace a CPU card in a Combined Controller Assembly that is mounted in a system.

2. Grasp the replacement CPU card by the top handle and the bottom edge and align it with the top and bottom card guides of the Combined Controller Assembly.
3. Push the CPU card in until it makes contact with the SWI connectors. Use your thumbs to push the extractors toward the front panel.
4. Replace the screw at the top of the CPU card front panel.
5. With both hands, grasp the Combined Controller Assembly on its top and bottom edges and align it with the top and bottom card guides of the card slot.
6. Push the Combined Controller Assembly inward until it makes initial contact with the backplane.

   Make sure the ejector levers are perpendicular to the front panel. Continue pushing the Combined Controller Assembly inward until it makes firm contact with the backplane. The hooks on the ejectors must be behind the front rail of the card slot. Use your thumbs to push the ejectors inward toward the front panel. The card should be fully seated into the backplane connectors when the levers are flush against the front panel.
7. Grasp the replacement CPU card by the top handle and the bottom edge and align it with the top and bottom card guides of the Combined Controller Assembly.
8. Push the card inward until it makes contact with the backplane.
9. Firmly grasp the handles at the top and bottom of the CPU card and push the card toward the backplane. The card fits tightly into the backplane connectors and some force is required to seat the card back firmly into the backplane connectors.
10. Use a 1/8-inch bladed screwdriver to tighten the mounting screws at the top and bottom of the CPU card.
11. Refer to *Section 6.1* and place the Combined Controller Assembly back in service.
12. Reinstall the top and bottom PCB card retainer bars (see Figure 4). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers (five per bar).

    CAUTION: The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

7.0 TROUBLESHOOTING

7.1 HOST COMMUNICATIONS – SYSTEM

The *VCO/4K System Maintenance Manual* describes corrective maintenance procedures for host communications links. In addition to this manual, you should refer to the *VCO/4K Standard or Extended Programming Reference* for details relating to command/report formats. The *VCO/4K System Administrator's Guide* describes the network messages associated with problems detected with the host communications links.

If you are using the optional Ethernet Communications Package, refer to the *VCO/4K Ethernet Supplement* for maintenance procedures.

Other reference materials include the OEM manuals supplied with the host computer I/O package and the modems used for the link (optional), and any documentation related to the communication and application packages to be run on the host computer.

7.2 FAULT ISOLATION - CPU CARD

To isolate and correct CPU card problems perform the steps detailed below:

CAUTION: Initiating a reset on the CPU card in an Active Combined Controller Assembly will result in disruption of system service. Set the Combined Controller Assembly to Standby (redundant control) or be sure that such an interruption is acceptable prior to performing any of the troubleshooting procedures described below.

1. Verify that power is available to the Combined Controller Assembly and COMM bus. Check all power cabling to and from the Power Subsystem.
2. Perform a reset by pressing and releasing the RESET switch on the Alarm Arbiter Card (AAC) front panel. The LED on the hard disk drive should go ON and OFF intermittently. When the reboot is completed the RUN, +12V, and SCON indicators should be illuminated.
3. If the Combined Controller Assembly will not reboot, remove and reseat the CPU card into the Combined Controller Assembly. Perform a reset and observe the hard disk drive.
4. Refer to the *VCO/4K System Maintenance Manual* for additional information on system level troubleshooting techniques. If all else fails, call Cisco Systems Technical Support.

8.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the CPU refer to the following system publications:

- *VCO/4K Product Overview*
- *VCO/4K System Maintenance Manual*
- *Control Subrack Technical Description*

Combined Controller Assembly (CCA)

1.0 GENERAL

The Combined Controller Assembly consists of the following components:

- Central Processing Unit (CPU) card (33 MHz)
- Switch Interface (SWI) and floppy disk drive assembly

The CPU is a high performance, single-board computer that serves as the heart of the system controller.

The SWI provides an interface between the system controller and the following sub-systems: Network Bus Controller-3 (NBC-3), Alarm Arbiter Card (AAC), and redundant system controller.

The floppy disk drive is a 1.44 MB high density, 3-1/2 inch, half-height floppy disk drive. The floppy disk drive is used to load software and make back-up copies of the system data base. You can also choose to store the system data base, and log and trace files on floppy disk.

The SWI/floppy disk drive assembly also acts as a carrier for the CPU card.

Figure 1 shows the front of a VCO/4K and the location of the Combined Controller Assembly.

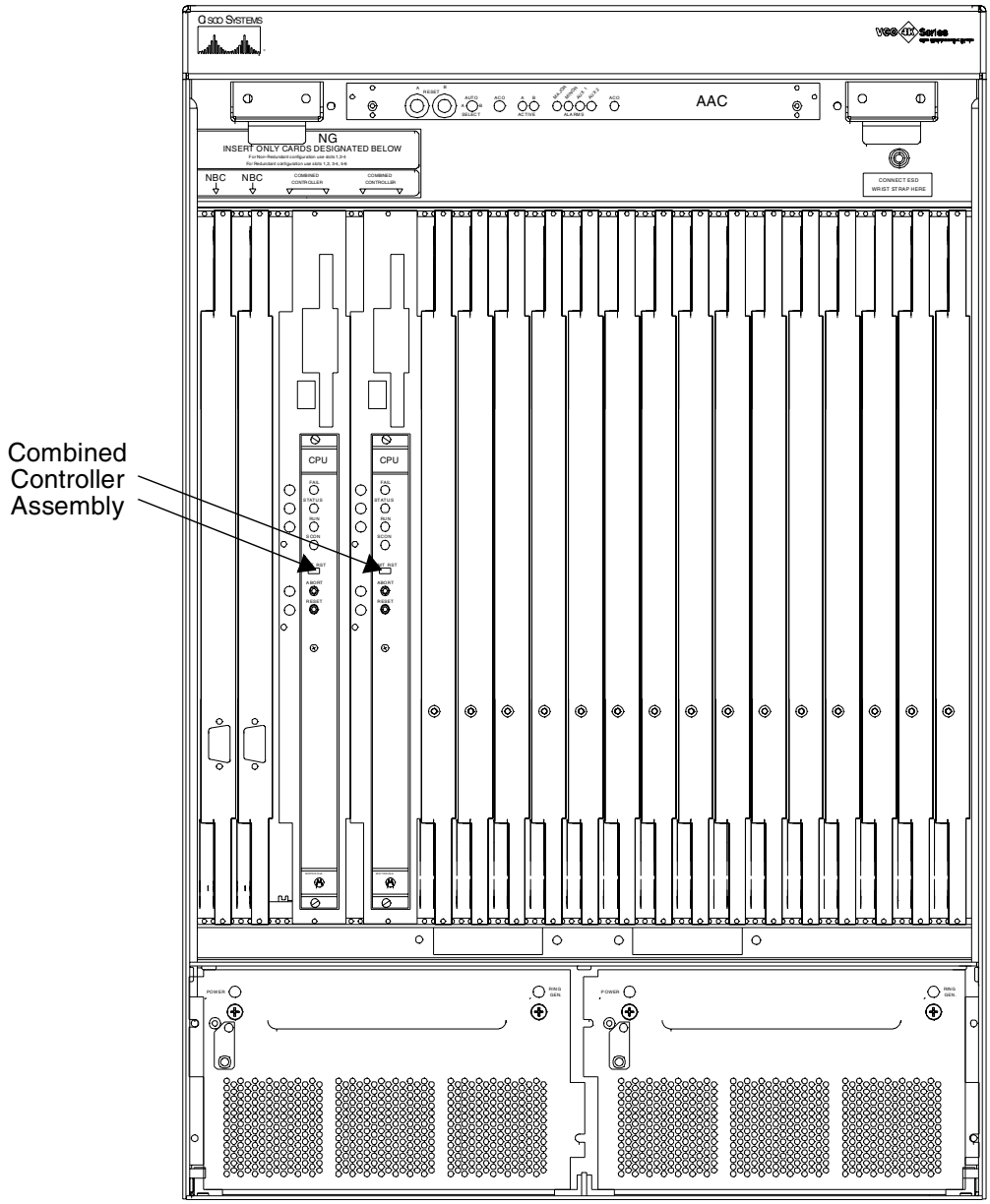


Figure 1: Combined Controller Assembly (Front Panel)

Figure 2 is a top view of the Combined Controller Assembly, showing its components.

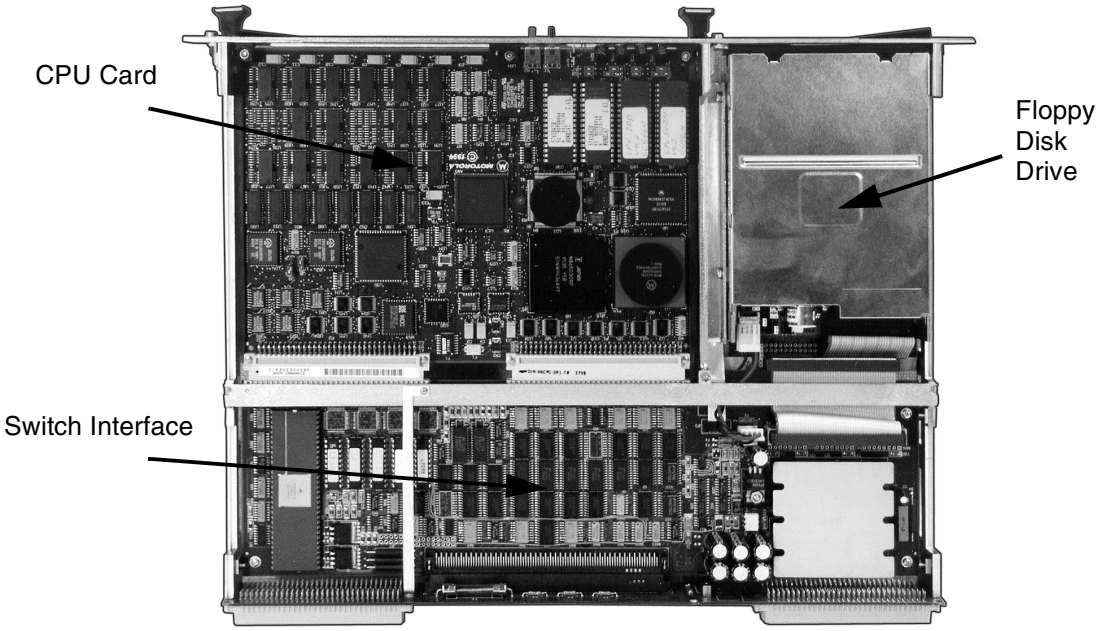


Figure 2: Combined Controller Assembly (Top View)

2.0 SPECIFICATIONS

Power Requirements:	+5Vdc	
	-48Vdc	
	-15Vdc	
Physical Dimensions:	Height:	15.6 in. (396mm)
	Depth:	12.1 in. (305mm)
	Width:	0.79 in. (20mm)

3.0 CPU CARD

The CPU performs the following system functions:

- Directs read/write data transfers to and from the Switch Interface
- Supports host-to-system communication over an Ethernet interface with Transmission Control Protocol/Internet Protocol (TCP/IP)
- Controls high-speed data transfers to and from the hard and floppy disk drives in the Storage Subsystem
- Allows transparent access/transfer of system log and trace files between the system and an external device connected via the Ethernet interface
- Provides control to peripheral devices (master console, remote maintenance modem, and system printer)

The CPU card incorporates a 68030 type 32-bit microprocessor, 16 Mbytes of dynamic RAM, and 512 Kbytes of ROM. A battery backed-up clock supports time-stamped applications.

3.1 SPECIFICATIONS

Microprocessor:	MC68030 (33MHz)
Real Time Clock:	Programmable real-time clock with battery back-up
Memory:	16 Mbytes of DRAM
Firmware:	512 Kbytes of EPROM
Physical Dimensions:	Height - 9.2 in (234mm)
	Depth - 6.3 in (160mm)
	Width - 0.8 in (19.8mm)

3.2 CPU CARD CIRCUIT DESCRIPTION

The 68030 microprocessor supports memory addressing and refreshing, and multiple I/O ports. The real-time clock is set through a system administration menu (refer to the *VCO/4K System Administrator's Guide* for more information). Figure 3 is a simplified block diagram of the CPU card.

The 68030 microprocessor (MPU) operates at 33 MHz and includes an asynchronous 32-bit data bus and 32-bit address bus. Memory and I/O devices communicate with the CPU card over its local system bus.

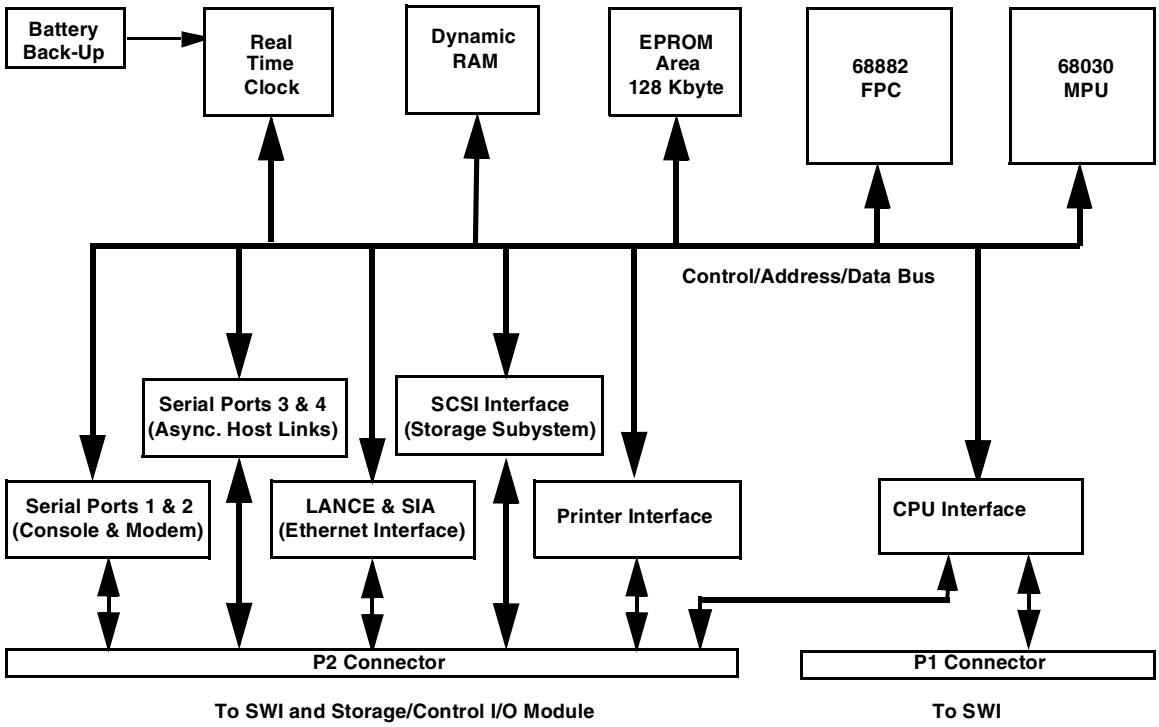


Figure 3: Block Diagram of CPU Card

3.2.1 ON-BOARD DYNAMIC RAM

The on-board RAM (16 Mbytes) is accessible by the 68030 Main Processing Unit (MPU) and Local Area Network Controller for Ethernet (LANCE). The CPU refreshes dynamic, RAS-only, and RAM every 8ms by cycling through the memory at each of the 512 row addresses. To accomplish this, once every 15ms, the refresh timer requests that the RAM sequencer performs a column address strobe.

3.2.2 FIRMWARE

There are four 32-pin EPROM sockets on the CPU card. Two different EPROM memory banks (2 PROMs per bank) are used—one for boot-up and the other for the system application programs. During power-up, the microprocessor reads two vectors from the EPROM area: the initial stack pointer and the initial program counter.

3.2.3 REAL TIME CLOCK

The real time clock provides seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. The Clock/Calendar Configuration screen under the System Configuration menu allows users to reset the system clock via system administration (refer to the *System Administrator's Guide* for more information). Automatic corrections are made for 28, 29 (leap year) and 30-day months. The internal backup battery for the clock has a typical life span of three to five years.

3.2.4 FRONT PANEL SWITCHES AND INDICATORS

Two switches, RESET and ABORT, and four LED indicators (FAIL, STATUS, RUN, and SCON) are located on the front panel of the CPU card. The RESET switch forces a reset of all on-board devices, but does not reset the system.

NOTE: To reset the system, use the RESET *button(s) on the AAC.*

The Combined Controller front panel also contains a connector for a remote reset switch and cable assembly that performs the same function as the RESET switch. Cisco Systems, Inc. does not provide this switch/cable assembly and does not recommend its use.

The ABORT switch generates a Level 7 interrupt to the 68030 microprocessor.

The red FAIL LED illuminates when the 68030 microprocessor stops processing due to a board failure condition. Users should compare this LED to the yellow STATUS LED to diagnose the failure condition. The STATUS LED indicates a halt condition on the microprocessor. A halt indication following a successful system reset indicates a software problem or a possible DRAM error. A halt on reset may indicate a firmware problem. The PROMs on the CPU card could be improperly installed (wrong location or not in socket), or the firmware may not be at proper revision level.

CAUTION: A FAIL condition indicates a severe problem that must be dealt with immediately to avoid prolonged loss of service. Reset the system controller from the AAC as a first course of action. If the FAIL condition remains, contact Cisco Systems, Inc. Technical Support.

The green RUN and SCON LEDs remain illuminated during normal operation. The RUN LED indicates the 68030 microprocessor is executing a normal bus cycle. The SCON LED indicates the CPU is the system controller. The following table describes the front panel status LEDs.

Table 1: CPU Card LED Indicators and Meanings

FAIL Red	STATUS Yellow	RUN Green	CPU STATUS
OFF	OFF	OFF	No power applied to CPU or CPU is not the current local bus master.
OFF	OFF	ON	CPU waiting for cycle to complete.
OFF	ON	OFF	CPU is halted.
OFF	ON	ON	Normal operation.
ON	OFF	OFF	CPU is not current local bus master and board failure condition exists.
ON	OFF	ON	Board failure condition exists and CPU is waiting for cycle to complete.
ON	ON	OFF	CPU is halted and board failure condition exists.
ON	ON	ON	Complete board failure.

3.2.5 CONNECTORS

The CPU card plugs into the SWI/floppy disk drive assembly through two standard DIN 41612 triple-row, 96-pin male connectors.

3.3 CONFIGURATION NOTES

The CPU is a multipurpose, OEM-supplied package modified by Cisco Systems, Inc. for operation in a system. Modifications include the insertion of custom EPROM chips in the firmware sockets.

3.3.1 EPROM LOCATIONS – CPU CARD

CAUTION: Do not remove or reposition the jumpers on the CPU card, as this may result in system failures and possible damage to the CPU card or to devices connected to it. Jumpers should remain in the factory-set position on the CPU card and should not be removed or changed.

3.3.2 EPROM 1

The 128Kx8 EPROM1 contains firmware with the Low Kernel of the VRTX operating system.

3.3.3 EPROM 2

The 128Kx8 EPROM2 contains firmware labelled *High Kernel*.

3.3.4 EPROM 3 & EPROM 4

EPROMs 3 and 4 contain boot EPROM for CPU operation.

4.0 SWITCH INTERFACE (SWI) AND FLOPPY DISK DRIVE ASSEMBLY

4.1 SPECIFICATIONS

DMA Controller:	68450 (4 MHz)	
Memory:	64K Bytes Static RAM	
Formatted Capacity:	1.44 Megabytes	
Signal Interface:	SCSI	
Recording Method:	MFM	
Media Requirement:	3.5-inch, high density (2HD) micro floppy diskettes	
Rotational Speed:	300 rpm	
Read/Write Heads:	2 heads	
Track Density:	135 tracks per inch (tpi)	
Data Transfer Rate:	500 Kbps	
Physical Dimensions:	Height:	15.6 in. (396mm)
	Depth:	12.1 in. (305mm)
	Width:	1.58 in. (40mm)

4.2 SWI CARD CIRCUIT DESCRIPTION

The SWI is located on the Combined Controller Assembly along with the floppy disk drive and outer backplane. The SWI card generates the specific voltages that are used by the CPU card and the floppy disk drive and Storage/Control I/O Module. It also passes SCSI information to the floppy disk drive and the hard disk drive. The hard disk drive is located on the Storage/Control I/O Module.

The SWI provides a memory-addressable interface from the CPU to the NBC-3 and the AAC. The SWI also passes power to the AAC (see Figure 4).

The NBC-3 interface includes a 16-bit bi-directional data path and handshaking signals. This path carries command data and call setup data loaded into SWI registers by the system controller CPU. Two uni-directional 8-bit data channels allow communication between the A-side and B-side SWI cards in redundant systems.

4.2.1 DMA CONTROLLER

All data transfers between the NBC-3 and SWI, or between two SWIs, are performed by a 68450 4-channel bi-directional DMA controller. The DMA controller only transfers data to and from the SWI's on-board 64 KB of static RAM. The SWI cannot write data to and from the CPU as a bus master.

The 68450 is a four-channel DMA controller. Channels 0 and 1 are configured for 16-bit data transfers to and from the NBC-3. Channels 2 and 3 are configured for 8-bit data transfers to and from the SWI in a redundant system configuration. Channels 0 and 2 are dedicated to incoming data; channels 1 and 3 are used for outgoing (relative to the SWI) data.

Logic on the SWI causes a DMA operation to terminate normally when the last byte/word of data is sent or received. When a data transfer is complete, the DMA controller interrupts the CPU. On the CPU's interrupt acknowledge cycle, the DMA controller returns the appropriate channel's normal interrupt vector.

If a bus error occurs while the DMA controller is in control of the internal SWI bus, the DMA controller terminates the bus cycle, aborts the transfer, sets the channel error register to indicate that a bus error occurred, and interrupts the CPU. On the CPU's interrupt acknowledge cycle, the DMA controller returns the appropriate channel's error interrupt vector.

4.2.2 PATH SETUP

Two sets of bi-directional registers are provided on the SWI. These registers are loaded by the CPU to send path setup information to the NBC-3. Verify path setup information by reading the contents of these registers.

4.2.3 STATIC RAM

Static RAM on the SWI is isolated from the CPU so that DMA transfers to and from memory can occur without interrupting activity on the CPU. When CPU access to any on-board SWI device occurs, the current DMA cycle, if any, is completed before the CPU access takes place.

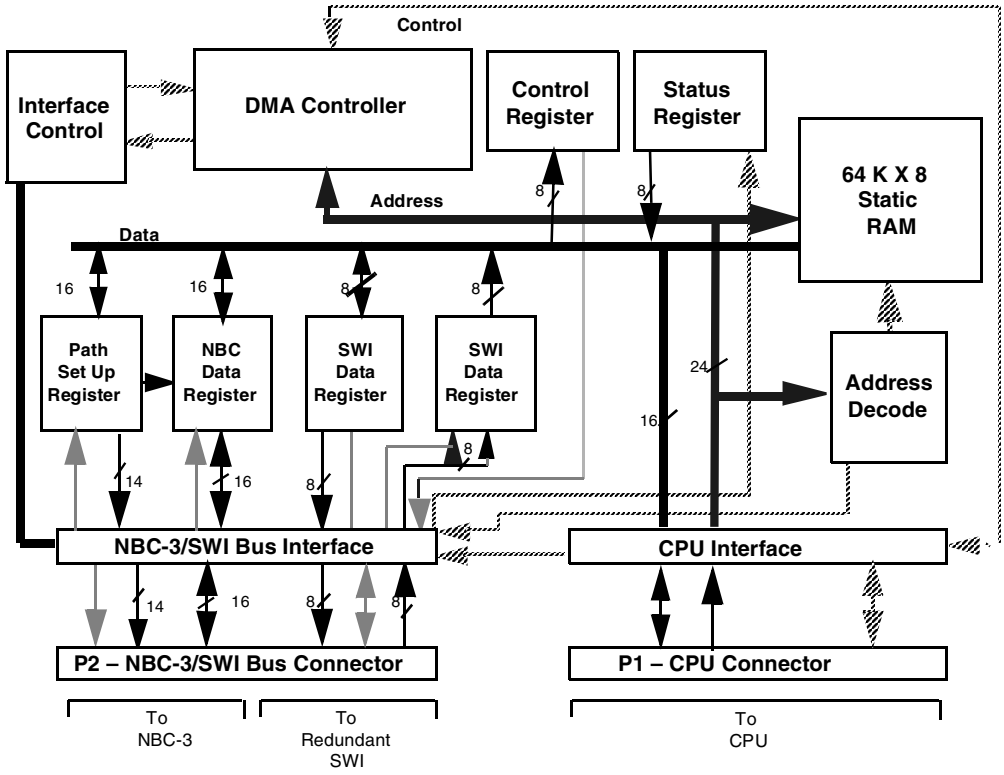


Figure 4: Block Diagram of SWI Card

4.2.4 SWI INTERCONNECTIONS

The signals between SWIs are carried on the control midplane. The signals to the AAC are carried to the control midplane and then through a ribbon cable to the Alarm Interface Card (AIC). The AAC then seats directly into the AIC. The connection between the SWI and the NBC-3 is made through the control midplane.

4.3 FLOPPY DISK DRIVE DESCRIPTION

The floppy disk drive is a 1.44 Mbyte high density, 3-1/2 inch, half-height floppy disk drive. Use the floppy disk to load software and make back-up copies of the system data base. Disk utilities are accessible from the Maintenance menu during system operation and from the Software Installation Utility diskette when this diskette is used to initialize the system.You can also choose to store the system data base, and log and trace files on floppy disk. Refer to the *VCO/4K System Administrator's Guide* for more information.

The drive reads/writes to 3-1/2" double-sided, high density (2HD) diskettes. Files are stored on the floppy drive in MS-DOS format. The floppy drive has a black ABS plastic front with a disk ejection button and a drive access LED indicator.

4.4 FRONT PANEL LEDS

The front panel of the Combined Controller Assembly contains five LEDs.

Three SWI status LEDs are located at the top of the front panel. These LEDs are OFF when the card is operating normally. The red (top) LED is illuminated when either the system controller or the NBC-3 fails. All LEDs are illuminated during system initialization.

The red 12VF LED located near the bottom of the panel shows a local 12-volt combined controller power failure.

The red HDD LED located below the 12VF LED shows hard disk drive activity.

5.0 REMOVAL & REPLACEMENT PROCEDURES

5.1 COMBINED CONTROLLER ASSEMBLY

System controllers require slightly different procedures for removing and replacing the other cards. Depending on whether you have a redundant or a non-redundant system, there are some common procedures to follow before removing and after replacing the combined controllers. These procedures are discussed in the following sections.

CAUTION: Observe antistatic precautions whenever handling the Combined Controller Assembly to avoid damage to sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing control circuit cards.

For a system with one Combined Controller (non-redundant systems), the system remains out of service until a failed Combined Controller Assembly is replaced.

To remove and replace a Combined Controller in a non-redundant system:

1. Power off the system, according to the instructions in the *VCO/4K System Maintenance Manual*.
2. Remove and replace the Combined Controller Assembly.
3. Power on the system, according the instructions in the *VCO/4K System Maintenance Manual*. The system should boot from the hard disk. If it does not, press the RESET A button on the AAC. Normal operation should resume after the system is fully initialized.

To remove and replace a Combined Controller Assembly in a redundant system:

1. Use the system administration menus to place the Combined Controller Assembly to be serviced in STANDBY mode. Refer to the *VCO/4K System Administrator's Guide* for more information.
2. Remove and replace the STANDBY Combined Controller Assembly. Calls will continue to be processed through the ACTIVE system.
3. When the service activity is complete, use the system administration menus to place the STANDBY Combined Controller Assembly in ACTIVE mode. Refer to the *VCO/4K System Administrator's Guide* for more information.The update channel is established and automatic file synchronization is initiated.

5.1.1 REMOVAL PROCEDURES

To remove a Combined Controller Assembly:

1. Wear a ground strap connected to the VCO/4K equipment frame.
2. Use a #1 Phillips-head screwdriver to remove the mounting screws/washers (five per bar) from the top and bottom PCB card retainer bars (see Figure 5) on the system. Keep the retainers and screws together in a safe place for replacement later.

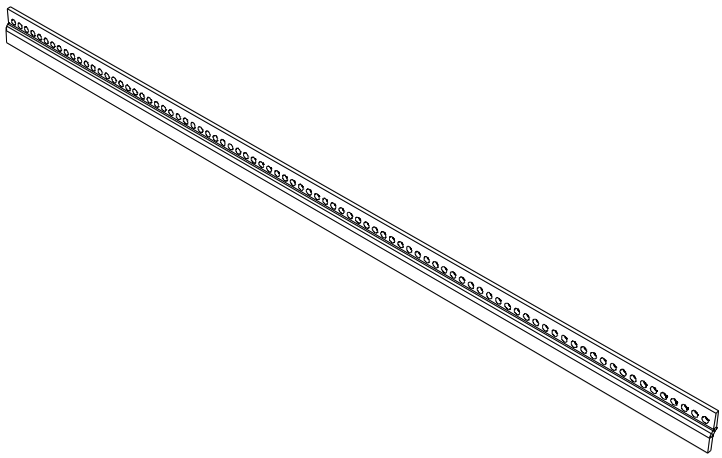


Figure 5: PCB Card Retainer Bar

3. Use your thumbs to push the upper and lower extractors away from the card front panel. This action disconnects the assembly from the backplane connectors.
4. Pull the Combined Controller Assembly away from the card slot.
5. When the card is removed, place it on an antistatic mat or an antistatic envelope.

5.1.2 REPLACEMENT PROCEDURES

To replace a Combined Controller Assembly:

1. Wear a ground strap connected to the VCO/4K equipment frame.
2. Grasp the replacement Combined Controller Assembly by the top handle and the bottom edge and align it with the top and bottom card guides of the rack.

WARNING: Be sure to plug the Combined Controller Assembly into the slot marked for the Combined Controller Assembly. Plugging the Combined Controller into the wrong slot may cause serious damage to the controller.

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3. Be sure the extractor levers are perpendicular to the front panel. Push the Combined Controller Assembly into the rack until it makes contact with the backplane. The hooks on the extractors must be behind the front rail of the rack.
4. Reinstall the top and bottom PCB card retainer bars (see Figure 5). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers (five per bar).

CAUTION: The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

5.2 CPU CARD

The CPU card contains the unique serial number required for the system's Time-Slot Allocation License. This serial number was encoded in the card at the factory and cannot be altered. After the CPU card is replaced, you must update the Time-Slot Allocation License before the system will operate normally. For information on how to update the license, refer to the *VCO/4K System Administrator's Guide*.

5.2.1 REMOVAL PROCEDURES

To remove a CPU card:

1. Wear a ground strap connected to the VCO equipment frame.
2. Remove the Combined Controller Assembly. Refer to the previous section for more information.

   CAUTION: Always remove the Combined Controller Assembly before removing the CPU card. Never remove a CPU card from a Combined Controller Assembly that is mounted in a system.
3. Remove the screw at the top of the CPU card front panel.
4. Use your thumbs to push the upper and lower extractors away from the CPU card front panel. This action disconnects the card from the SWI connectors.
5. Pull the CPU card away from the Combined Controller Assembly.
6. Place the CPU card on an antistatic mat or an antistatic envelope.

5.2.2 REPLACEMENT PROCEDURES

To replace the CPU card:

1. Wear a ground strap connected to the VCO equipment frame.

   CAUTION: Always remove the Combined Controller Assembly before replacing the CPU card. Never replace a CPU card in a Combined Controller Assembly that is mounted in a system.
2. Grasp the replacement CPU card by the top handle and the bottom edge and align it with the top and bottom card guides of the Combined Controller Assembly.
3. Push the CPU card in until it makes contact with the SWI connectors. Use your thumbs to push the extractors toward the front panel.
4. Replace the screw at the top of the CPU card front panel.
5. Replace the Combined Controller Assembly. Refer to the previous section for more information.

6.0 TROUBLESHOOTING

6.1 FAULT ISOLATION

6.1.1 CPU CARD

Use the following steps to isolate and correct programs with the CPU card:

CAUTION: Initiating a reset on the CPU card in an ACTIVE Combined Controller Assembly will result in disruption of system service. Set the Combined Controller to STANDBY (redundant control) or be sure that such an interruption is acceptable prior to performing any of the troubleshooting procedures described below.

1. Verify that power is available to the Combined Controller Assembly. Check all power cabling to and from the Power Subsystem. Also, check the 12V Fail LED on the front panel of the Combined Controller Assembly.
2. Perform a reset by pressing and releasing the appropriate RESET switch on the Alarm Arbiter Card (AAC) front panel. The hard disk drive access LED should go ON and OFF intermittently. When the reboot is complete, the RUN and SCON indicators should be illuminated.
3. If the Combined Controller will not reboot, remove it and check that the CPU is properly seated. Perform a reset and observe the hard disk drive.
4. If the Combined Controller resets but the login screen does not appear on the master console screen, the problem may be due to either the VDT or the connecting cable. Check the cable and refer to the OEM manual supplied with the VDT for troubleshooting procedures.
5. Refer to the *VCO/4K System Maintenance Manual* for additional information on system-level troubleshooting techniques. If all else fails, call Cisco Systems, Inc. Technical Support.

6.1.2 SWI/FLOPPY DISK DRIVE ASSEMBLY

Use the following steps to isolate and correct problems with the SWI/floppy disk drive assembly:

1. Problems with the floppy disk drive are indicated by error messages displayed on the master console and status LEDs on the front of the Combined Controller.
2. Refer to the *VCO/4K System Maintenance Manual* for additional information about system level troubleshooting techniques. If all else fails, call Cisco Systems, Inc. Technical Support.

6.2 ERROR MESSAGES

Problems with the floppy disk drive are shown in error messages generated when the operating system attempts to read or write files to the drive. These messages are displayed on the master console screen and stored in the system error log on the hard disk. A review of the error logs will reveal developing patterns of stored file errors. These errors may indicate impending failure of a floppy disk drive component. Messages associated with floppy disk drive errors begin with a "PRM" prefix. The *System Administrator's Guide* contains a complete listing of error messages with brief definitions.

Problems with the SWI are shown in error messages generated when the SWI/NBC-3 interface fails. If such messages are discovered, refer to the *VCO/4K System Administrator's Guide* and the *Technical Description: Network Bus Controller-3 (NBC-3)* for additional troubleshooting information.

6.3 LEDS

6.3.1 CPU CARD

If error messages indicate stored file problems, look to the CPU card LEDs and verify these indicators. If the CPU card appears to be operating normally, use the Disk Utilities menu under the Maintenance menu to call up a directory of the drive (refer to the *VCO/4K System Administrator's Guide*). Observe the access LEDs on the floppy disk drive and hard disk drive. These LEDs should be illuminated as the operating system reads the directory.

6.3.2 SWI/FLOPPY DISK DRIVE ASSEMBLY

The red SWI LED located at the top of the panel indicates a major alarm condition when either the system controller or the NBC-3 fails.

The red 12VF LED located at the bottom of the panel indicates a local 12V combined controller power failure.

The red HDD LED located above the 12VF LED indicates hard disk drive activity.

The floppy disk drive access LED is illuminated when the drive is accessed for a read/write operation. This LED should illuminate under the following conditions:

- During a reinstall from a floppy
- When saving or loading the data base to or from floppy disk
- During initialization of a floppy
- When reading a directory

7.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation, and maintenance of the Combined Controller Assembly, refer to the following documentation:

- VCO4K Product Overview
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- VCO/4K Technical Description: Storage/Control I/O Module
- VCO/4K Technical Description: Modular Power Subsystem
- Technical Description: Network Bus Controller-3 (NBC-3)
- VCO/4K System Administrator's Guide

Network Bus Controller 3 Card (NBC3)

1.0 GENERAL

The Network Bus Controller 3 (NBC3) is a special control circuit card that drives the communications bus (Comm Bus) and timeslot address bus, and generates the system clocks. The NBC3 also provides the data communication path between other control circuit cards and the rest of the system.

The intelligence of the NBC3 comes from an on-board 68360 microprocessor. The 68360 microprocessor memory includes 1MB RAM (selectable) and 256KB of EPROM.

The 68360 processor allows the NBC3 to serve as the Comm Bus master. The Switch Interface (SWI) functions as a direct memory access (DMA) interface to the NBC3 for communication with the other control circuit cards. Redundant NBC3 cards operate in active or standby mode, depending on which controller is selected as master through the Alarm Arbiter Card (AAC).

CAUTION: Do not pull the active side NBC3 on an operating production switch. Pulling an active NBC3 can generate errors and impact traffic. If you suspect a problem with an NBC3 card and you wish to remove it, first switch sides to make it the standby side.

The NBC3 uses dynamic random access memory (DRAM) for program storage. The program/application is downloaded from the CPU card to the NBC3 through the SWI.

The NBC3 implements special Phase Locked Loop (PLL) circuitry that allows for system synchronization to the network via incoming T1/E1 facilities, or to the Central Office (CO) composite clock from a Building Integrated Timing Source (BITS) signal, or to the internal clock.

The card is equipped with a Stratum 4 clock.

1.1 DTG-2 MEZZANINE CARD

The NBC3 has connections for a DTG-2 mezzanine card. The DTG-2 mezzanine card functions the same as the full size DTG card. You can use either DTG card in your system. However, the DTG-2 mezzanine card does not require its own card slot. For more information on the DTG or DTG-2 card, refer to the *Digital Tone Generator (DTG) Card Technical Description* or the *Digital Tone Generator 2 (DTG-2) Mezzanine Card Technical Description*.

2.0 SPECIFICATIONS

Microprocessor	MCG8EN360-25
Memory	1, 2, 4, or 8MB DRAM SIMM 256KB EPROM
Power Requirements (Typical)	5 Volts – 4000 mA +15 Volts – 350 mA -15 Volts – 375 mA
System Synchronization:	
Clock Input	1.544 MHz ±75Hz (bus) 64 KHz ± 6.4 Hz (external)
Internal Reference Clock	1.544 MHz ± 40 Hz (standard) 1.544 MHz ± 7.1 Hz
Physical Dimensions	Height – 15.6 inches (in.) (396mm) Depth – 12.1 in. (305mm) Width – 0.79 in. (20mm)

3.0 CIRCUIT DESCRIPTION

Figure 1 is a block diagram of the NBC3 card.

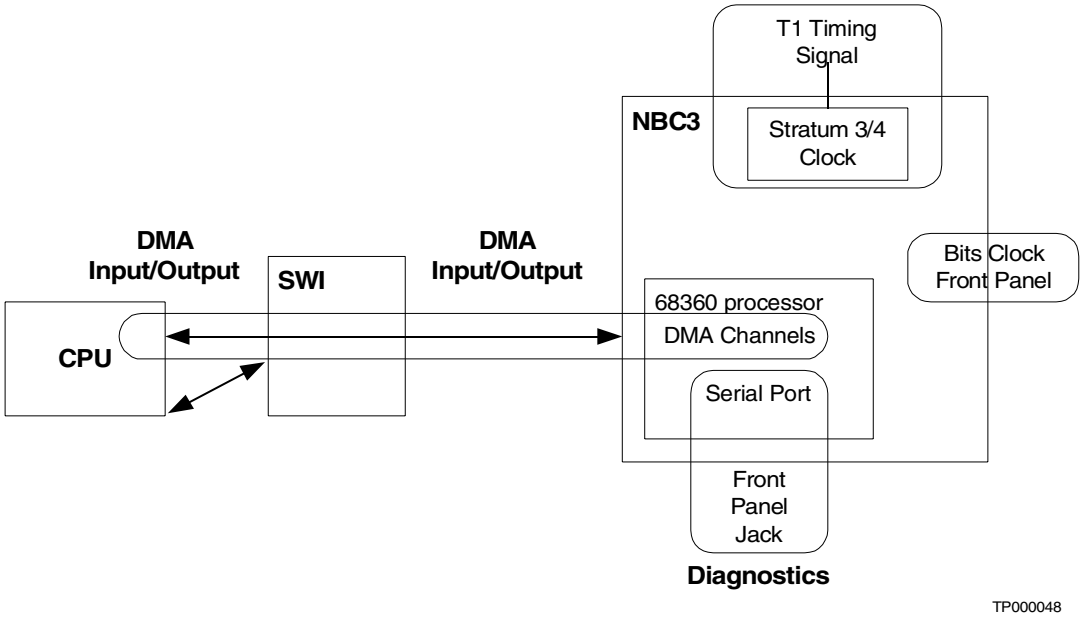


Figure 1: Block Diagram of NBC3 Card

3.1 COMMUNICATIONS BUS

As the master of the Comm Bus, the NBC3 performs the following communication functions:

- Communicates with other boards on the backplane through the Comm Bus.
- Initiates all data transfers on the Comm Bus.
- Sends messages to just one card or broadcasts messages to many other cards (except a redundant NBC3) at the same time.

The Comm Bus is a one byte wide half-duplex interface. This interface facilitates the transfer of messages between the port cards and the NBC3.

3.2 CLOCK SYNCHRONIZATION

The NBC3 includes PLL circuitry that lets you synchronize system clocks from an internal or external source. Internally, the NBC3 generates the timeslot reference quadrature (Stratum 4) clock.

Externally, the NBC3 synchronizes the system with a 64 KHz BITS clock input or with any incoming T1 (1.544 MHz clock) stream or E1 (2.048 MHz clock) stream. It can synchronize to an internal 1.544 MHz Stratum 4 clock.

Table 1 describes the timing synchronization options on the NBC3.

Table 1: System Clock Synchronization Options

Timing Source	Description
A central office 64KHz bipolar BITS clock.	Signal comes from the BITS. The BITS signal supplies DS1 and/or composite clock timing reference to all the other clocks in the central office. Synchronizes the system to the network. Input is through a DB-9 connector on the NBC3 card front panel[1].
A 1.544MHz internal clock reference that synchronizes the pulse code modulation (PCM) bus on T1/E1data streams. This source does not synchronize the system to the network; it provides a clock source that is Stratum 4 compliant. This clock is normally used for short periods of time (a day or less) when the network timing signal is lost for stand-alone switch operation.	Stratum-4 Clock Oscillator on card has a 20 year accuracy rating of ±25 ppm (parts per million). Oscillator meets the requirements for Stratum 4.
An incoming T1, E1, or PRI facility that gets its timing from a network timing source.	Timing is sourced from an incoming T1 stream. Input is through a backplane connection.

[1] A BITS clock cable kit is available that routes the BITS signals to the rear of the VCO/4K chassis. This allows easy access for external cabling.

The BITS clock signals at the DB-9 (J8) connector on the face of the NBC-3 card (and on the optional BITS clock rear conector) are listed in Table 2.

If the NBC3 is the last destination of the BITS clock signal, install a jumper at JP3 (Rev E0xR boards) or JP7 (Rev C0xR boards) to terminate the clock signal.

Table 2: BITS Clock Connector Pinouts

Signal	Pin
Bipolar, Twisted pair	2
	3

3.3 SWI INTERFACE

The NBC3 communicates with the control circuit cards through a 16-bit, DMA-controlled, bi-directional data bus between the NBC3 and the SWI card. The NBC3 translates information from control circuit cards into a serial or 8-bit parallel stream.

The interface is connected internally via one of the serial communications controllers within the CPU, which is controlled by the NBC3 application. The input channel transfers data from the control circuit cards to the NBC3. The output channel transfers data from the NBC3 to the control circuit cards.

Data is transferred to and from the NBC3 memory by the DMA controllers on the SWI that are directionally dedicated.

3.3.1 Control Circuit Cards To NBC3 Messaging

The NBC3 receives command messages from the control circuit cards through the two SWI DMA channels. Received messages are placed into one of the receive buffers on the NBC3. Individual messages are extracted from the receive buffer(s) and placed in the appropriate card output buffer. There is an output buffer for each of the cards in the system.

The NBC3 sends messages to the control circuit cards through the SWI DMA channels. Messages are received from the cards during the card polling cycle, aggregated in one of NBC3 transmit buffers, and when the buffer is full, sends the messages to the control circuit cards.

3.3.2 Control Circuit Cards To NBC3 Timeslot Base Address Information

The timeslot address information stream shares the path on the SWI to the NBC3 with the normal messaging. The NBC3 receives the information from the control circuit cards, after which the information is translated into serial or parallel data. The data is then sent to the cards equipped to receive and interpret translated information through either the high speed serial interface or the Comm Bus on the backplane. Other cards receive path setup commands as part of the messages from the control circuit cards through the NBC3.

3.4 EXTERNAL INTERFACES

Table 3 lists the external interfaces for the NBC3 cards.

Table 3: NBC3 External Interfaces

Connections	VCO/4K
NBC3 to SWI	NBC3 and Combined Controller Assembly are connected to the six-slot midplane on the rear of the system backplane.
BITS Clock	DB-9 connection on NBC3 card front panel[1]
Debugging	RS-232 connection on the NBC3 front panel. This is not for customer use.

[1] A BITS clock cable kit is available that routes the BITS signals to the rear of the VCO/4K chassis.

Figure 2 shows the NBC3 interconnections for VCO/4K systems.

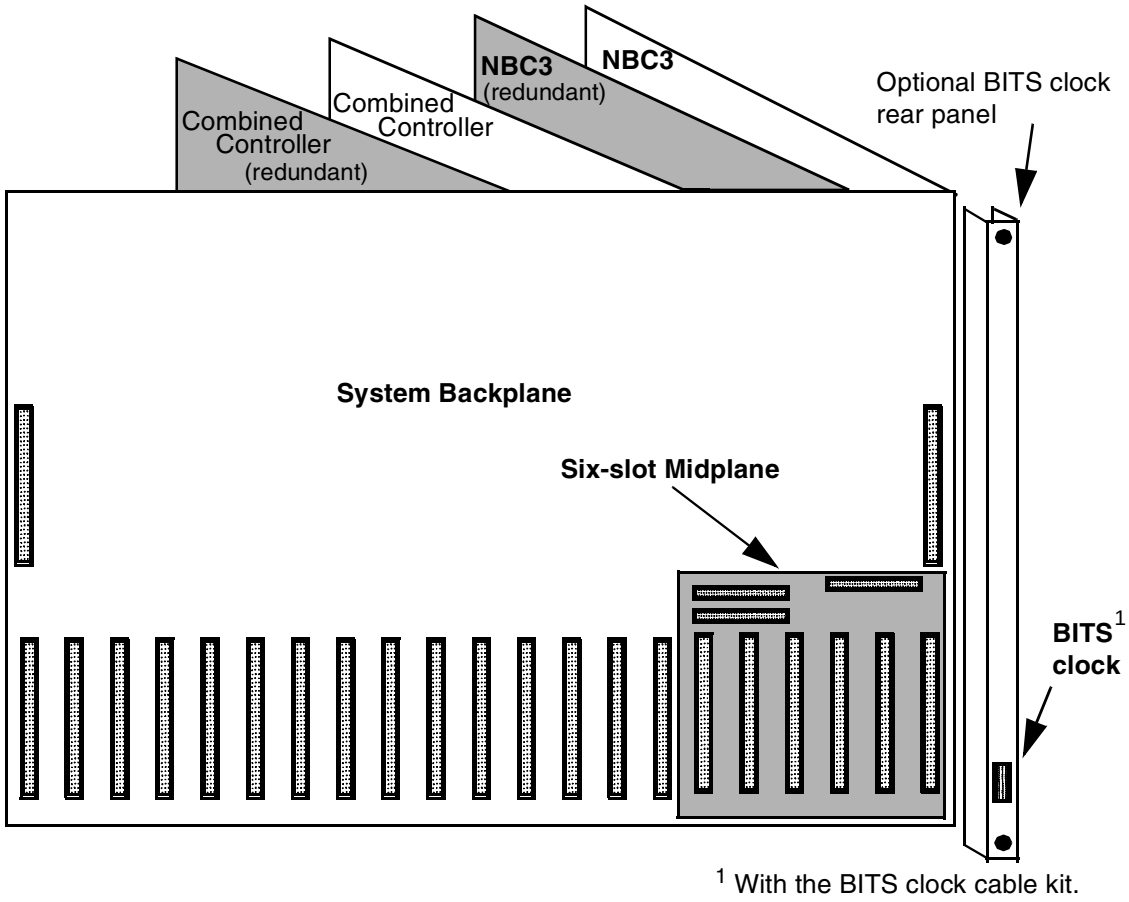


Figure 2: NBC3 Card Interconnections for VCO/4K Systems

3.5 NBC3 STATUS LEDS

The NBC3 card has seven status LEDs on the front panel, as shown in Figure 3. (The DTG-2 Presence LED is ON when a DTG-2 mezzanine card is installed on the NBC3 card.)

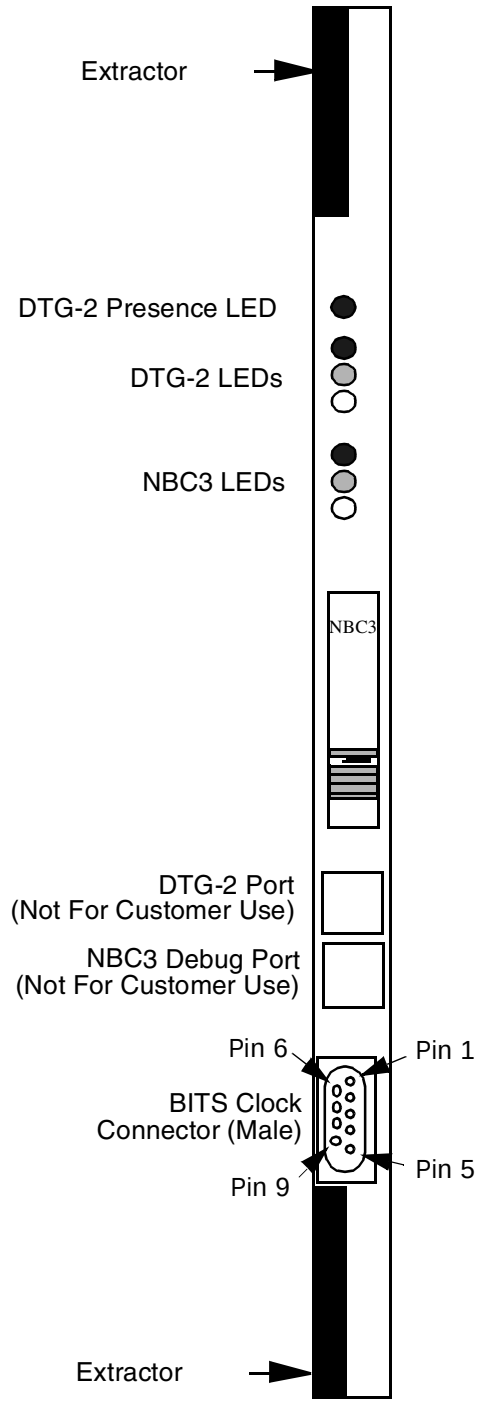


Figure 3: NBC3 Card Front Panel

Table 4 lists the LED display for the DTG-2 mezzanine card.

Table 4: DTG-2 Mezzanine Card LED Display

Card Status	Green	Yellow	Red
Major DTG-2 card failure	OFF	OFF	**ON**
Minor DTG-2 card failure	OFF	**ON**	OFF
DTG-2 card is in standby or diagnostic mode or out of service	**ON**	OFF	OFF

Refer to the *Digital Tone Generator 2 (DTG-2) Technical Description* for detailed information regarding DTG-2 operations.

Table 5 lists the LED display for the NBC3 card.

Table 5: NBC3 LED Display

Card Status	Green	Yellow	Red
Card plugged in (not initiated)	**ON**	**ON**	**ON**
Card initializing/self testing	**ON**	Blinking	OFF
Card receiving download	Blinking	OFF	OFF
OOS/Admin menu/standby/ maintenance/diagnostics/remote	**ON**	OFF	OFF
Card operational/active	OFF	OFF	OFF
Major alarm (seeTable 6 for details)	OFF	OFF	**ON**
Minor alarm (seeTable 6 for details)	OFF	**ON**	OFF
Self test failure *or* stop processing/ card failure *or* register dump	**ON**	OFF	**ON**

Table 6 lists the conditions that cause a major or minor alarm in the NBC3.

Table 6: NBC3 Minor and Major Alarms

Major Alarm	Minor Alarm
Loss of synchronization timing	Unable to communicate due to NBC3 or control circuit cards failure
Communications failure	Cannot obtain 32M lock
Receive buffer overrun encountered	Cannot obtain 3M lock
Transmit buffer overrun encountered	Receive buffer overrun pending
Comm Bus failure	Transmit buffer overrun pending

3.6 CONNECTOR J1 PIN ASSIGNMENTS

Table 7 lists the J1 pin assignments on the NBC3 card. J2 and J3 pin assignments are proprietary and, therefore, are not documented for customer use.

Table 7: NBC3 J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24 V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog (-15V)	Unused	Analog (-15V)
19	Analog (-15V)	Unused	Analog (-15V)
20	Analog (+15V)	Unused	Analog (+15V)

Table 7: NBC3 J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
21	Analog (+15V)	Unused	Analog (+15V)
22	Card Address Bit 1	Unused	Card Address Bit 0
23	Card Address Bit 3	Unused	Card AddressBit 2
24	Card Address Bit 5	Unused	Card Address Bit 4
25	Card Address Bit 7	Unused	Card Address Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

4.0 CONFIGURATION NOTES

The NBC3 card is manufactured by Cisco Systems, Inc. and includes firmware in the form of a PROM. All NBC3 jumpers except for the JP3 (Rev E) are factory set. If the NBC3 is the last destination of the composite clock signal, install a jumper at the J7/JP3 location to terminate the clock signal.

Figure 4 shows the location of the firmware PROM and the JP3 on the NBC3 Rev E card.

CAUTION: Removing or repositioning the jumpers on an NBC3 card may cause system failures and damage to the card. Always verify that the jumpers are in their proper positions before installing or replacing an NBC3 card in the system.

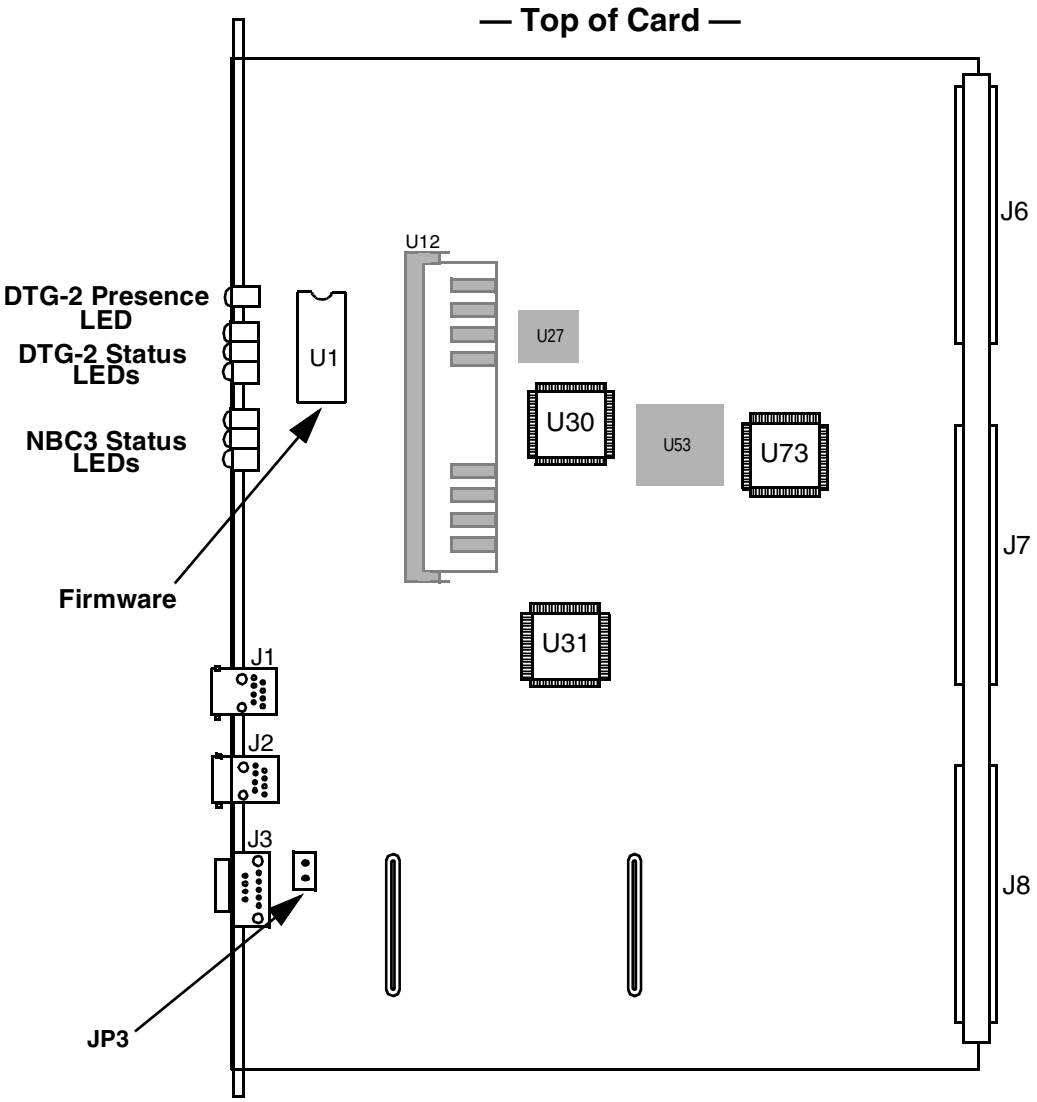


Figure 4: NBC3 (Rev E) JP3 and Firmware Location

Note: For Rev C cards the jumper is located at JP7, not JP3.

5.0 NBC3 CARD POPULATION RULES

The following card population rules apply to the NBC3:

- In non-redundant VCO/4K systems, the NBC3 must reside in slot 1 of the card rack.
- In redundant VCO/4K systems, the NBC3s must reside in slots 1 and 2 of the card rack.

6.0 REMOVAL/REPLACEMENT PROCEDURES

This subsection describe how to remove and replace the NBC3 card. The NBC3 card can be removed and inserted while the system is powered on.

CAUTION: Do not pull the active side NBC3 on an operating production switch. Pulling an active NBC3 can generate errors and impact traffic. If you suspect a problem with an NBC3 card and you wish to remove it, first switch sides to make it the standby side.

Observe antistatic precautions whenever handling the NBC3 to avoid damage to sensitive CMOS devices. Wear a ground strap connected to the system's equipment frame.

6.1 REMOVAL PROCEDURES

Perform the following steps to remove an NBC3:

1. If you have a redundant system, verify that the NBC3 you want to remove is in the standby side. If the card is not in the standby side, run the Switch Active Side to Standby Utility as described in the *VCO/4K System Administrator's Guide* .

   If the utility does not switch the system over, flip the **SELECT** toggle on the AAC to force the system to switch over. (Refer to the *Alarm Arbiter Card (AAC) Technical Description* or *Alarm Arbiter Card (AAC) With Alarm Interface Card (AIC) Technical Description* for more information.)
2. If you have a redundant system and the NBC3 has a DTG-2 mezzanine card, verify that the DTG-2 is in standby mode and take the DTG-2 card out of service.
3. If you have a non-redundant system, shut down the system. If you have a redundant system, shut down the standby side.
4. Use a #1 Phillips-head screwdriver to remove the mounting screws/washers from the top and bottom PCB card retainer bars (see Figure 5) on the system. Keep the retainers and screws together in a safe place for replacement later.

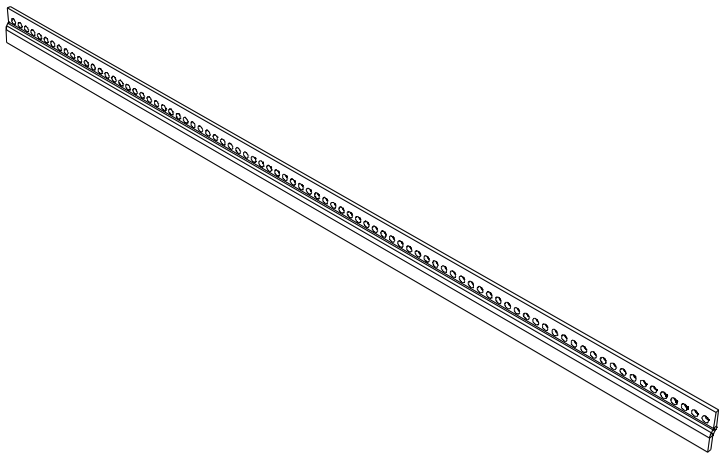


Figure 5: PCB Card Retainer Bar

5. Disable the external alarm system to which the AAC might be connected.
6. Disconnect all cables that are attached to the card (for example, BITS clock cable.)
7. Use your thumbs to pull the upper and lower extractors away from the card front panel. This action extracts the card from the backplane connectors.
8. Pull the NBC3 free of the card slot.
9. After you remove the card from the system, place it on an antistatic mat or envelope.

6.2 REPLACEMENT PROCEDURES

To replace an NBC3, perform the following steps:

1. Place the replacement NBC3 card next to the removed card on the antistatic mat or antistatic envelope.
2. Refer to your release notes and verify that the revision levels of the PROMs match the requirements of the generic software currently loaded in the system.
3. Verify that the switch and jumper settings on the replacement NBC3 are the same as those on the removed card.
4. Grasp the replacement NBC3 by the top handle and the bottom edge and align it with the top and bottom card guides of the subrack.
5. Make sure the extractor levers are perpendicular to the front panel. Push the NBC3 in until it makes contact with the master port subrack backplane. The hooks on the extractors must be behind the front rail of the subrack. Use your thumbs to push the extractors toward the front panel.
6. If you are using the BITS clock option, reconnect the clock source to the DB-9 connector on the NBC3 front panel.
7. Enable the external alarm system connected to the AAC terminals.
8. If you have a non-redundant system, reboot the system. If you have a redundant system, reboot the standby side. (Refer to the *VCO/4K System Maintenance Manual* for more information.)
9. If you have a redundant system, flip the SELECT toggle switch on the ACC to the AUTO position.
10. The DTG-2 is automatically brought into service when the NBC3 is downloaded. If the DTG-2 card fails to automatically come into service, change the card status to active from the master console Card Maintenance menu. (Refer to the *VCO/4K System Administrator's Guide* for more information.)
11. Reinstall the top and bottom PCB card retainer bars (see Figure 5). Use a #1 Phillips-head screwdriver to replace the mounting screws/washers (five per bar).

CAUTION: The PCB card retainer bars must be installed for the system to meet NEBS Zone 4 Earthquake compliance.

7.0 TROUBLESHOOTING

Since problems with the NBC3 critically affect system operation, the generic software provides numerous system error messages describing what type of NBC3 fault is detected. These error messages are fully described in the *System Administrator's Guide.*

A special set of messages which identify problems with T1 and NBC3 synchronization is also provided in the *System Administrator's Guide.*

7.1 TROUBLESHOOTING PROCEDURES FOR NON-REDUNDANT SYSTEMS

When an NBC3 major alarm occurs in a non-redundant system, the AAC initiates a system reset. The CPU is cleared of all current data and all calls in progress are dropped. Service disruption lasts until the entire reset process is complete.

If the system reset fails to restore NBC3 operation on VCO/4K systems, replace the NBC3 card. See *Section 6.2* for replacement procedures.

7.2 TROUBLESHOOTING PROCEDURES FOR REDUNDANT SYSTEMS

Verify that the system switched over so that the malfunctioning NBC3 is on the standby side. If the system did not switch over, flip the SELECT toggle on the AAC to force the system to switch over. (Refer to the *Alarm Arbiter Card (AAC) Technical Description* or *Alarm Arbiter Card (AAC) With Alarm Interface Card (AIC) Technical Description* for more information.)

On VCO/4K systems, if the reset fails to restore NBC3 operation, replace the NBC3 card. See *Section 6.2* for replacement procedures.

8.0 RELATED DOCUMENTS

For additional information on the NBC3 card in VCO/4K systems, refer to the following publications:

- VCO/4K Hardware Planning Guide
- VCO/4K System Administrator's Guide
- VCO/4K System Maintenance Manual
- Combined Controller Assembly Technical Description
- VCO/4K Alarm Arbiter Card (AAC) With Alarm Interface Card (AIC) Technical Description

Direct Inward Dial Card (DID-2)

1.0 GENERAL

The Direct Inward Dial (DID-2) card is a standard system port interface circuit card that resides in the Master or any Expansion Port Subrack. The DID-2 card provides interface to eight terminating 2-wire connections with battery reversal on seizure, each with a dedicated DTMF receiver and dial pulse detection;. The DID-2 card supplies office battery. Tip and Ring leads are fused and surge protected.

2.0 SPECIFICATIONS

Microprocessor: 8031 (12 MHz)

Memory: 8K Bytes EPROM
2K Bytes RAM

Power Requirements:

	Typical	Maximum
+5 Volts:	500 mA	900mA
+15 Volts:	120 mA	210mA
–15 Volts:	125 mA	230mA
+24 Volts:	25 mA	29mA*
–48 Volts:	35 mA	60mA

** per-port current requirements*

Trunk Specifications

Input Level:	0 dB ± 0.5 dBm
Output Level:	-3 dB ± 0.5 dBm
Crosstalk Attenuation:	68 dB minimum
Idle Circuit Noise:	23 dBrnc maximum
Line Impedance:	600 ohms ± 10%
Echo Return Loss:	18 dB minimum (-2 dBm input)

Singing Return Loss:

Low (200 - 500Hz)	12 dB minimum
High (2500 - 3200Hz)	15 dB minimum

Frequency Response:

(Signal levels relative to 1004 Hz with C Message Filter)

60 Hz:	-20 dB maximum
300 Hz:	-3.0 to 1.0 dB
600 to 2400 Hz:	-1.0 to 1.0 dB
3200 Hz:	-3.0 to 1.0 dB

Longitudinal Balance:

200–1000 Hz	60 dB minimum
1000–4000 Hz	50 dB minimum

Loop Current: 20 mA minimum
60 mA maximum

DTMF Receiver:

Detectable input level	-25 dBm minimum
	1 dBm maximum
Acceptable twist	10 dB maximum
Tone or quiet duration	40 mS minimum

CAUTION: This version of the DID-2 card may be used interchangeably in listed (UL 1459) and non-listed systems. However, earlier versions of the DID card (P/N 50174060200 or 50174060200) cannot be used in listed systems.

2.1 ANSWER SUPERVISION

Allowing this equipment to be operated in such a manner as to not provide proper answer supervision signalling is in violation of FCC Part 68 rules. This equipment returns answer supervision signals to the Public Switched Telephone Network when:

- answered by the called station
- answered by the attendant
- routed to a recorded announcement that can be administered by the CPE user
- routed to a dial prompt

This equipment returns answer supervision on all DID calls forwarded back to the Public Switched Telephone Network. Permissible exceptions are:

- the call is unanswered
- a busy tone is received
- a reorder tone is received

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the DID-2. The five major elements of the DID-2 card are:

- Per Port Circuitry
- PCM Time Slot Bus Interface
- Packet Processor
- Control & Status Registers
- Protective Devices

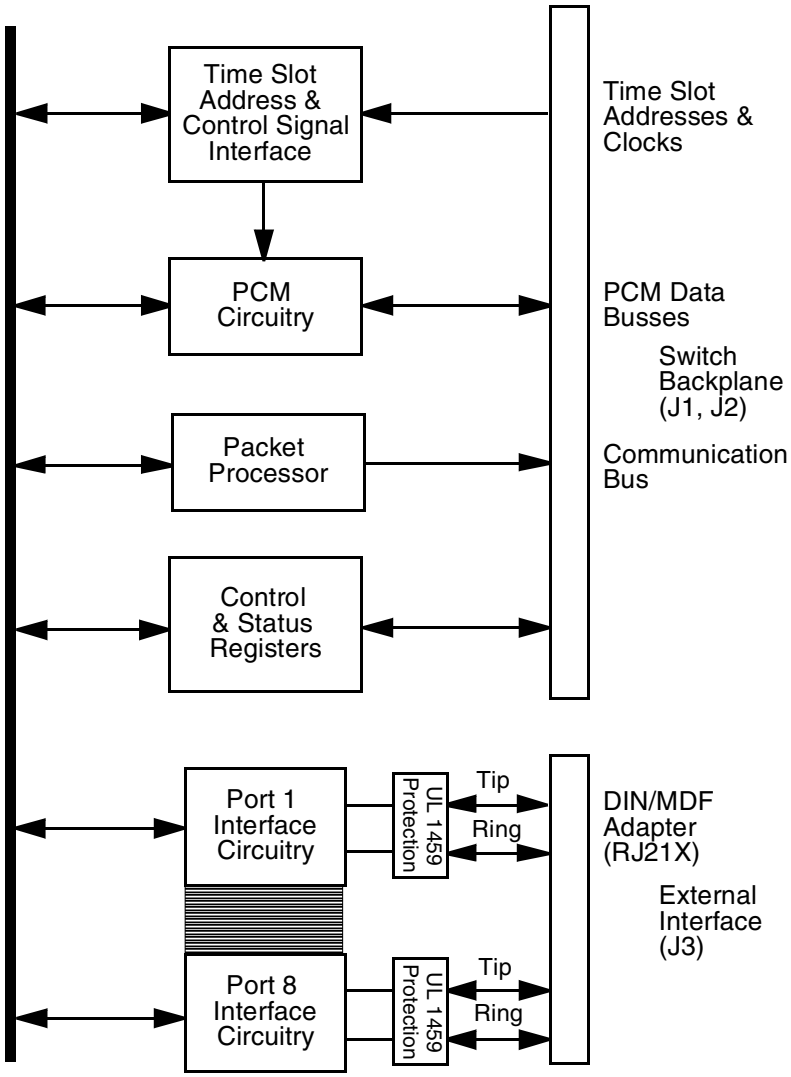


Figure 1: Block Diagram Of DID-2 Card

3.1 PER PORT CIRCUITRY

Each of the eight ports on a DID-2 card includes the following:

- DTMF digit receiver
- Analog to digital encoding and decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On/Off hook detection
- Relay to reverse tip and ring
- Tip and ring lead fuses
- Surge protection across rip and ring leads.

3.1.1 DTMF DIGIT RECEIVER

A DTMF digit receiver integrated circuit (I.C.) is provided for each DID-2 port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

3.1.2 ANALOG TO DIGITAL ENCODING & DECODING

A 2913 codec provides digital-to-analog and analog-to-digital signal conversion. A codec semi-custom interface I.C. performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between itself and the codec.

Data received from both PCM busses is latched into parallel in/serial out shift registers internal to the codec interface I.C. The codec semi-custom interface I.C. supplies the data by selecting the output of one of the two internal parallel-to-serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode/decode A-law or µ-law PCM data. Two jumper areas on the DID-2 card allow selection of the clock frequency and PCM encoding rule for all eight codecs.

3.1.3 ANALOG INTERFACE

The analog interface consists of the circuitry from the tip and ring leads to the codec. An AMSþ2006 Subscriber Line Interface Circuit Hybrid performs the 2-wire to 4-wire conversion, provides internal lightning protection, and drives battery onto the tip and ring leads. The hybrid also monitors the current on the tip and ring leads to determine port on/off hook status, and outputs an on/off hook status bit. When a port is not terminated (on hook), the balance network is unbalanced. When this condition exists, an analog signal driven from the codec's receive amplifier into the hybrid is driven back to the input of the codec's transmit amplifier.

A DTMF digit receiver I.C. is connected to the analog signal output by the hybrid and input by the codec's transmit amplifier. A 3.5795 MHz crystal oscillator is provided to generate the clock signal required by the DTMF digit receivers.

3.1.4 CONTROL RELAY

A relay is provided for each DID-2 port. When energized by host command, the relay contacts reverse the tip and ring leads between the 2-wire/4-wire hybrid and the J3 connector. The relay is disabled when a line goes offhook.

3.1.5 TIP & RING PROTECTIVE DEVICES

Tip and Ring leads of the eight circuits on the DID-2 are protected from overvoltage and overload conditions as shown in Figure 2 below.

The SIDACtor™ on each port provides transient surge protection from lightning, line transients and other damaging voltage spikes. This single package device protects against Tip to Ring, Tip to Ground, and Ring to Ground transients. When the monitored voltage exceeds 235Vac, the SIDACtor switches on through a negative resistance region to a low on-state voltage in nanoseconds. It continues to conduct until the current is interrupted or drops below the minimum holding current of the device.

The 2AG Slo-Blo fuses are soldered into the circuit board and are not field replaceable. If a fuse blows, contact Cisco Systems Technical Support to arrange for repair.

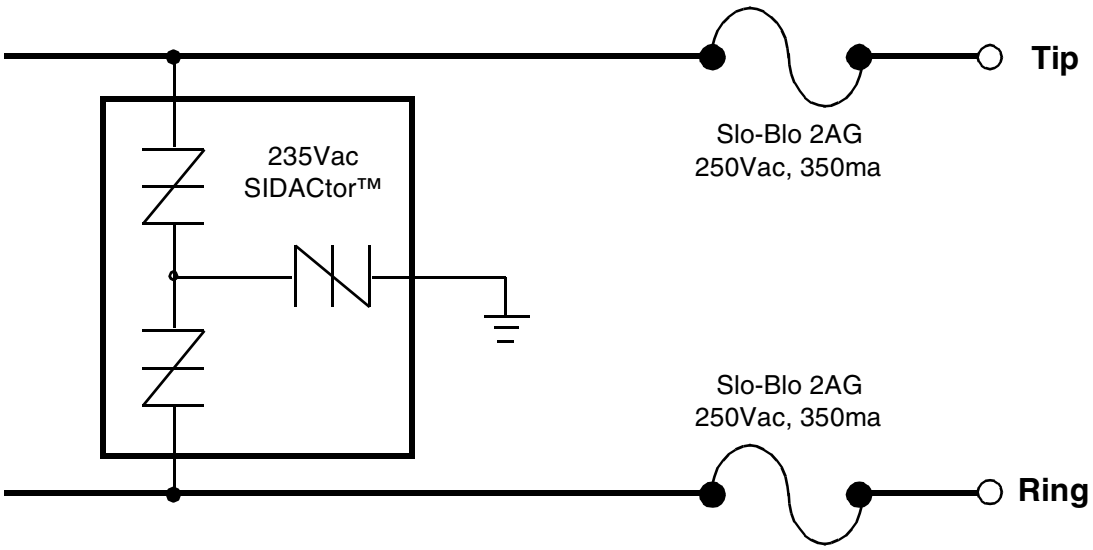


Figure 2: Schematic Diagram Of Tip & Ring Protective Devices

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within a system is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the DID-2 card translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The DID-2 card interfaces to the dual PCM time slot busses with bus interface circuitry common to several system port-oriented circuit cards. Each of the eight port interfaces on the DID-2 card can "listen to" any time slot on either PCM data bus.

A DID-2 card is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular DID-2 card port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The DID-2 card contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC). The Packet Processor polls each of the eight line/trunk connections looking for an event (i.e. off hook detection or valid DTMF digit reception). When polled by the NBC, the Packet Processor reports any status change. The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the DID-2 card.

The Communication Bus is the path by which the Packet Processor receives commands from and sends status to the Network Bus Controller.

3.4 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the DID-2 card.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.5 EXTERNAL INTERFACES

The connections to the Tip and Ring leads of the eight line/trunk interfaces on the DID-2 card are made via the J3 connector. A DIN to I/O Module attaches to J3 and terminates the tip/ring connections of up to three DID-2s to a standard RJ21X, 25-pair connector. It is expected that dry line/trunk connections be made via the RJ21X connector to the tip and ring leads of the individual lines/trunks (DID-2 card provides battery). The J3 pin assignments for each DID-2 card are provided as Table 2. J3 to RJ21X pinouts are shown in Table 3 and Figure 4.

Table 1: DID-2 Card J-1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0

Table 1: DID-2 Card J-1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID-2	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: DID-2 Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Unused
2	Trunk 1 – Tip	Unused	Trunk 1 – Ring
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – Tip	Unused	Trunk 2 – Ring
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – Tip	Unused	Trunk 3 – Ring
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Trunk 4 – Tip	Unused	Trunk 4 – Ring
15	Unused	Unused	Unused

Table 2: DID-2 Card J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – Tip	Unused	Trunk 5 – Ring
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – Tip	Unused	Trunk 6 – Ring
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Trunk 7 – Tip	Unused	Trunk 7 – Ring
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – Tip	Unused	Trunk 8 – Ring
31	Unused	Unused	Unused
32	Unused	Unused	Unused

Table 3: J3 to RJ21X Pinouts

Card	Trunk	Tip Lead			Ring Lead		
1	1	J3-2A	to	RJ21X-26	J3-2C	to	RJ21X-1
1	2	J3-6A	to	RJ21X-27	J3-6C	to	RJ21X-2
1	3	J3-10A	to	RJ21X-28	J3-10C	to	RJ21X-3
1	4	J3-14A	to	RJ21X-29	J3-14C	to	RJ21X-4
1	5	J3-18A	to	RJ21X-30	J3-18C	to	RJ21X-5
1	6	J3-22A	to	RJ21X-31	J3-22C	to	RJ21X-6
1	7	J3-26A	to	RJ21X-32	J3-26C	to	RJ21X-7
1	8	J3-30A	to	RJ21X-33	J3-30C	to	RJ21X-8
2	1	J3-2A	to	RJ21X-34	J3-2C	to	RJ21X-9
2	2	J3-6A	to	RJ21X-35	J3-6C	to	RJ21X-10
2	3	J3-10A	to	RJ21X-36	J3-10C	to	RJ21X-11
2	4	J3-14A	to	RJ21X-37	J3-14C	to	RJ21X-12
2	5	J3-18A	to	RJ21X-38	J3-18C	to	RJ21X-13
2	6	J3-22A	to	RJ21X-39	J3-22C	to	RJ21X-14
2	7	J3-26A	to	RJ21X-40	J3-26C	to	RJ21X-15
2	8	J3-30A	to	RJ21X-41	J3-30C	to	RJ21X-16
3	1	J3-2A	to	RJ21X-42	J3-2C	to	RJ21X-17
3	2	J3-6A	to	RJ21X-43	J3-6C	to	RJ21X-18
3	3	J3-10A	to	RJ21X-44	J3-10C	to	RJ21X-19
3	4	J3-14A	to	RJ21X-45	J3-14C	to	RJ21X-20
3	5	J3-18A	to	RJ21X-46	J3-18C	to	RJ21X-21
3	6	J3-22A	to	RJ21X-47	J3-22C	to	RJ21X-22
3	7	J3-26A	to	RJ21X-48	J3-26C	to	RJ21X-23
3	8	J3-30A	to	RJ21X-49	J3-30C	to	RJ21X-24

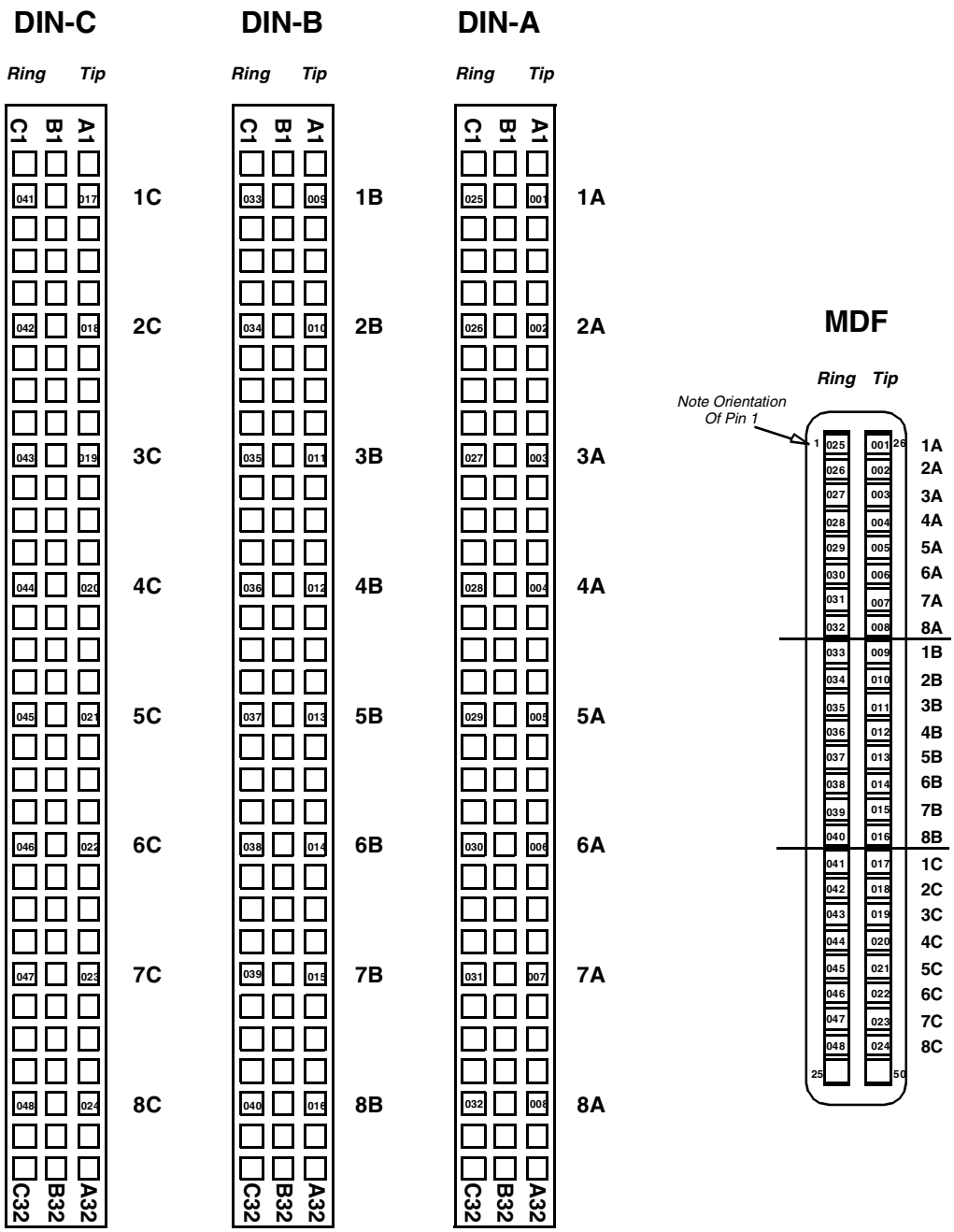


Figure 3: Pin-Out Diagram Of DIN–RJ21X MDF Adapter

4.0 CONFIGURATION NOTES

The DID-2 card is manufactured by Cisco Systems, Inc. Jumper plugs on the DID-2 card are factory set for use in systems. Figure 5 indicates the location and correct installation of jumper plugs on a DID-2 card based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it in a Port Subrack.

> *NOTE: The artwork revision level for the PCB itself (unpopulated) is etched on the solder side of the board near the front panel. The circuit card assembly part number, revision level and serial number appear on the component side of the PCB near the card front panel. The assembly part number includes four characters indicating the revision level. The first three characters are the actual revision level. The final letter "R" indicates that the PCB is at Release level. For example, a revision level A0L card is marked as Rev. "A0LR".*

If a card is improperly configured, it may fail to perform its interface function between external lines/trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a DID-2 card in the system data base, refer to the *VCO/4K System Administrator's Guide.*

Class of Service (COS) also greatly affects operation of the card. A COS of "T" or "2" sees inward seizures as call originations If calls are not being properly processed, check the COS. NOTE: Because of differences in firmware, a DID-2 card cannot be converted to a SLIC by reconfiguring jumper settings. Nor can individual ports be set for DID-2 or SLIC operation.

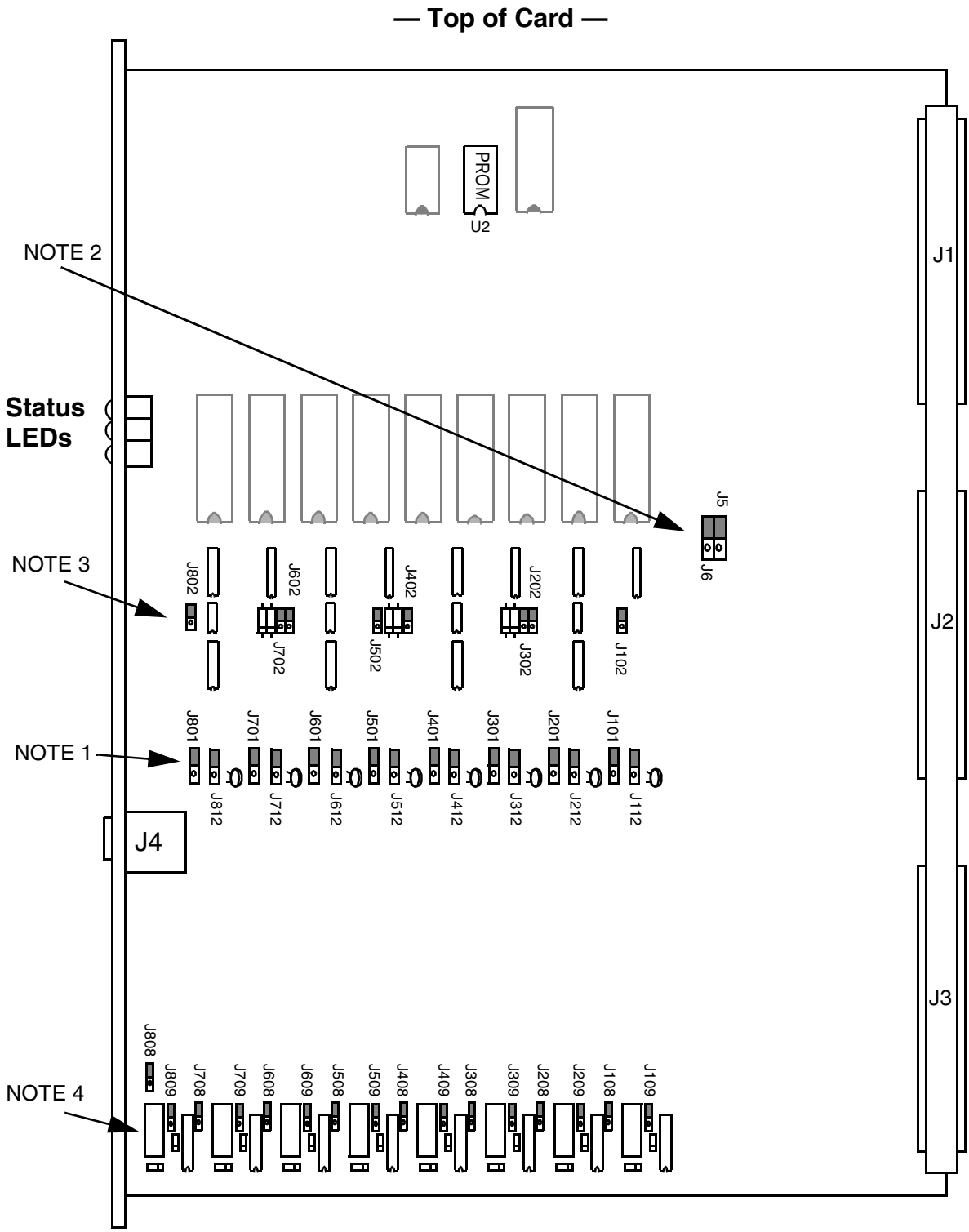


Figure 4: DID-2 card Jumper & PROM Locations

4.0.1 JUMPER LOCATIONS

NOTE 1

- Jumpers at J101 through J801 must be set to "-3" for -3dB gain on circuit transmit signal (8þjumpers).
- Jumpers at J112 through J812 must be set to "DID" for DID-2 operation (8þjumpers).

NOTE 2

- Install jumper plug at J5 in the "U" position for codec µlaw operation (North American standard).
- Install jumper plug at J5 in the "A" position for codec A-law operation (European standard). Position "U" (µlaw) is the factory default setting for J5.
- Install the jumper plug at J6 in the "1.5" position for 1.544MHz codec clock (North American standard).
- Install the jumper plug at J6 in the "2.0" position for 2.048MHz codec clock (European standard). Position "1.5" (1.544MHz) is the factory default setting for J6.

NOTE 3

- Jumpers at J102 through J802 must be set to "D" position for DID-2 operation (8þjumpers).

NOTE 4

- Jumpers at J108 through J808 and J109 through J809 must be set to "DID" position for DID-2 operation (2 X 8 =16 jumpers).

PROM

The 2764 PROM in location U2 contains firmware appropriate to DID-2 card signalling interface requirements.

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the DID-2 card, refer to the following publications:

5.1 VCO DOCUMENTATION

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K System Maintenance Manual
- VCO/4K Technical Descriptions: Plug-In MDF Adapters

Drop and Insert Card (D+I)

1.0 GENERAL

The Drop and Insert (D+I) card provides DS0 transmission-only access to the VCO/4K system. It supports a maximum of eight interfaces per card, synchronous operation at either 56 KB or 64 KB. The D+I card is configurable as DCE or DTE with normal or reverse bit-packing, and supports both RS-449 and V.35 signal specifications for dates and clock leads only. The D+I card can be inserted into the system while the system is active.

Administration of the card is done through the existing System Administration console. Configuration messages are sent to the card from the Generic through the NBC/NBC-3 interface.

2.0 SPECIFICATIONS

Microprocessor:	68360 (25MHz)
Memory:	4 MBytes DRAM 256 KBytes EPROM
Power Requirements:	+5 Volts4 amps –15 Volts0.5 amp
I/O Port Specifications:	
Input Level:	RS449 or V.35 (date and clock only)
Output Level:	RS449 or V.35 (date and clock only)

NOTE: The DB9 to DB37 cable for DCE operation can be ordered from Cisco Systems.

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the D+I card. The major elements of the card are:

- Mitel switch
- Core Processor
- PCM Interface
- Communications Bus (comm bus) Interface
- Port Interface

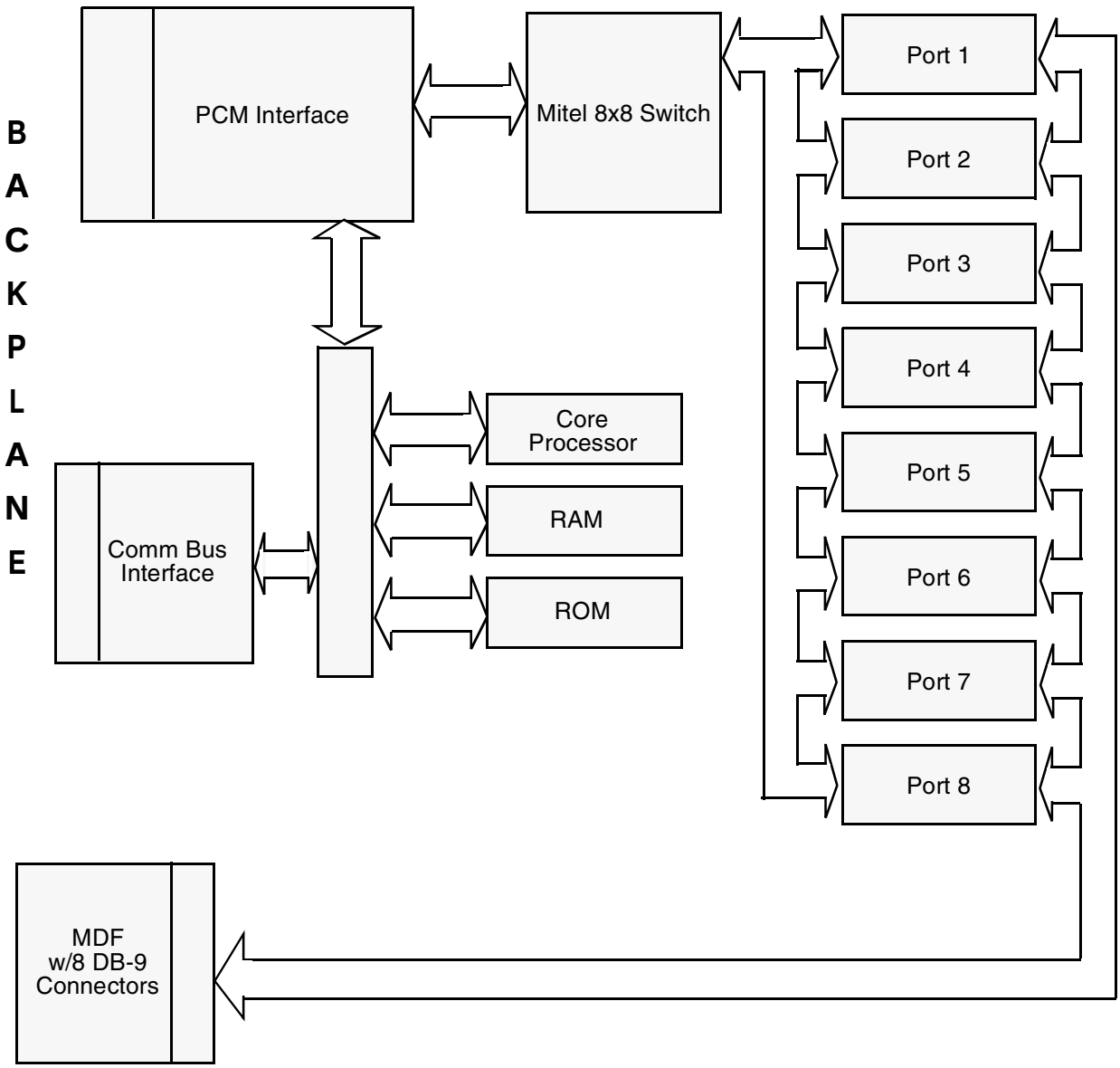


Figure 1: Block Diagram of the D+I Card

The core processor controls the eight synchronous serial links and communicates to the Network Bus Controller (NBC-3) via the comm bus. The comm bus interface handshakes all signals with the NBC-3, and moves data to and from memory through dedicated DMA channels present on the core CPU.

3.1 MITEL SWITCH

Each D+I port is connected to the Mitel 8985 voice/data switch. The Mitel Switch switches data packets between multiple serial PCM highways generated within the PCM interface.

3.2 CORE PROCESSOR

The core processor is a Motorola MC68360, a highly integrated microprocessor that can implement most of the core processor requirements through on-chip peripherals. The 68360 operates at 25MHz.

The core processor has an RS232 port that is accessible from the face plate via an RJ45 jack. The electrical signals are +12V and -12V (RS232).

3.3 PCM BUS

The VCO/4K uses the PCM bus to move voice and data traffic between port cards. The NBC/NBC-3 supplies clocking.

The PCM interface controls the following:

- independent dynamic time slot assignment for transmit and receive matrices
- full utilization of PCM buses A and B for a total of 1776 available time slots maximum.

3.4 COMM BUS INTERFACE

The CORE Processor communicates with the NBC/NBC-3 through the comm bus interface, which is implemented with the two DMA channels provided on the MC68360. One channel is dedicated to moving data *off* the comm bus, and one channel is dedicated to placing data *on* the comm bus.

3.5 PORT INTERFACE

The D+I card contains eight synchronous ports that can be individually configured by the system administrator. Since each D+I port interfaces to the VCO/4K, modem control signals are not provided. Only transmit and receive, clock and data signals are provided.

Users may select from the following features and configure the card on a per port basis:

- 56 KBps or 64 KBps
- DCE or DTE
- Bit ordering (normal or reverse)
- Loop back

3.5.1 CLOCK RATE

Each D+I port is capable of operating at either 64 KBits/sec or 56 KBits/sec. The user selects the operating rate through system administration screens. Refer to the *System Administration Guide* for information on the D+I screens.

3.5.2 COMMUNICATION LINK

Each D+I port communicates over either an RS-449 or V.35 link (designed for transmission-only). Refer to Figure 2 for the appropriate wiring for the link.

On the port side, the cable connects via a 9-pin D-sub connector. On the equipment side, the cable connection is customer-supplied and is dependent on the type of link. The cable pin-outs for the D+I in DTE or DCE mode are different. Specific cables are required for each type of link.

If you are cabling the D+I card to Cisco Systems' integrated SS7 system, note that a DB9 to DB37 cable is available from Cisco Systems.

3.5.3 DCE/DTE OPERATION

Each D+I port is individually capable of operating as either a DCE or DTE, as selected by the system administrator. When configured for DCE operation, the port uses the system clock to create the transmit and receive clocks. In DCE mode, the transmit and receive data path is not subject to data slips. This is the preferred configuration.

When configured for DTE operation, the port uses the received clocks to transmit data as well as receive data. Since receive clocks may not be locked to the VCO/4K system clock, the transmit and receive data paths are subject to data slips. In DTE mode, the port may lose its transmit and receive clocks. (Refer to the *System Administration Guide* for information on selecting DCE or DTE operation.)

Each port has a transmit and receive loss of clock (LOC) detector. When a port is in DTE mode and an LOC occurs, or a LOC condition clears, the core processor is informed via an interrupt. When a port is in DCE mode, no LOC events occur.

3.5.4 PIN ASSIGNMENTS

Each port has the following signals:

- Receive clock — INPUT (DTE)/OUTPUT (DCE)
- Receive data —INPUT
- Transmit clock — INPUT (DTE)/OUTPUT (DCE)
- Transmit data — OUTPUT

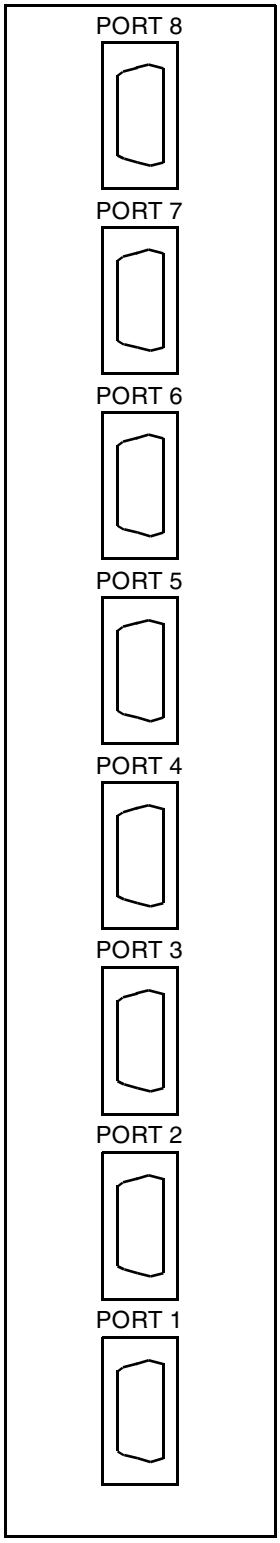
NOTE: The D+I card cannot be used as a system clock reference source.

The D+I port only operates in a synchronous mode and as such, only the Data and Clock signals are provided. All I/O signals exit the board through the J3 connector, and an MDF board provides the interface to 8 DB9 female connectors. The eight female DB9 connectors provide the necessary signals for RS-449/V.35 connection.

The DB9 pinout is shown below.

Ground	Pin 1	GND
Transmit Clock A	Pin 2	TXCLKA
Transmit Clock B	Pin 6	TXCLKB
Transmit Data A	Pin 3	TXDATAA
Transmit Data B	Pin 7	TXDATAB
Receive Clock A	Pin 5	RXCLKA
Receive Clock B	Pin 9	RXCLKB
Receive Data A	Pin 4	RXDATAA
Receive Data B	Pin 8	RXDATAB

Figure 2 illustrates the DB9 pinout.



Customers must supply the cabling from the MDF to their equipment. Note that the cabling is different for DTE and DCE applications.

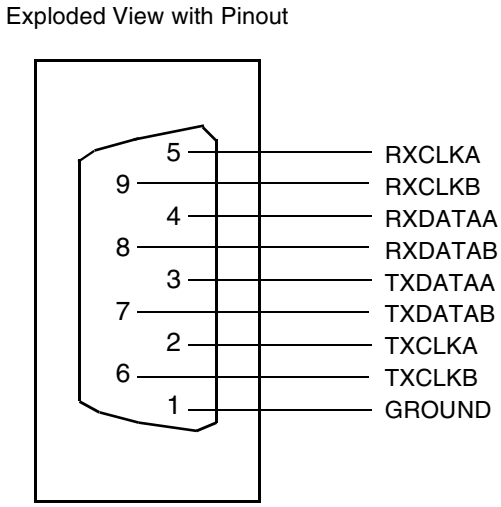


Figure 2: D+I MDF and DB9 Pinout

3.5.5 BIT PACKING ORDER

Users may select normal or reverse bit ordering. The bits may be packed into a PCM byte in normal or reverse order as shown in the table below:

Mode	Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
64 Kbits/ sec Normal	1st bit	2nd bit	3rd bit	4th bit	5th bit	6th bit	7th bit	8th bit
56 Kbits/ sec Normal	1st bit	2nd bit	3rd bit	4th bit	5th bit	6th bit	7th bit	Fixed at 0
64 Kbits/sec Reverse	8th bit	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit
56 Kbits/sec Reverse	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit	Fixed at 0

3.5.6 LOOPBACK MODE

Each D+I port is capable of looping back the data presented at each interface. When you place a port in loopback, the data received at the port is looped back to the port transmit path without going through the FIFOs or slip circuits. Loopback also enables transmit data from the transmit PCM bus to go through the (Mitel) voice/data switch to the port controller EPLD, back through the voice/data switch, to the receive PCM bus.

NOTE: The port EPLD provides all clock selection and synchronization, control of the port side of the FIFOs, error detection, and loopback. All input signals to the EPLD are synchronized with the internal 8Mhz clock so that the state machines are synchronous.

The RX and TX data is sent directly from the port interface, and the incoming and outgoing serial data goes to the shift registers prior to the FIFOs.

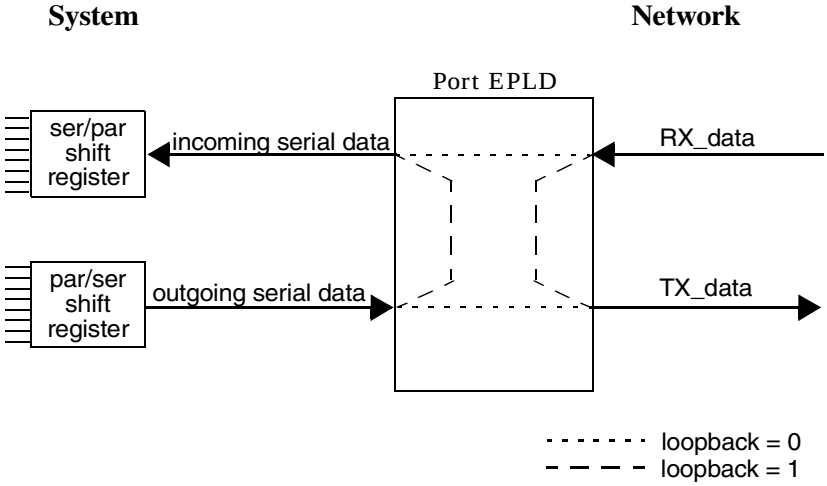


Figure 3: Data Loopback

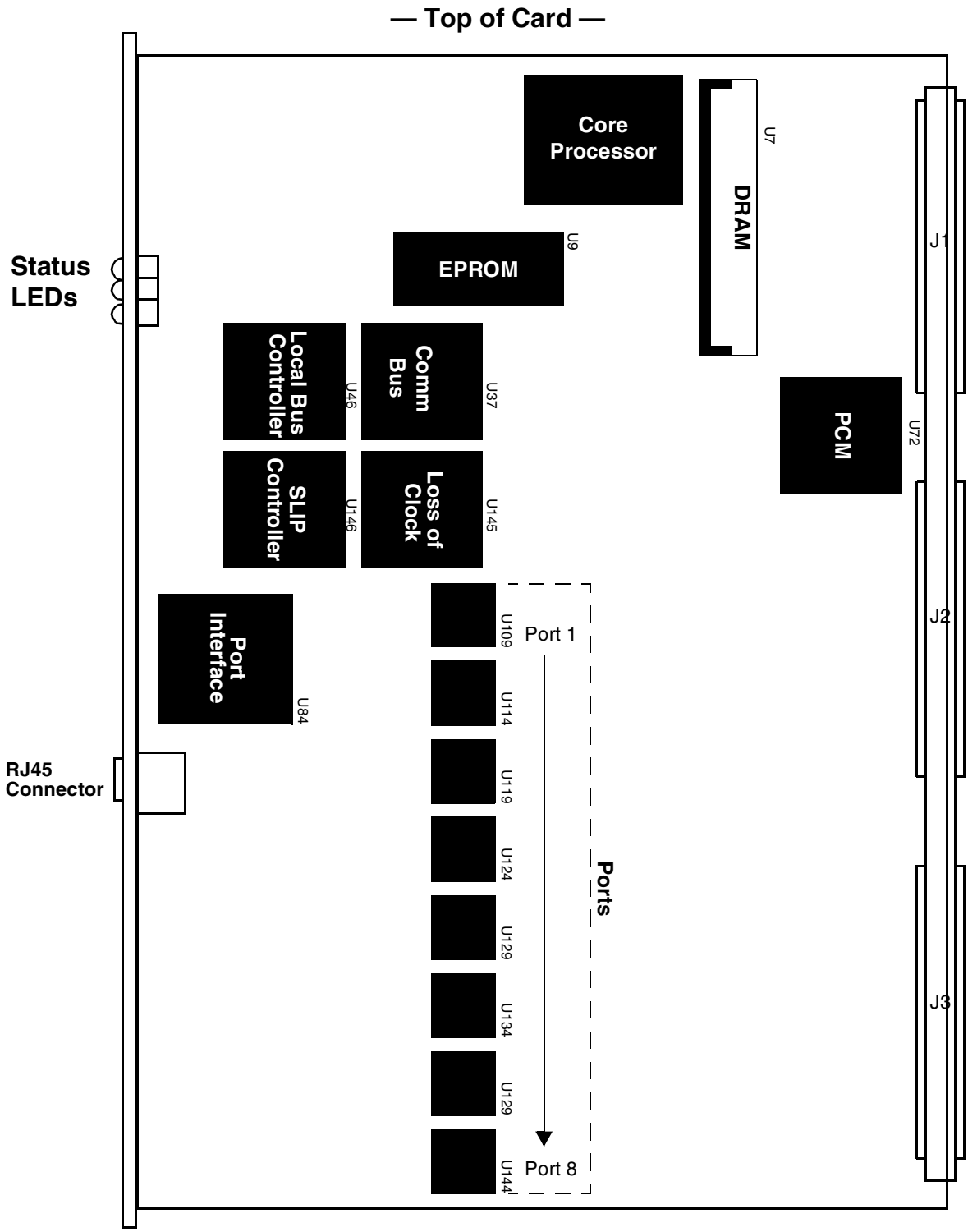


Figure 4: D+I Card

The EPROM on the core processor boots the processor and loads the application in RAM.

Pin	Row A	Row B	Row C
1	RX0CLCA	FRGND	RX0CLKB
2	RX0DATAA	FRGND	RX0DATAB
3	TX0CLKA	GND	TX0CLKB
4	TX0DATAA	GND	TX0DATAB
5	RX1CLKA	GND	RX1CLKB
6	RX1DATAA	GND	RX1DATAB
7	TX1CLKA	GND	TX1CLKB
8	TX1DATAA	GND	TX1DATAB
9	RX2CLKA	GND	RX2CLKB
10	RX2DATAA	GND	RX2DATAB
11	TX2CLKA	GND	TX2CLKB
12	TX2DATAA	GND	TX2DATAB
13	RX3CLKA	GND	RX3CLKB
14	RX3DATAA	GND	RX3DATAB
15	TX3CLKA	GND	TX3CLKB
16	TX3DATAA	GND	TX3DATAB
17	RX4CLKA	GND	RX4CLKB
18	RX4DATAA	GND	RX4DATAB
19	TX4CLKA	GND	TX4CLKB
20	TX4DATAA	GND	TX4DATAB
21	RX5CLKA	GND	RX5CLKB
22	RX5DATAA	GND	RX5DATAB
23	TX5CLKA	GND	TX5CLKB
24	TX5DATAA	GND	TX5DATAB
25	RX6CLKA	GND	RX6CLKB
26	RX6DATAA	GND	RX6DATAB
27	TX6CLKA	GND	TX6CLKB
28	TX6DATAA	GND	TX6DATAB
29	RX7CLKA	GND	RX7CLKB
30	RX7DATAA	GND	RX7DATAB
31	TX7CLKA	FRGND	TX7CLKB
32	TX7DATAA	FRGND	TX7DATAB

E+M Trunk Card (E+M)

1.0 GENERAL

The E+M Trunk Card (E+M) is a standard system port interface circuit card that resides in the Master or any Expansion Port Subrack. It supports eight E+M trunk connections. Both 2-wire and 4-wire versions are available. Jumper options are provided for Type I, II, IV or V, trunk side or signaling side operation.

2.0 SPECIFICATIONS

Microprocessor	8031 (12 MHz)
Memory	8K Bytes EPROM 2K Bytes RAM
Power Requirements	+5 Volts: 750 mA (typical) +15 Volts: 130 mA (typical) -15 Volts: 135mA (typical) +24 Volts: 96 mA (typical, with all relays On)
2-Wire Trunk Specifications	
Input Level	0 dB ± 0.5 dB
Output Level	-3 dB ± 0.5 dB
Crosstalk Attenuation	68 dB minimum
Idle Circuit Noise	23 dBmc maximum
Line Impedance	600 ohms ± 10%
Frequency Response *(Signal levels relative to 1004 Hz with C Message Filter)*	
60 Hz	-20 dB maximum
200 Hz	-10 to 0.0 dB
300 Hz	-6 to 0.0 dB
500 to 3000 Hz	-2.5 to 1.5 dB
3200 Hz	-1.5 to 1.5 dB
3400 Hz	-3.0 to 0.0 dB
Longitudinal Balance	
200 – 4000 Hz	60 dB minimum
4-Wire Trunk Specifications þþ	
Input Level	16 dB + 0.5 dB
Output Level	7.0 dB + 0.5 dB
Crosstalk Attenuation	
inter-channel	60 dB minimum
intra-channel	50 dB minimum
Idle Circuit Noise	23 DBmc maximum
Line Impedance	600 ohms ± 10%

Frequency Response *(Signal levels relative to 1004 Hz with C Message Filter)*	
60 Hz	-20 dB maximum
200 Hz	-5.0 to 0.0 dB
300 to 3000 Hz	-1.5 to 0.5 dB
3200 Hz	-1.5 to 0.5 dB
3400 Hz	-3.0 to 0.0 dB
Longitudinal Balance	
200 – 4000 Hz	60 dB minimum

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the E+M card. The four major elements of the E+M card are:

- Per Port Circuitry
- Pulse Code Modulated (PCM) Time Slot Bus Interface
- Packet Processor
- Control & Status Registers

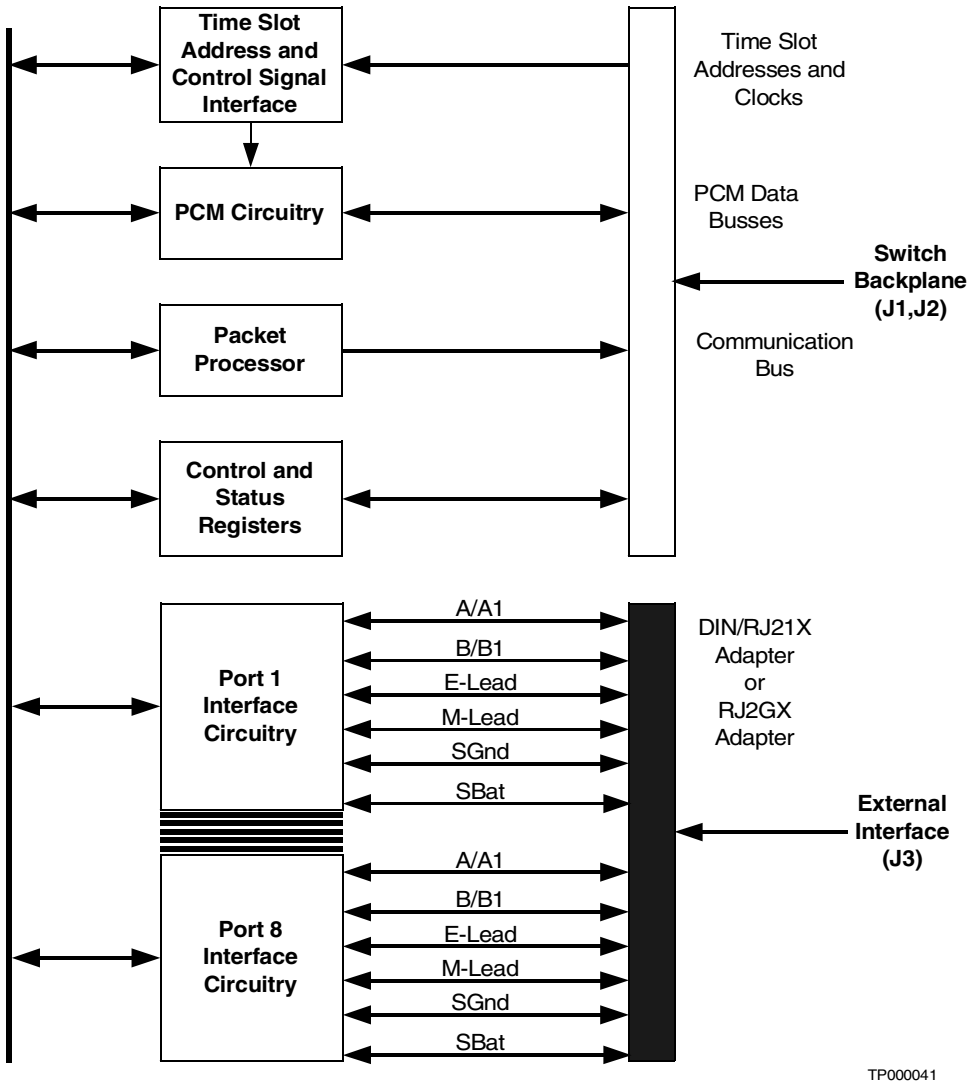


Figure 1: Block Diagram Of E+M Card

3.1 PER PORT CIRCUITRY

Each of the eight ports on a E+M card includes the following:

- Analog to Digital Encoding and Decoding
- Jumper options for Type I, II, IV or V signaling
- Jumper options for trunk or signaling side operation
- 2-wire or 4-wire voice trunks

3.1.1 ANALOG TO DIGITAL ENCODING AND DECODING

A 2913 codec provides digital to analog and analog to digital signal conversion. A codec semi-custom interface I.C. performs parallel to serial and serial to parallel conversion of the PCM data transferred between itself and the codec.

Data received from both PCM busses is latched into parallel in/serial out shift registers internal to the codec interface I.C. The codec semi-custom interface I.C. supplies the data by selecting the output of one of the two internal parallel to serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode and decode A-law or µ-law PCM data. Two jumper areas on the E+M card allow selection of the clock frequency and PCM encoding rule for all eight codecs.

3.1.2 ANALOG INTERFACE

The analog interface consists of circuitry from the tip and ring leads to the codec. Protection diodes are connected across the secondary of transformers TX01 and TX02. The analog interface is jumper-configurable for two-wire or four-wire operation. Jumper areas JX01, and JX04 through JX08 are provided for this configuration. E+M cards are factory configured for two-wire 600 ohm or four-wire 600 ohm operation with the appropriate resistor values and jumper settings.

3.1.3 E+M SIGNALING INTERFACE

No signaling is performed on the voice path of the E+M trunks. Separate signaling leads, called the E and M leads, are provided for signaling purposes. Each E+M port has a signaling relay and a signaling detector. Four electrical signaling schemes are supported on the E+M card: Type I, Type II, Type IV, and Type V. The software required to interface to the signaling circuitry is the same for all four signaling types with either trunk or signaling side hardware configurations (see Figure 2 through Figure 5). For more information on E+M signaling, refer to the *Supervision & Call Progress Tone Detection* module of the *Host Application Development Series*.

Each E+M port has signaling circuitry that is jumper-configurable for E+M Type I, Type II, Type IV, or Type V signaling. Both trunk and signaling side interfaces are supported. Protection diodes are connected between the E and M leads and battery ground for lightning protection. Two 10 ohm, half-watt resistors are connected in series with the E and M leads to limit current.

The signaling circuitry is configured via jumpers JX01, JX02, and JX03. The jumper settings are given in Section 4.0. Because of the differences in the cables required for the different signaling types, all eight ports should be configured for the same signaling type.

For each of the four interface types, the trunk circuit asserts the M lead and the signaling circuit asserts the E lead using relay KX01. A thermistor is connected in series with the asserted signal lead to protect the interface if a signaling lead is improperly shorted.

A signaling lead detector is attached to the E lead in the trunk circuit and the M lead in the signaling circuit to detect when the far end of the trunk circuit asserts its signaling lead. The detector consists of an opto-isolator whose output goes low when detecting a signaling lead assertion.

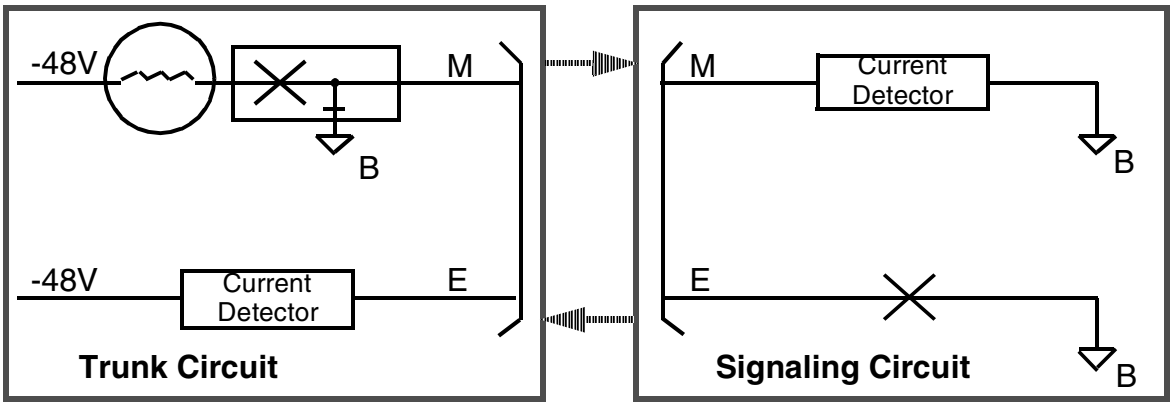


Figure 2: E+M Type I Interface

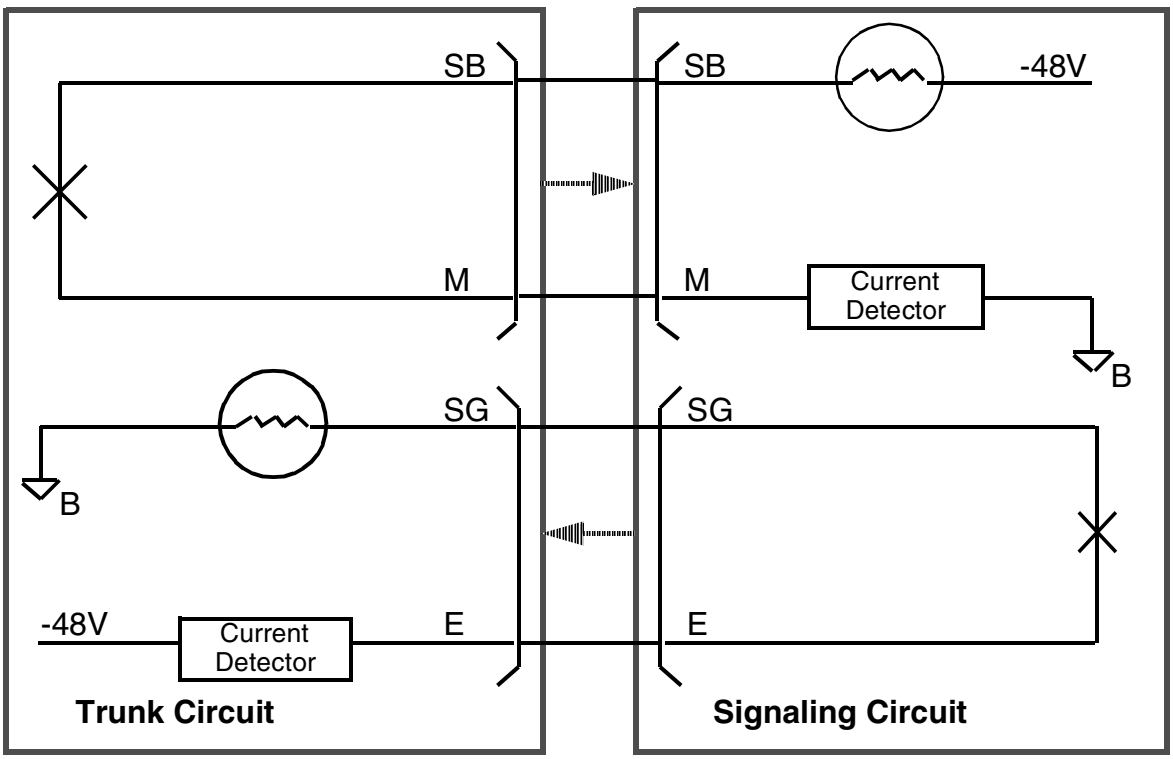


Figure 3: E+M Type II Interface

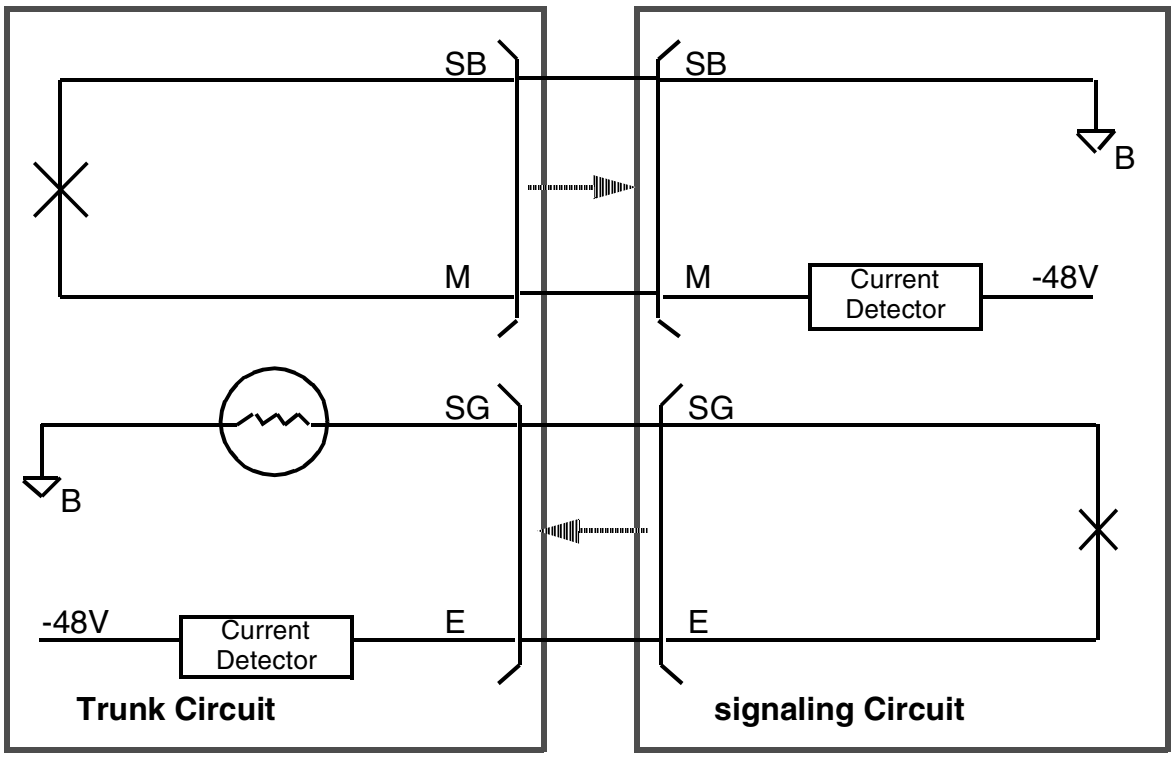


Figure 4: E+M Type IV Interface

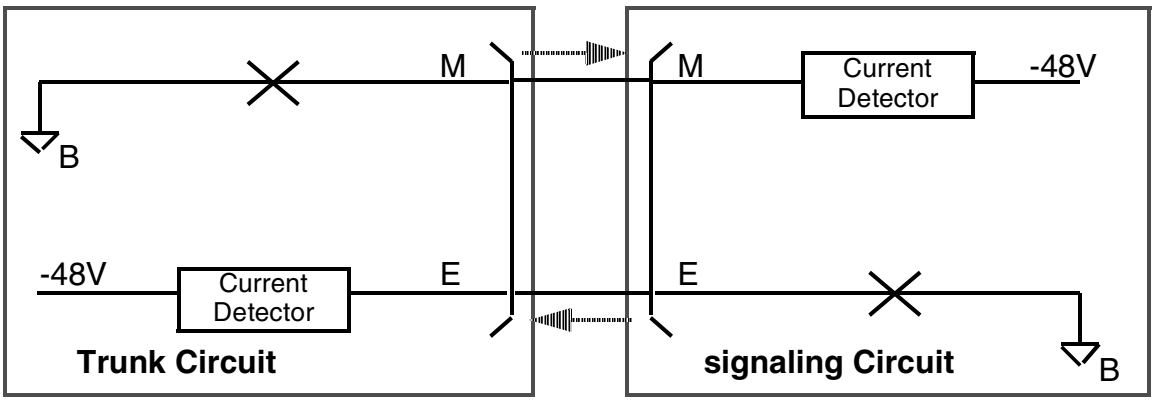


Figure 5: E+M Type V Interface

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within a system is encoded and transmitted as PCM data. The per port codec on the E+M card translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The E+M card interfaces to the dual PCM time slot busses with standard bus interface circuitry common to several system port-oriented circuit cards. Each of the eight port interfaces on the E+M card can “listen to” any time slot on either PCM data bus.

An E+M card is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular E+M port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The E+M card contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC-3). The Packet Processor polls each of the eight trunk connections looking for an event (i.e. E+M signaling lead activity). When polled by the NBC-3, the Packet Processor reports any status change. The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the E+M card.

The Communication Bus is the path by which the Packet Processor receives commands from and sends status to the NBC-3.

3.4 PCM BUS INTERFACES – J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the E+M card. Table 2 lists the pin assignments for J3.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

Table 1: E+M J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: E+M J3 Pinouts

Pin	Row A	Row B	Row C
1	Trunk 1 – E Lead	Unused	Trunk 1 – M Lead
2	Trunk 1 – Tip	Unused	Trunk 1 – Ring
3	Trunk 1 – SG	Unused	Trunk 1 – SB
4	Trunk 1 – T1	Unused	Trunk 1 – R1
5	Trunk 2 – E Lead	Unused	Trunk 2 – M Lead
6	Trunk 2 – Tip	Unused	Trunk 2 – Ring
7	Trunk 2 – SG	Unused	Trunk 2 – SB
8	Trunk 2 – T1	Unused	Trunk 2 – R1
9	Trunk 3 – E Lead	Unused	Trunk 3 – M Lead
10	Trunk 3 – Tip	Unused	Trunk 3 – Ring
11	Trunk 3 – SG	Unused	Trunk 3 – SB
12	Trunk 3 – T1	Unused	Trunk 3 – R1
13	Trunk 4 – E Lead	Unused	Trunk 4 – M Lead
14	Trunk 4 – Tip	Unused	Trunk 4 – Ring
15	Trunk 4 – SG	Unused	Trunk 4 – SB
16	Trunk 4 – T1	Unused	Trunk 4 – R1
17	Trunk 5 – E Lead	Unused	Trunk 5 – M Lead
18	Trunk 5 – Tip	Unused	Trunk 5 – Ring
19	Trunk 5 – SG	Unused	Trunk 5 – SB
20	Trunk 5 – T1	Unused	Trunk 5 – R1
21	Trunk 6 – E Lead	Unused	Trunk 6 – M Lead
22	Trunk 6 – Tip	Unused	Trunk 6 – Ring
23	Trunk 6 – SG	Unused	Trunk 6 – SB
24	Trunk 6 – T1	Unused	Trunk 6 – R1
25	Trunk 7 – E Lead	Unused	Trunk 7 – M Lead
26	Trunk 7 – Tip	Unused	Trunk 7 – Ring
27	Trunk 7 – SG	Unused	Trunk 7 – SB
28	Trunk 7 – T1	Unused	Trunk 7 – R1
29	Trunk 8 – E Lead	Unused	Trunk 8 – M Lead
30	Trunk 8 – Tip	Unused	Trunk 8 – Ring
31	Trunk 8 – SG	Unused	Trunk 8 – SB
32	Trunk 8 – T1	Unused	Trunk 8 – R1

3.5 EXTERNAL INTERFACES

The connections to the Tip and Ring leads (both 2-wire and 4-wire) and the E+M signaling leads of the eight trunk interfaces on the E+M card are made via the J3 connector. A VCO I/O Module attaches to J3 and terminates the tip/ring connections of up to three E+Ms. Table 3 lists the Plug-In Adapters/I/O Modules required for each E+M application.

Table 3: E+M DIN-to-DIN Adapter Assemblies

Application			VCO I/O Module
Trunk Type	**Signaling Interface**	**Total Trunks**	**Type**
2-Wire	I or V	24	RJ2EX
2-Wire	II or V	8	RJ2FX
4-Wire	I or V	8	RJ2GX
4-Wire	II or V	8	RJ2HX

For further information on the VCO I/O Modules, refer to the *VCO/4K Mechanical Assemblies: I/O Modules Technical Description*.

4.0 CONFIGURATION NOTES

Jumper plugs on the E+M are factory set for use in systems. Figure 6 indicates the location of jumper plug areas on E+M card. Figure 7 through Figure 9 show the jumper plug settings specific to the type of E+M signaling application. Use this information to verify or reset jumpers on an interface card prior to installing it in a Port Subrack.

> **CAUTION: Jumpers associated with interface characteristics (2- or 4-Wire) and signaling type (Type I, II, IV or V) must be identically set for all eight circuits on the E+M card. Settings must correspond to the VCO I/O Module installed on the system Port Subrack. Failure to set each circuit for identical operation will result in cross-wiring problems.**
>
> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card. The PCB may be etched with two to four characters indicating the revision level. Only the first two or three characters are important. In four-character rev. level markings, the final letter "R" indicates that the PCB is at Release level. For example, a revision level C0Q card may be marked as Rev. "CQ", "C0Q" or "C0QR".*

If a card is improperly configured, it may fail to perform its interface function between external trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a E+M in the system data base, refer to the *System Administrator's Guide.*

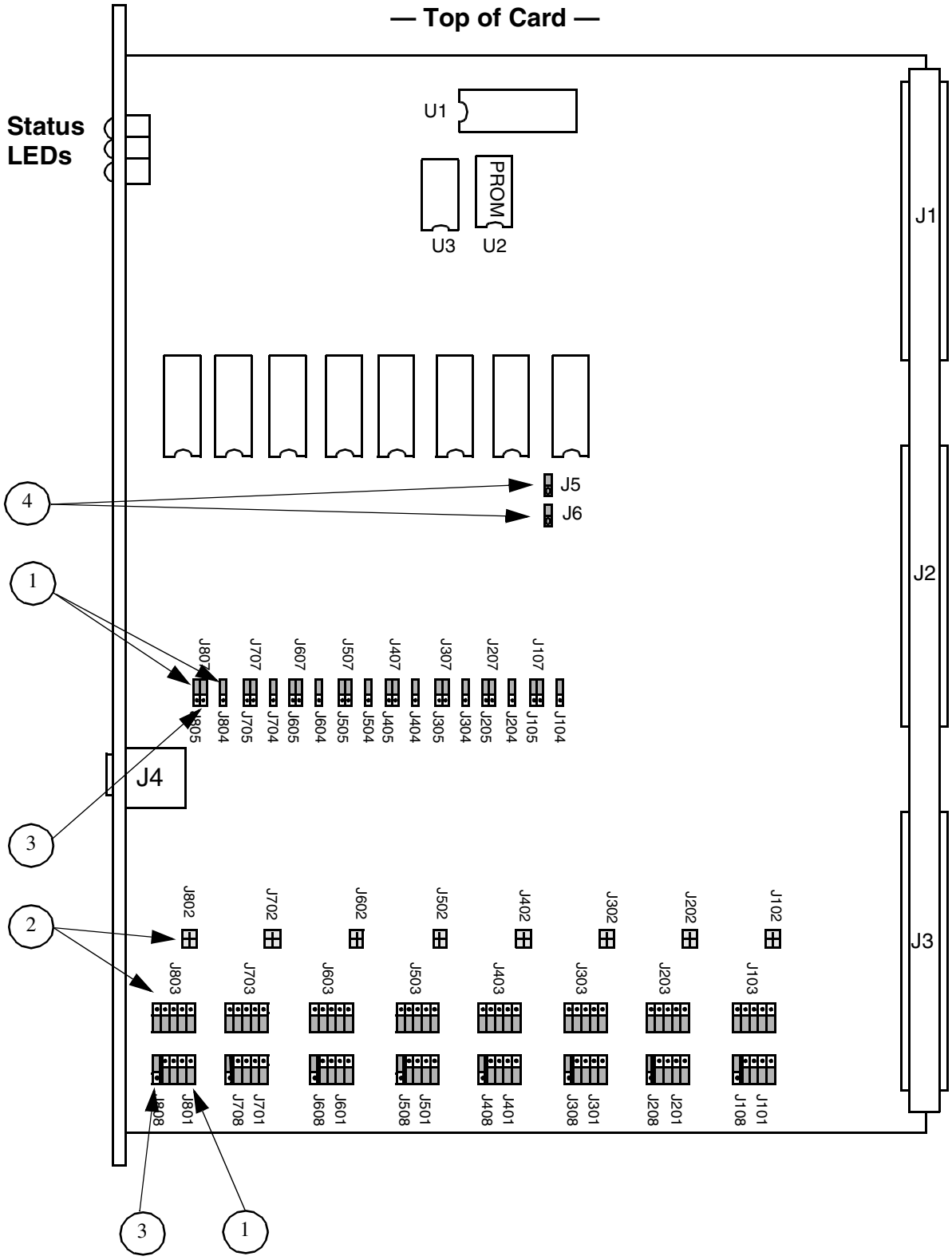


Figure 6: E+M Jumper & PROM Locations

4.1 E+M TRUNK CARD

4.1.1 JUMPER LOCATIONS

NOTE 1

A block of twelve jumper pins constitutes JX01 on the E+M card (X = circuits 1 through 8). JX01 sets each circuit for 2-Wire or 4-wire operation along with JX04 and JX05. Block diagrams of the jumper pin arrangements for JX01, JX04, JX05, and JX07 are provided in Figure 7 (2-wire), Figure 8 (2-wire), and Figure 9 (4-wire).

> *NOTE: E+M Cards using PCB artwork Rev. C0Q and C0R require different jumper settings for 2-Wire configurations. These unique jumper settings are shown in Figure 8*

NOTE 2

Jumper locations JX02 and JX03 are set for the type of signaling employed for the circuit (Xþ=þcircuits 1 through 8). Jumper arrangements vary according to whether the trunk is set for Switching or signaling side operation. Block diagrams of JX02 and JX03 jumper pin arrangements are provided in Figure 7 (2-wire), Figure 8 (2-wire), and Figure 9 (4-wire).

NOTE 3

Jumper locations JX07 and JX08 are set for either 900-ohm or 600-ohm trunk circuits (Xþ=þcircuits 1 through 8). Only 600-ohm terminations are currently supported for system E+M cards. See Figure 7 (2-wire), Figure 8 (2-wire), and Figure 9 (4-wire).

NOTE 4

Jumpers at J5 and J6 determine the codec clock and PCM law for the card.

- Install jumper plug at J5 in “U-LAW” position for µlaw operation (North American standard).
- Install jumper plug at J5 in “A-LAW” position for A-law operation (European standard).
  The default setting for J5 is “U-LAW” for µlaw operation
- Install jumper plug at J6 in “1.544” position for 1.544Mhz operation (North American standard).
- Install jumper plug at J6 in “2.048” position for 2.048MHz operation (European standard).
  The default setting for J6 is “1.544” for 1.544MHz operation

PROM 1

The 2764 PROM in location U2 contains firmware appropriate to E+M signaling interface requirements.

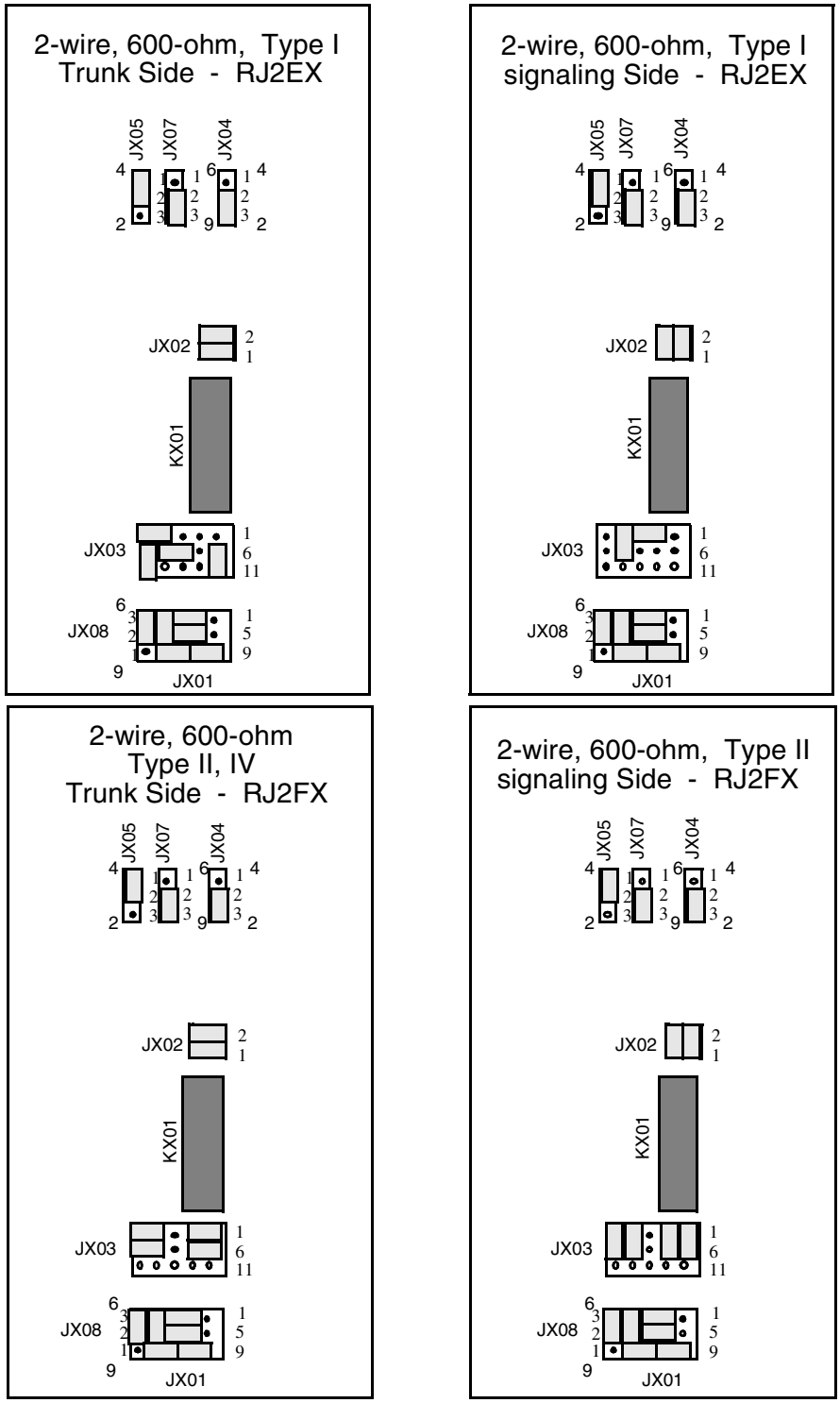


Figure 7: E+M 2-Wire Jumper Settings
Rev. C (Except Rev. C0Q & C0R)

Figure 4 (continued): E+M 2-Wire Jumper Settings
Rev. C (Except Rev. C0Q & C0R)

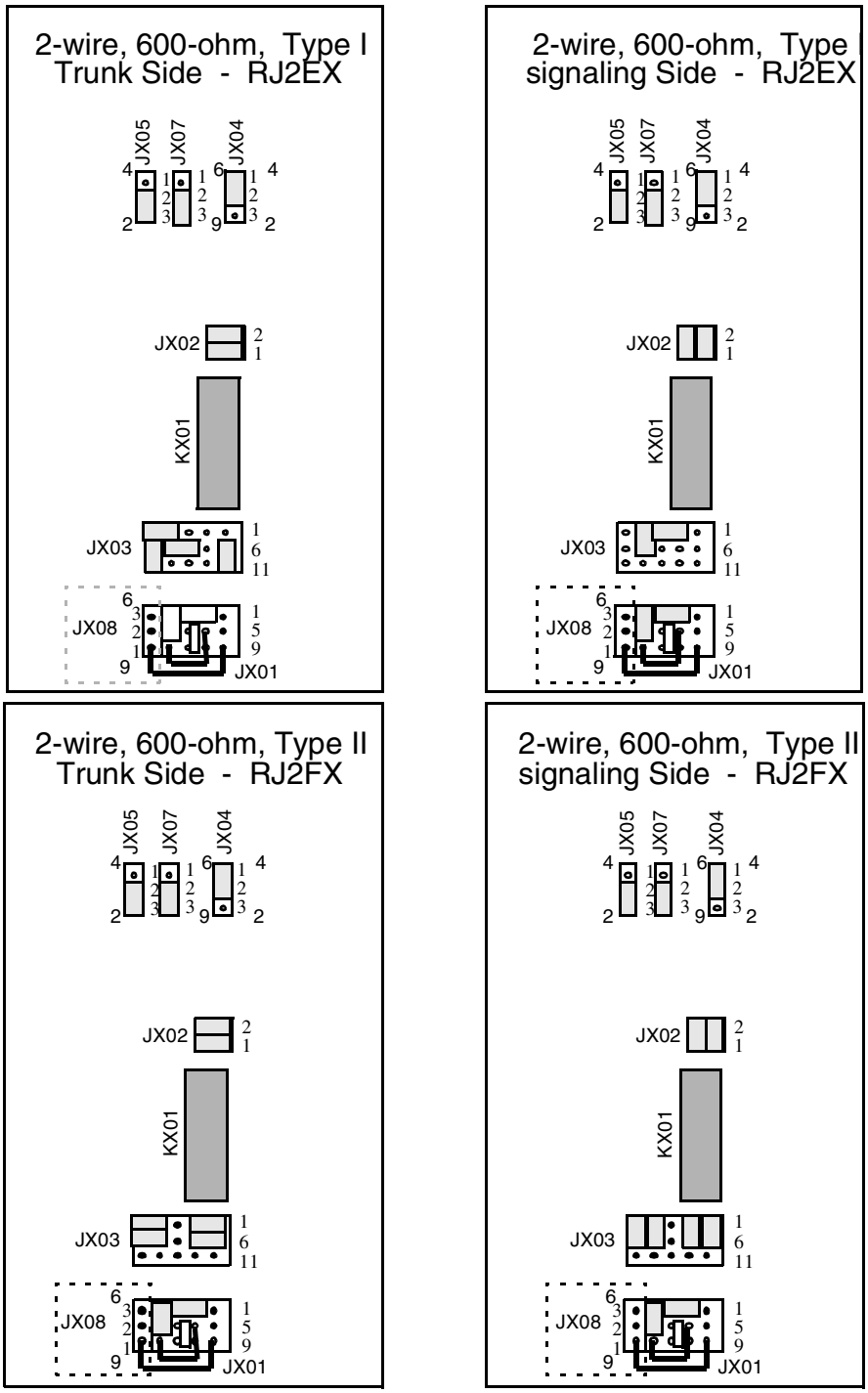


Figure 8: E+M 2-Wire Jumper Settings
Rev. C0Q, C0R & Rev. D

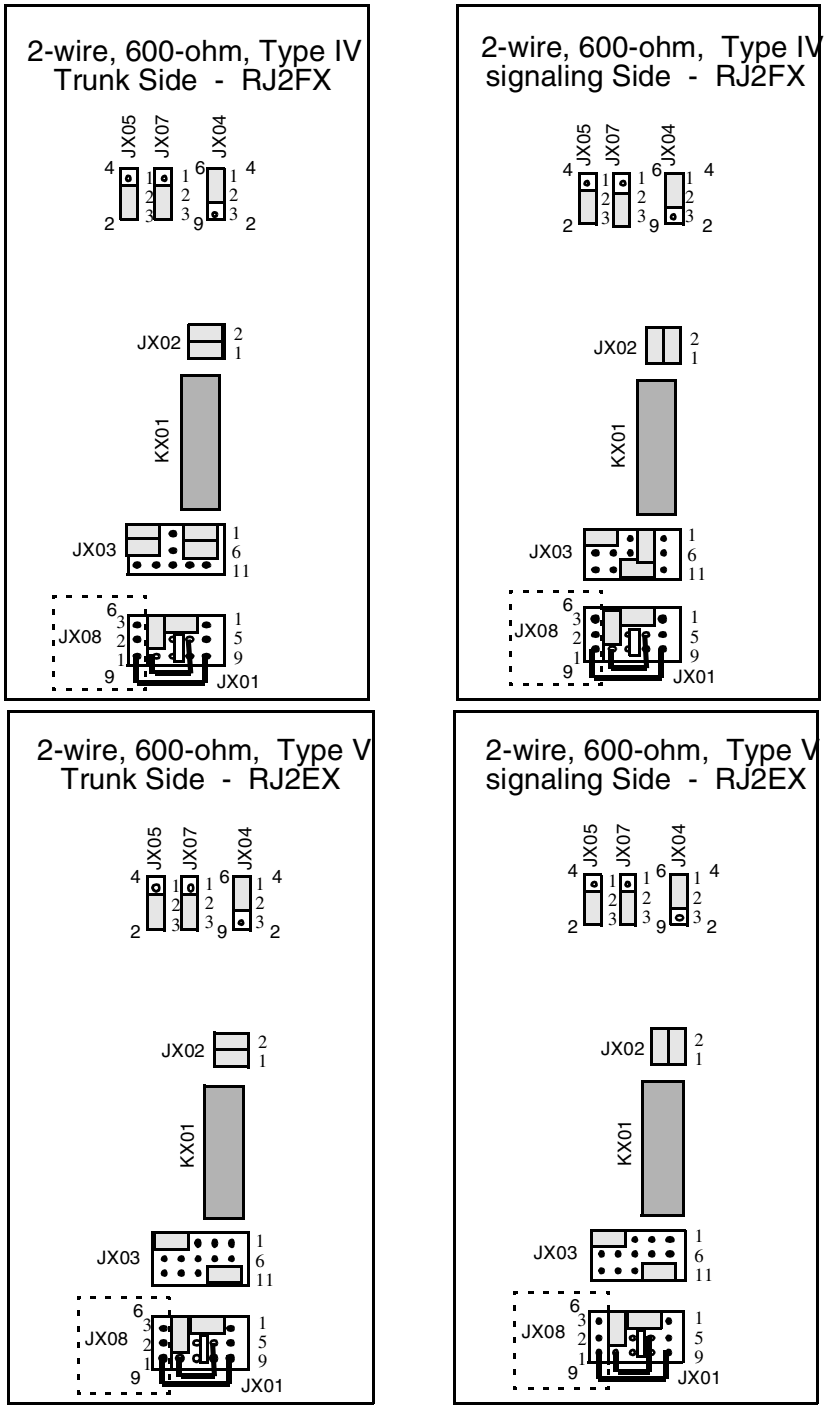


Figure 4 (continued): E+M 2-Wire Jumper Settings
Rev. C0Q, C0R & Rev. D

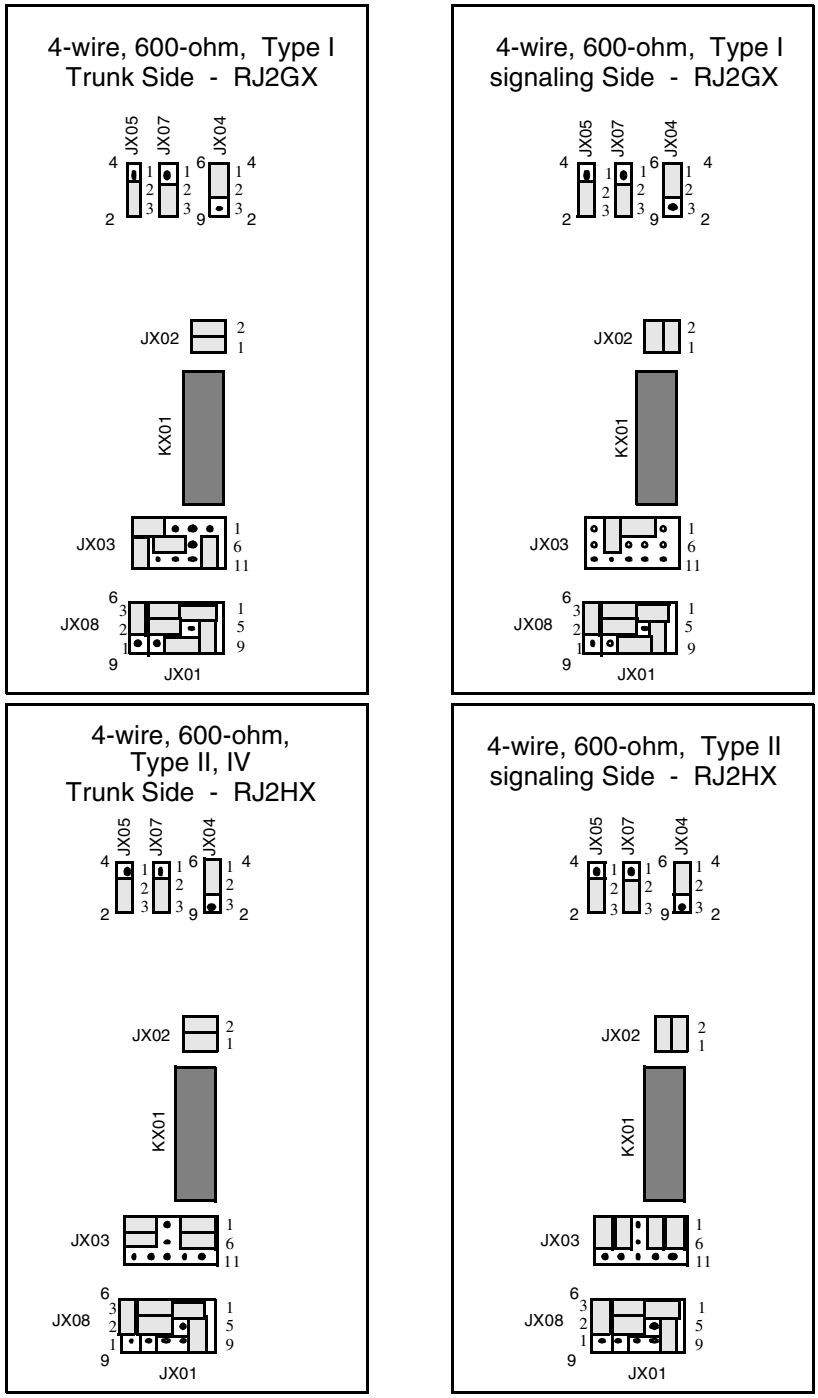


Figure 9: E+M 4-Wire Jumper Settings, Rev. C & D

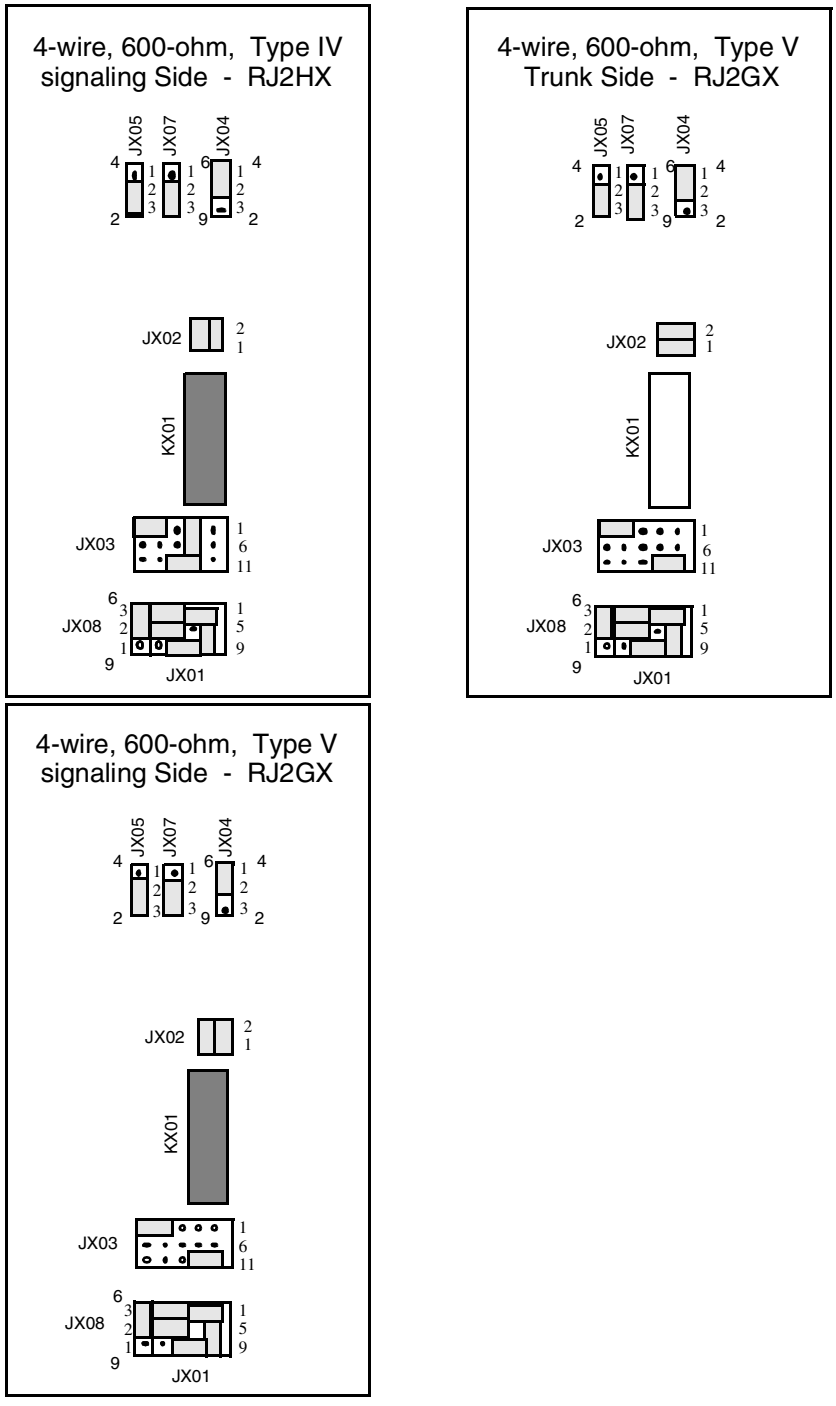


Figure 4 (continued): E+M 4-Wire Jumper Settings, Rev. C & D

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the E+M card, refer to the following publications:

- VCO/4K Product Overview
- VCO/4KSystem Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K Host Application Development Series: Supervision & Call Progress Tone Detection
- VCO/4K System Maintenance Manual
- VCO/4K Technical Description: Port Subrack
- VCO/4K Mechanical Assemblies: VCO/4K I/O Modules Technical Description

Four Span Programmable T1 Interface Card (4xT1)

1.0 GENERAL

The Four Span Programmable T1 Interface (four span T1) card is a standard port interface circuit card that resides in the Master or Expansion Port subrack. It supports four spans of 24 voice and data channels at 56 Kbps or 64 Kbps, and complies with Bell System DS-1 specifications for transmission at 1.544 Mps. You can assign incoming, outgoing, and two-way service to 24 individual non-blocking channels on a span.

You can synchronize system timing to a programmable T1 span, or an internal or external reference. Additionally, you can designate primary and secondary Master Timing links to which the system is synchronized. If both links fail, or the external reference signal is lost, the system defaults to the internal reference clock. For more information about any of the features on the Four Span T1 card, refer to the *System Administrator's Guide*.

2.0 SPECIFICATIONS

Microprocessor:	(4) MC68302, (1) MC68340
Memory:	256K per processor SRAM
	64K/68302 EPROM 28K/68340 EPROM
Power Requirements:	17.5 Watts @ 5VDC max
Input T1 Stream Format:	D4 or ESF
Data Encoding:	Alternate Mark Inversion (AMI)
Data Transparency:	Selectable bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, or none
Frequency:	1.544 MHz ± 76 Hz
Impedance:	100 ohms ± 10 ohms
Output T1 Stream Format:	D4 or ESF
Data Encoding:	AMI
Data Transparency:	B8ZS, Bit 7 zero stuff, or none
Frequency:	1.544 MHz ± 76 Hz
Impedance:	100 ohms ± 10 ohms

2.1 PROGRAMMABILITY

The application software is downloaded to each span controller which enables independent provisioning of each span as well as each channel. For more information about provisioning spans or channels, refer to the *System Administrator's Guide.*

3.0 CIRCUIT DESCRIPTION

The Four Span T1 card has duplicate circuitry for each of the spans and the common interface to the system backplane, which includes an MC68340 communication controller.

Each span circuit consists of an MC68302 span controller, a framer, and a Line Interface Unit (LIU). The system controller passes internal commands to each span controller, which provisions the framer and LIU. The span controller monitors the framer and LIU for alarms or signaling transitions and reports these events back to the system controller.

The LIU terminates the T1 stream and passes it to the framer. Channel information is passed onto the PCM circuitry.

The system controller sets up and tears down circuit paths through the high-speed serial bus.

Figure 1 illustrates a simplified block diagram of the Four Span T1 card. The components of the card are discussed in the following subsections.

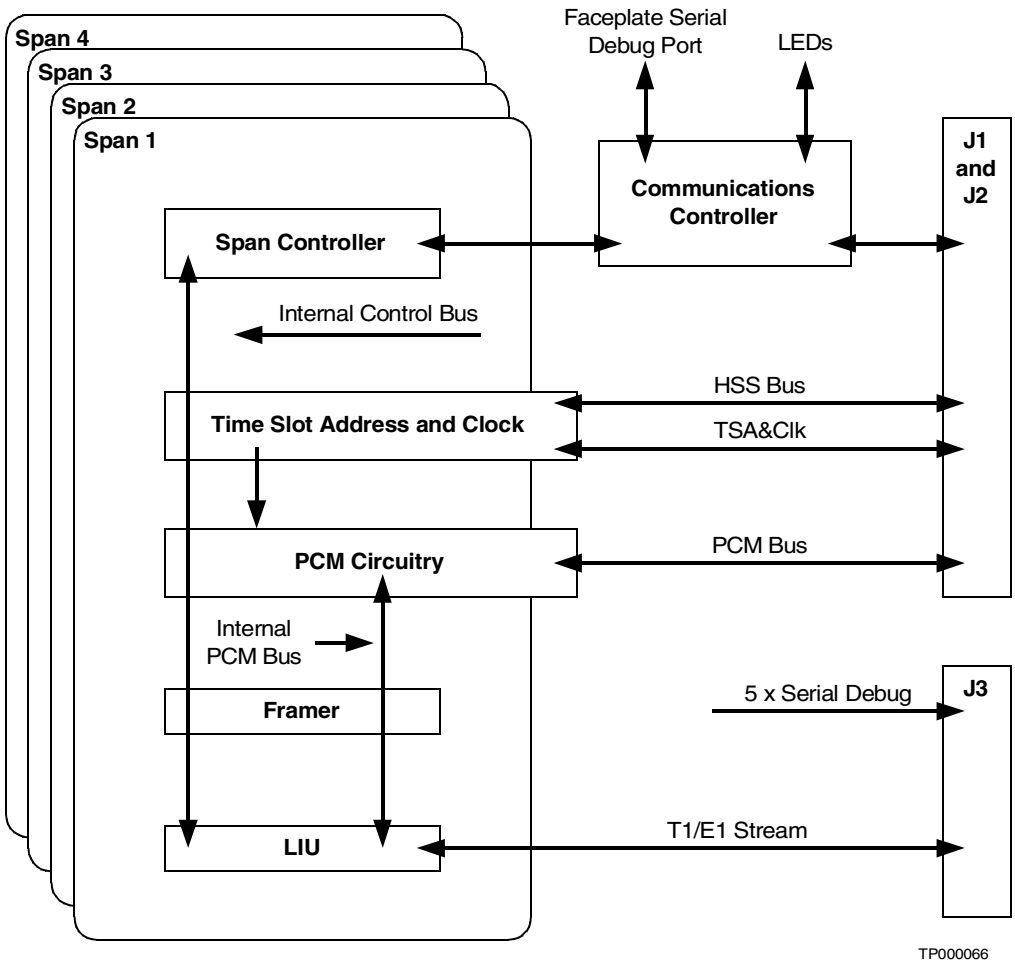


Figure 1: Block Diagram of the Four Span T1 Card

3.1 SHARED CIRCUITRY

The Four Span T1 card includes the following shared circuitry.

- Clock drivers
- PCM drivers
- Base address definition

3.2 INDIVIDUAL SPAN CIRCUITRY

The Four Span T1 card interfaces the system with a T1 digital data carrier stream. The Four Span T1 card transmits/receives four 1.544 MHz, 24-channel, bipolar digital data streams. The J3 connector and a compliant connector configuration (RJ45, DB15, and RJ48H types) on the back of the system interfaces with the PCM stream. You can synchronize the stream with the system clock, the receive clock, or an on-board crystal.

The Four Span T1 card detects loss of carrier, frame, and remote alarms on its incoming T1 stream. It detects and reports receive slips when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus. It similarly detects and reports transmit slips. The Four Span T1 card contains an elastic PCM data buffer to minimize slips caused by any Four Span T1 stream frequency jitter.

The Line Interface Unit (LIU) and the T1 framer provides electronically compliant signal levels.

3.2.1 INTERNAL CONTROL BUS

The Span controller has a full functional memory mapped interface to the Framer and LIU. It also has a memory-mapped interface to the Base Address Time Slot and Clock circuitry with which it sets the base address and chooses the system reference clock.

The PCM circuit interrupts the span controller on receive and transmit slip events.

3.2.2 FRAMER (PER SPAN)

The DS2141 framer interfaces to a T1, 1.544Mbps digital trunk through the LIU. The framer performs

- Alarm detection (Yellow, Blue, Carrier Lost, Loss of Sync)
- Alarm injection (Yellow and Blue alarms)
- Channel separation
- D4/ESF framing and D4 superframing (in-band, robbed-bit signaling transmission)
- Robbed bit signaling/channel (A, B, C and D)
- Data transparency
- AMI, B8ZS, data encoding

  NOTE: You can use B8ZS for T1 to maintain 1's density (and timing) while providing data transparency.

3.2.3 LIU (PER SPAN)

The LIU on the Four Span T1 card (CS61575 or LXT304A) is a fully integrated transceiver designed for 1.544/2.048 Mbps operation. The LIU supports full-duplex transmission of digital data over a 100Ω (T1) balanced installation. The LIU supports Stratum 4 clocking and also requires a transmit clock of 1.544 MHz ±76 Hz to maintain clock integrity (and therefore data integrity, i.e., 0 bit errors). The LIU performs

- Bipolar-to-TTL conversion on the transmit side
- Electrical wave shaping on the receive side
- Clock recovery
- Jitter attenuation - AT&T 62411 1990 Stratum 4, Type 2
- Line buildout selection
- Loopback and maintenance functions
- All ones (1s) generation
- Signal monitoring (for loss of signal and quality transmission)

3.3 LED STATES

LED indicators appear on the front panel of the Four Span T1 card.

Table 1 lists the LED states on the Four Span T1 card.

Table 1: LED States on the Four Span T1 Card

Card Status	Controller	Green	Yellow	Red
Card Plugged In	68340	ON	ON	ON
Self Test	68340	ON	Blinking	OFF
Receiving Download	68340	Blinking	OFF	OFF
Card Failure	68340	ON	OFF	ON
Card OOS[ab]	1) All	ON	OFF	OFF
Major Alarm[a]	2) All	OFF	OFF	ON
Minor Alarm[a]	3) All	OFF	ON	OFF
Card Active	4) All	OFF	OFF	OFF

[a] If one span is OOS and another span has a major alarm, the OOS status takes precedence and the green LED illuminates.

[b] If the span status is diagnostics, remote, or payload, the green LED is illuminated.

3.4 PIN ASSIGNMENTS

Table 2 lists the J1 pin assignments on the Four Span T1 card.

Table 2: J1 Pin Assignments on the Four Span T1 Card

Pin	Row A	Row B	Row C
1	DGND	*Unused*	DGND
2	DGND	*Unused*	DGND
3	DGND	*Unused*	DGND
4	DGND	*Unused*	DGND
5	Battery Return	*Unused*	Battery Return
6	Battery Return	*Unused*	Battery Return
7	Battery Return	*Unused*	Battery Return
8	*Unused*	*Unused*	*Unused*
9	Ring Voltage	*Unused*	Ring Voltage
10	*Unused*	*Unused*	*Unused*
11	Digital +5V	*Unused*	Digital +5V

Table 2: J1 Pin Assignments on the Four Span T1 Card (Continued)

Pin	Row A	Row B	Row C
12	Digital +5V	*Unused*	Digital +5V
13	Digital +5V	*Unused*	Digital +5V
14	–24V	*Unused*	+24V
15	Battery (-48V)	*Unused*	Battery (-48V)
16	Battery (-48V)	*Unused*	Battery (-48V)
17	Battery (-48V)	*Unused*	Battery (-48V)
18	Analog -15V	*Unused*	Analog -15V
19	Analog -15V	*Unused*	Analog -15V
20	Analog +15V	*Unused*	Analog +15V
21	Analog +15V	*Unused*	Analog +15V
22	Card Addr. Bit 1	*Unused*	Card Addr. Bit 0
23	Card Addr. Bit 3	*Unused*	Card Addr. Bit 2
24	Card Addr. Bit 5	*Unused*	Card Addr. Bit 4
25	Card Addr. Bit 7	*Unused*	Card Addr. Bit 6
26	SRV	*Unused*	AB1
27	DID	*Unused*	AB2
28	RST	*Unused*	Serial Bus
29	*Unused*	*Unused*	*Unused*
30	AGND	*Unused*	AGND
31	AGND	*Unused*	AGND
32	DGND	*Unused*	DGND

Table 3 lists the J3 pin assignments on the Four Span T1 card.

Table 3: J3 Pin Assignments on the Four Span T1 Card

Pin	Row A	Row B	Row C
1	*RX_RS232_340*	*Unused*	*TX_RS232_340*
2	DGND	*Unused*	DGND
3	*RX_RS232_302_1*	*Unused*	*TX_RS232_302_1*
4	DGND	*Unused*	DGND
5	*RX_RS232_302_2*	*Unused*	*TX_RS232_302_2*
6	DGND	*Unused*	DGND
7	*RX_RS232_302_3*	*Unused*	*TX_RS232_302_3*
8	DGND	*Unused*	DGND
9	*RX_RS232_302_4*	*Unused*	*TX_RS232_302_4*
10	DGND	*Unused*	DGND
11	*Reserved*	*Unused*	*Reserved*
12	*Reserved*	*Unused*	*Reserved*
13	*Reserved*	*Unused*	*Reserved*
14	*Reserved*	*Unused*	*Reserved*
15	*Unused*	*Unused*	*Unused*
16	*Unused*	*Unused*	*Unused*
17	*Unused*	*Unused*	*Unused*
18	*Unused*	*Unused*	*Unused*
19	*Unused*	*Unused*	*Unused*
20	*Unused*	*Unused*	*Unused*
21	*Unused*	*Unused*	*Unused*
22	Rx Line Ring Span 1[a]	*Unused*	Tx Line Ring Span 1[b]
23	Rcv Line Tip Span 1[a]	*Unused*	Tx Line Tip Span 1[b]
24	*Unused*	*Unused*	*Unused*
25	Rx Line Ring Span 2[a]	*Unused*	Tx Line Ring Span 2[b]
26	Rcv Line Tip Span 2[a]	*Unused*	Tx Line Tip Span 2[b]
27	*Unused*	*Unused*	*Unused*
28	Rx Line Ring Span 3 [1]	*Unused*	Tx Line Ring Span 3 [2]
29	Rcv Line Tip Span 3[1]	*Unused*	Tx Line Tip Span 3[2]
30	*Unused*	*Unused*	*Unused*
31	Rx Line Ring Span 4 [1]	*Unused*	Tx Line Ring Span 4 [2]
32	Rcv Line Tip Span 4[1]	*Unused*	Tx Line Tip Span 4[2]

[a] Signal to Four Span T1 Card.
[b] Signal from Four Span T1 Card

4.0 CONFIGURATION NOTES

The following subsections include configuration information for the T1 MDF adapter and the jumper positions on the Four Span T1 card.

4.1 MDF ADAPTER

The T1 MDF adapter accommodates two Four Span T1 cards in three slots.

NOTE: The third (unused)slot must be occupied by a service circuit card.

The MDF is located at P3 on the port subrack backplane, in the back of the system. There are three T1 MDF connectors; one offers eight DSUB-15 connectors, another offers eight RJ45 interfaces, and one more offers an RJ48H (50 pin Champ) connector to support three cards in three slots. For more information about the MDF adapter, refer to the *Plug-in MDF Adapter Technical Description*.

The layout of the Four Span T1 card is shown in Figure 2.

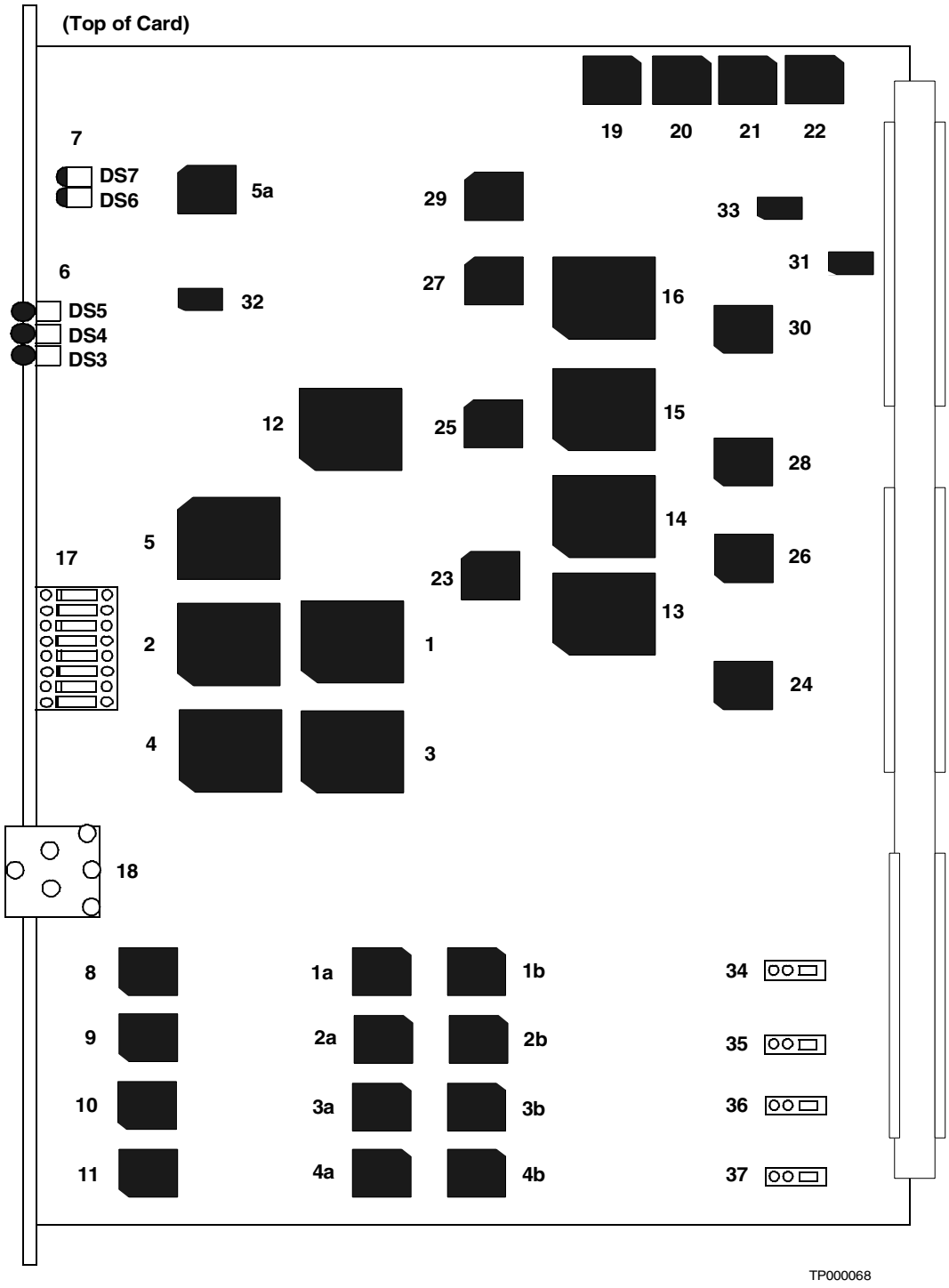


Figure 2: Four Span T1 Interface Board Layout

NOTE: Not all components/devices are shown.

Table 4 lists the callouts in Figure 2.

Table 4: Four Span T1 Interface Board Callouts

Callout	Meaning
1	MC68302 Span 1 (U65)
1a	MC68302 Span 1 Even PROM (U48)
1b	MC68302 Span 1 Odd PROM (U49)
2	MC68302 Span 2 (U111)
2a	MC68302 Span 2 Even PROM (U94)
2b	MC68302 Span 2 Odd PROM (U93)
3	MC68302 Span 3 (U200)
3a	MC68302 Span 3 Even PROM (U186)
3b	MC68302 Span 3 Odd PROM (U185
4	MC68302 Span 4 (U155)
4a	MC68302 Span 4 Even PROM (U151)
4b	MC68302 Span 4 Odd PROM (U150)
5	MC68302 (U1)
5a	MC68302 PROM (U10)
6	Front Panel LEDs (D3-5)
7	MC68302 Status LEDs (D6, 7)
8	Span 1 FRAMER-INT PLD (LP92, U44)
9	Span 2 FRAMER-INT PLD (LP92, U91)
10	Span 3 FRAMER-INT PLD (LP92, U183)
11	Span 4 FRAMER-INT PLD (LP92, U135)
12	1XT1PCM PLD (LP91, U211)
13	SPAN 1 4XT1PCM PLD (LP90, UU43)
14	SPAN 2 4XT1PCM PLD (LP90, UU90)
15	SPAN 3 4XT1PCM PLD (LP90, UU182)
16	SPAN 4 4XT1PCM PLD (LP90, UU134)
17	8-Position Switch (S1)
18	Front Panel Diag Port (5V RS232)

Table 4: Four Span T1 Interface Board Callouts (Continued)

Callout	Meaning
19	Span 3 Path Setup PROM (U178)
20	Span 1 Path Setup PROM (U35)
21	Span 2 Path Setup PROM (U86)
22	Span 4 Path Setup PROM (U116)
23	Span 1 RX Gain/Law PROM (U28)
24	Span 1 TX Gain/Law PROM (U25
25	Span 2 RX Gain/Law PROM (U67)
26	Span 2 TX Gain/Law PROM (U78)
27	Span 3 RX Gain/Law PROM (U158)
28	Span 3 TX Gain/Law PROM (U170)
29	Span 4 RX Gain/Law PROM (U120)
30	Span 4 TX Gain/Law PROM (U131)
31	Comm Bus PLD (LP94, U14)
32	Virt Comm Bus PLD (LP93, U8)
33	Base Address PLD (LP89, U219)
34	Span 1 Transmit Line Match Selector JP1
35	Span 2 Transmit Line Match Selector JP2
36	Span 3 Transmit Line Match Selector JP4
37	Span 4 Transmit Line Match Selector JP3

4.2 JUMPER POSITIONS

The following subsection includes configuration information for the jumper positions JP1 through JP4 on the Four Span T1 card. For more information about jumpers JP1 through JP4, see Figure 3.

4.2.1 75/120 OHM T1 LINE INTERFACE SELECTION

Verify that the jumpers JP1 through JP4 are set to the pin configuration shown in Figure 3.

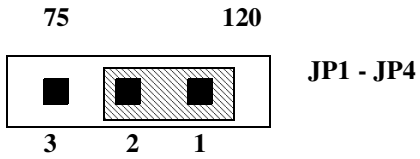


Figure 3: JP1 through JP4 Jumper Pin Configuration

4.2.2 EIGHT POSITION DIP SWITCH FOR LAW SETTINGS

A 8 position dip switch (S1) provides law configuration on a per-span basis. Table 5 lists the A- and µ-law settings for S1. For information about the S1 dip switch location, see Figure 3.

Table 5: A- and µ-law Settings for S1

Switch Setting	µ-law	A-law
1	Open	Closed
2	Open	Closed
3	Open	Closed
4	Open	Closed

NOTE: Switch selections 5 to 8 are not used.

The on-board switches match the PCM law of the switch. To provision the PCM law of the T1 stream, refer to the System Administrator's Guide.

Figure 4 shows an S1 switch configured for µ-law. The shaded areas signify that the switch is pushed in. This switch configuration sets all four spans to µ-law.

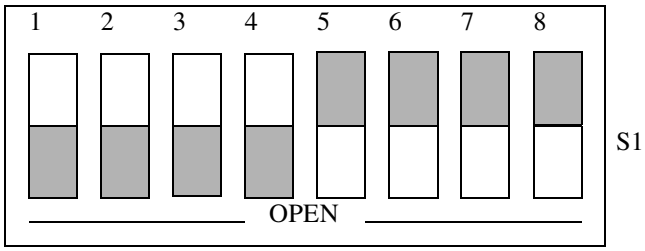


Figure 4: µ-law Configuration Switch

Figure 5 shows an S1 switch configured for A-law. The shaded areas signify that the switch is pushed in. This switch configuration sets all four spans to A-law.

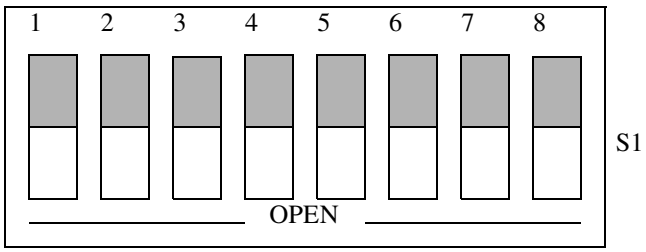


Figure 5: A-law Configuration Switch

5.0 TROUBLESHOOTING

5.1 LOSS OF SYNCHRONIZATION OF INCOMING REFERENCE

A modification to the Four Span T1/E1 card has been made which improves the integrity of the incoming synchronization reference signal. This modification is available to customers upon request.

Problem symptoms include loss of synchronization of the incoming reference, and/or excessive slips. Note that systems that take their incoming reference on a single-span T1 card may also be affected, systems which do not have any Four Span T1 cards are not affected.

Customers who are experiencing these symptoms should call Cisco Systems Technical Support to make arrangements to replace their existing Four Span T1/E1 cards.

5.2 CARDS NOT COMING INTO SERVICE

Mechanical stress on the center of Four Span T1/E1 cards can cause some of the socketed devices to come loose. When this occurs, spans on the card may not come in to service.

The affected devices are located at callouts 12 through 16 in Figure 6. If a card or any of the spans fail to come in to service, the devices may need to be reseated in their sockets.

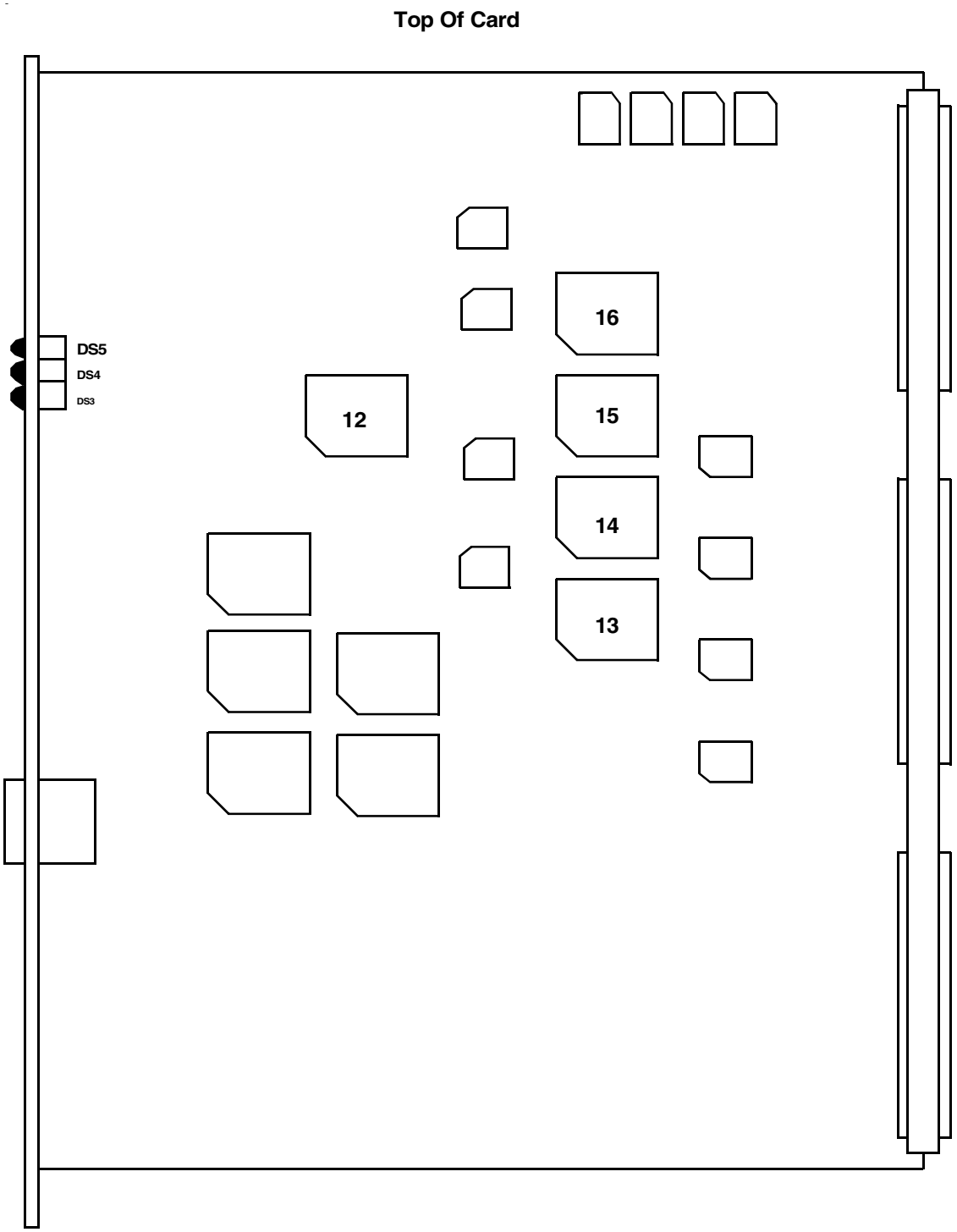


Figure 6: Four Span T1/E1 Card Devices 12 - 16

To reseat devices 12 through 16, complete the following steps:

1. Remove the card from the system following the instructions in the VCO/4K Card Overview. Be sure to observe proper Electro Static Discharge (ESD) procedures.
2. Place your antistatic mat or envelope and card on a flat surface, such as a table.
3. Press on the center of each device until it clicks into the socket.

   CAUTION: Do not continue to apply pressure after you hear the click. Continued pressure may cause the device pins to bend.

4. Reinstall the card in the system following the instructions in the VCO/4K Card Overview.
5. Test the card. If the card continues to fail, contact Cisco Systems Technical Support.

Interface Controller Card (ICC)

1.0 GENERAL

The Interface Controller Card (ICC) is a high-capacity network interface engine. The ICC card employs Cisco Systems' mid-plane architecture which enables it to connect with a series of I/O modules specific to different network interface requirements. The mid-plane isolates the unique physical characteristics of each type of connection leaving the ICC to perform all of the signaling and protocol processing independently. There are six I/O modules supporting 4, 8, or 16 network spans. A C-bus enabled, VCO switching platform (VCO 4K Series) with a full complement of ICC cards and 16-span I/O modules will support more than 4000 ports.

For information on the I/O Modules refer to the Interface Controller Card I/O Module technical description for the appropriate network.

The ICC is fully programmable, enabling user control over individual channels.

Other features:

- contains on-board FLASH memory for rapid configuration and boot-up time
- managed from Cisco Systems' Administration Console
- supports SNMP protocol
- is a single-slot Cisco Systems *Type 2* card
- can be installed on both C-bus and non-C-bus systems (lower port capacity)
- derives all on-board voltages from the +5v system supply
- may use any span as an incoming master timing source
- with 16 spans each, 11 cards will support 4,080 T1 timeslots, or 8 cards will support 4,064 (clear channel) E1 timeslots.

Restrictions:

- supported by VCO Series systems only (VCO 4K Series for maximum ports)
- C-bus must be enabled for the increased port capability
- all spans on a card must be of the same network type

2.0 SPECIFICATIONS

2.1 COMPLIANCE WITH STANDARDS

The ICC Card is in compliance with all applicable U.S. and international standards. See Table 1.

Table 1: Standards Compliance

Category	Standard
Safety	UL1459 CSA C22.2 EN-60950 IEC-950
EMI/EMC	FCC Part 15 (US/Canada) EN55022 (Europe) EN50082-1 (Europe) VCCI (Japan)
PCB Manufacture	IPC

2.2 ICC CARD SPECIFICATIONS

Microprocessor	MPC860MH-50
Memory	8MB FLASH
	16MB DRAM SIMM
Power Requirements	5 Volts – 3.5 A (Typical)

3.0 ICC CARD ARCHITECTURE

The ICC card is a single-slot Cisco Systems *Type 2* card. A separate I/O module provides access to the network interfaces. The I/O module includes active circuitry such as T1/E1 framers and is unique to each network configuration. Regardless of the span configuration, the CPU card is common.

The ICC card is inserted in the VCO switch from the front of the system. An I/O Module, inserted at the rear of the system, aligns with each ICC card.

The ICC card contains the following functions:

- Core CPU and memory subsystem
- Communications Bus Interface
- PCM Interface
- I/O Interface

The block diagram for the ICC card and I/O Module is shown in Figure 1.

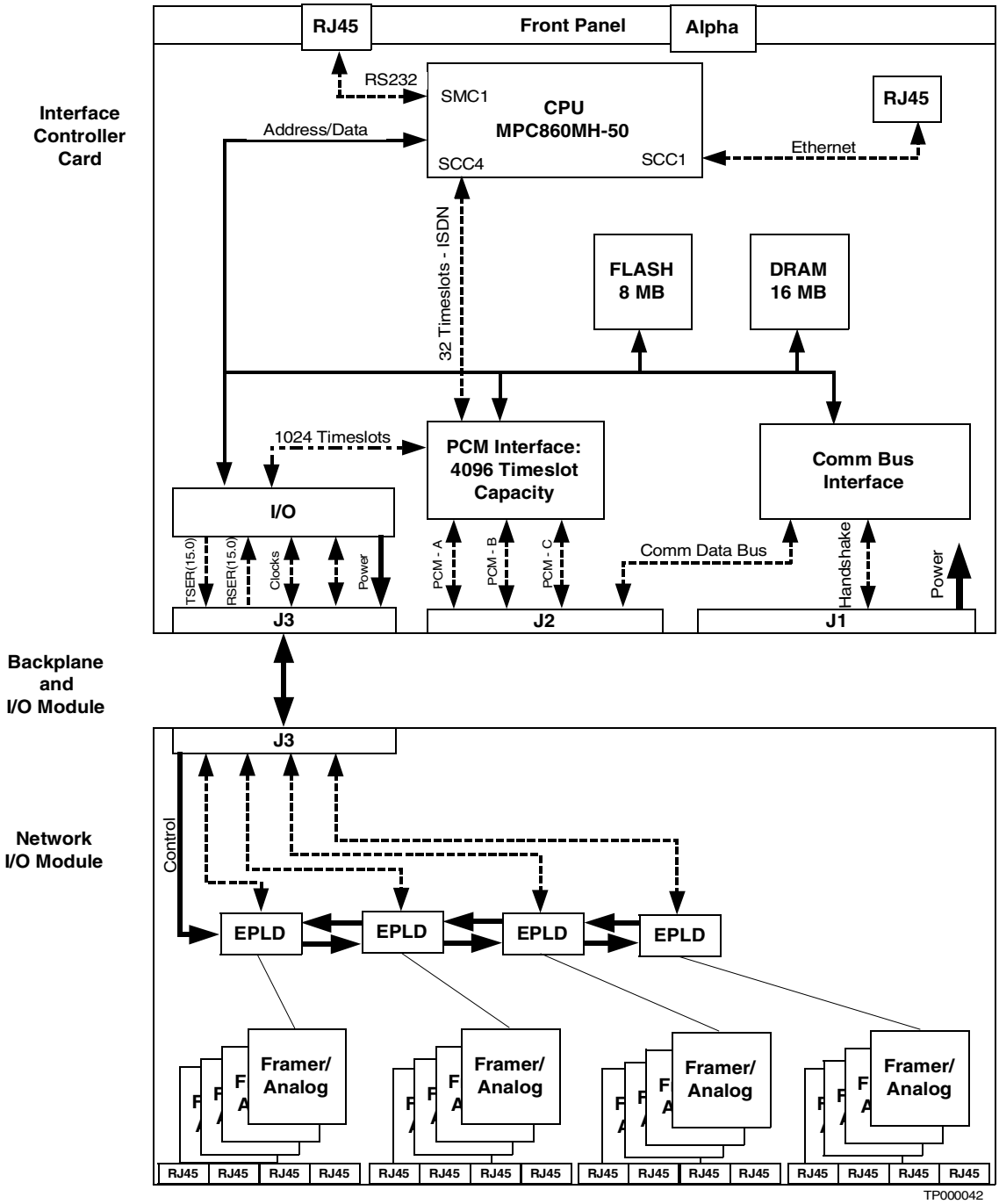


Figure 1: ICC Card and I/O Module Architecture

3.1 CPU AND MEMORY ARCHITECTURE

The Core Processor coordinates all activities of the ICC card including:

- Controlling time slot assignments on the PCM buses
- Controlling up to 16 network interfaces
- Communicating with the NBC over the Comm Bus (Tx/Rx FIFOs)
- Managing the PCM time slot assignments for voice traffic (Tx/Rx SMXs)
- Managing PCM law conversion & gain control (Tx/Rx look up table SRAM)
- Managing the telephony components of each network interface (Framers)
- Controlling the Alpha display on the faceplate

The MPC860 processor controls up to 16 network trunks and manages all aspects of the network interface such as framing, call control, mu-law/a-law conversion, gain control, etc.

The MPC860 processor communicates to the Network Bus Controller (NBC) via the Comm Bus. The Comm Bus interface is controlled primarily by dedicated hardware. The Comm Bus interface handshakes all signals with the NBC and retrieves data from, and store data to memory, by interrupting the MPC860 at the end of a cycle.

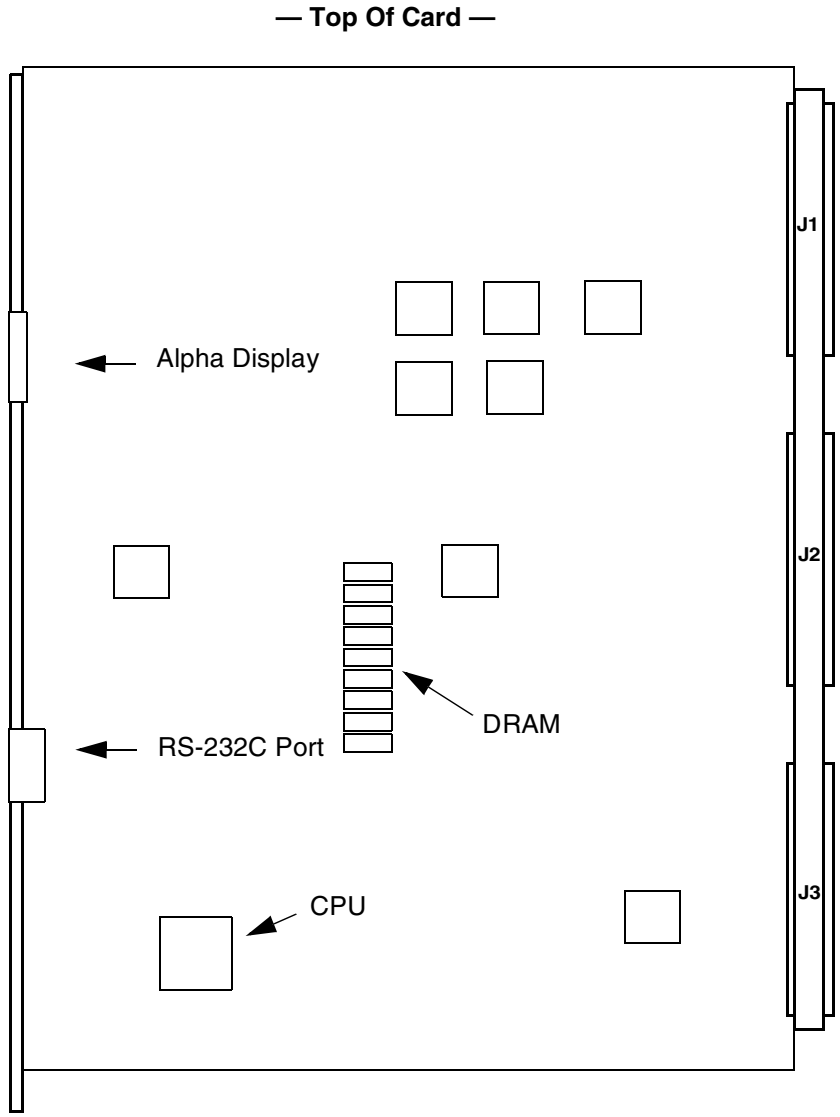


Figure 2: ICC Card Layout (Component Side)

NOTE: Not all components are shown.

3.1.1 SMC1 - RS232 PORT

The MPC860 Processor has one RS-232 port, which is accessible from the face plate. This port utilizes an RJ-45 jack. The electrical signal levels are RS-232 compliant.

NOTE: The front panel RJ45 jack is not intended for customer use.

3.1.2 FLASH MEMORY

The FLASH memory boots the processor so that the application and/or diagnostic software can be downloaded over the Comm Bus when new revisions are required. The boot FLASH is 8Mbytes.

3.1.3 DRAM MODULE

The MPC860 processor has an EDO DRAM array of 16Mbytes on a 72-pin SIMM memory device (similar to a PC memory). The EDO DRAM array is arranged in a 32-bit arrangement, and is controlled by the on-chip DRAM controller provided by the MPC860.

3.1.4 ALPHA DISPLAY/POWER FAILURE LED

The ICC card displays status on a 5x7 Alpha display located on the ICC front panel. Table 2 defines the Alpha display states.

> *NOTE: The ICC card has a card failure LED immediately above the Alpha display. This LED indicates a major ICC or I/O card circuit failure. Replace the cards if this is lighted.*

Table 2: Alpha Display States

Display	Meaning
B	Blue Alarm
E1	Card is E1
F	Framing Error
M	Maintenance
N	No I/O Module
O	Out-of-Service
R	Red Alarm
T1	Card is T1
Y	Yellow Alarm
Download Progress Meter	Rotating line pattern

Only the most severe alarm state is displayed on the LED.

The bottom row of the LED matrix identifies which group of spans is reporting the alarm. The left most LED indicates group 1, the next LED indicates group 2, etc. The fifth, right most, LED indicates the state of the core processor. If this fifth LED stops blinking, the card should be removed and reinserted. If the LED still fails to blink, replace the card.

Table 3 lists the conditions that cause a major or minor alarm in the ICC.

Table 3: ICC Card Alarm Conditions

Major Alarm	Minor Alarm
Loss of Carrier	Slip Threshold Exceeded
	OOF Threshold Exceeded
	Loss of Remote Carrier
	Signaling Bit Error
	OOF Error
	Out-of-Service (OOS)

3.2 COMMUNICATIONS BUS ARCHITECTURE

The MPC860 processor uses the Comm Bus to communicate with the NBC. The Comm Bus Interface protocol is managed mostly by hardware, although CPU control is required. An EPLD controls the handshaking and read/write strobes to (2) FIFOs which store inbound and outbound packets.

The communications bus has the following associated functions:

- Communicates with other boards on the backplane through the Comm Bus.
- Initiates all data transfers on the Comm Bus.
- Sends messages to just one card.

The Comm Bus is a one byte wide half-duplex interface. This interface facilitates the transfer of messages between the port cards and the NBC-3.

The Comm Bus architecture of the ICC card is responsible for:

- Managing the signal handshaking to/from the NBC (via EPLD)
- Managing packet storage (in and outbound FIFOs)
- Managing packet termination to/from CPU (via EPLD)

The Comm Bus architecture supports directed downloads.

3.3 PCM INTERFACE

3.3.1 BUS SUPPORT

There are three PCM busses on the Cisco Systems backplane, known as the A, B, and C Buses. These are 8-bit parallel busses running at 8.192 MHz, with the exception of the C-bus which runs at 16.384 MHz. The C-bus is used with the ICC card to achieve 4K ports.

3.3.2 TRANSMIT GAIN/LAW CONVERSION

Each of the inbound and outbound timeslots have the ability to apply mu-law/a-law conversion and gain control. The gain/law conversion occurs between the SMX-controlled Transmit PCM DPRAMs and the Transmit PAC.

The available gains are: 0dB, -3dB, -6dB, -12dB, +1.5dB, +3dB, +6dB, and +12dB.

3.4 I/O INTERFACE

The J3 connector is the interface between the I/O Module and the ICC card. This includes the following functions:

- Signal buffering
- Transmit clock configuration (per Framer)
- Reference clock selection
- Framer host interface and interrupt control

4.0 PROGRAMMABILITY

4.1 OVERVIEW

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

The ICC card supports a number of programmable parameters which allow card customization:

- Network programmable protocol
- Line build-out
- Gain control
- Companding law
- Timing for system synchronization
- Transmitted timing source
- Line coding
- Frame control

Cisco Systems can assist in creating your desired parameters on a floppy diskette which you load into the VCO.

4.2 PROTOCOL IMPLEMENTATION

Support for network protocols is provided by a state machine (the Protocol State machine) that operates on the ICC card. This is a software module that defines how the ICC card will behave as a result of specific events.

The state machine performs an action for each pre-defined event. This state machine is fully programmable, allowing any action to take place as a result of any specific event. This allows pre-defined configuration of a port or span. Standard network (T1, E1) protocols are pre-programmed. The standard protocols may be modified to meet specific needs and saved as a customized protocol or a new protocol can be developed. All protocols (pre-programmed, modified, or newly-developed) are stored with a unique identifier.

To configure the ICC with a new protocol, select one or more ports/spans on which the protocol will be executed. The protocol configuration information is transmitted to the ICC when each span is activated.

4.3 NETWORK CONSIDERATIONS

A standard or user-defined protocol is implemented at the port level when the ICC is configured as a T1 card and implemented at the span level when configured as an E1 card. Also, to configure the port (T1) or span (E1) with any protocol, the port/span cannot have active calls. The port or span must be placed in the OOS state when changing protocol configuration.

5.0 CONFIGURATION NOTES

The ICC card is software configurable via downloads. There are no jumpers or replaceable PROMs on the ICC card.

6.0 RELATED DOCUMENTS

For additional information on the ICC card in VCO/4K Systems, refer to the following publications:

- VCO/4K Series Hardware Planning Guide
- VCO/4K System Administrator's Guide
- VCO/4K System Maintenance Manual
- Central Processing Unit (CPU) Technical Description
- Combined Controller Assembly Technical Description
- Alarm Arbiter Card (AAC) With Alarm Interface Card (AIC) Technical Description

Interface Controller Card T1 I/O Module

1.0 GENERAL

The VCO System uses active I/O modules in conjunction with the ICC card to connect to the network. Each I/O Module uses one slot on the backplane and supports one ICC card. The I/O Module is located at the back of the switch and must be aligned with the ICC card. A block diagram for the ICC I/O Module is shown at the bottom of Figure 1.

The T1 I/O Module is a specialized backplane card that provides T1 network connection to the ICC card. It is available in three configurations supporting 4, 8, or 16 T1 spans. The ICC card is inserted in the VCO switch from the front of the system. The I/O Module, inserted at the rear of the system (before ICC insertion), aligns with each ICC card.

The T1 I/O module supports a 100-ohm network interface and includes active circuitry such as T1 framers.

For information on the ICC, card refer to the Interface Controller Card (ICC) technical description.

2.0 SPECIFICATIONS

2.1 COMPLIANCE WITH STANDARDS

The ICC I/O Module is in compliance with all applicable U.S. and international standards. See Table 1.

Table 1: Standards Compliance

Category	Standard
Safety	UL1459 CSA C22.2
Jitter	Pub 62411
EMI/EMC	FCC Part 15 (US/Canada) VCCI (Japan)
PCB Manufacture	IPC
Lightning/Power Cross	CSA C22.2 FCC Part 68 CS-03

Table 1: Standards Compliance

Category	Standard
Telecom	FCC Part 68 CS-03 JATE AT&T Publication 62411 Bellcore PUB43801 TR-NPL-000054 TR-TSY-000510 TR-TSY-000191 ANSI T1.403

2.2 I/O MODULE SPECIFICATIONS

Power Requirements (Maximum)	5 Volts (from the ICC card)
	4 Span T1 – 1.16 A
	8 Span T1 – 1.42 A
	16 Span T1 – 1.95 A

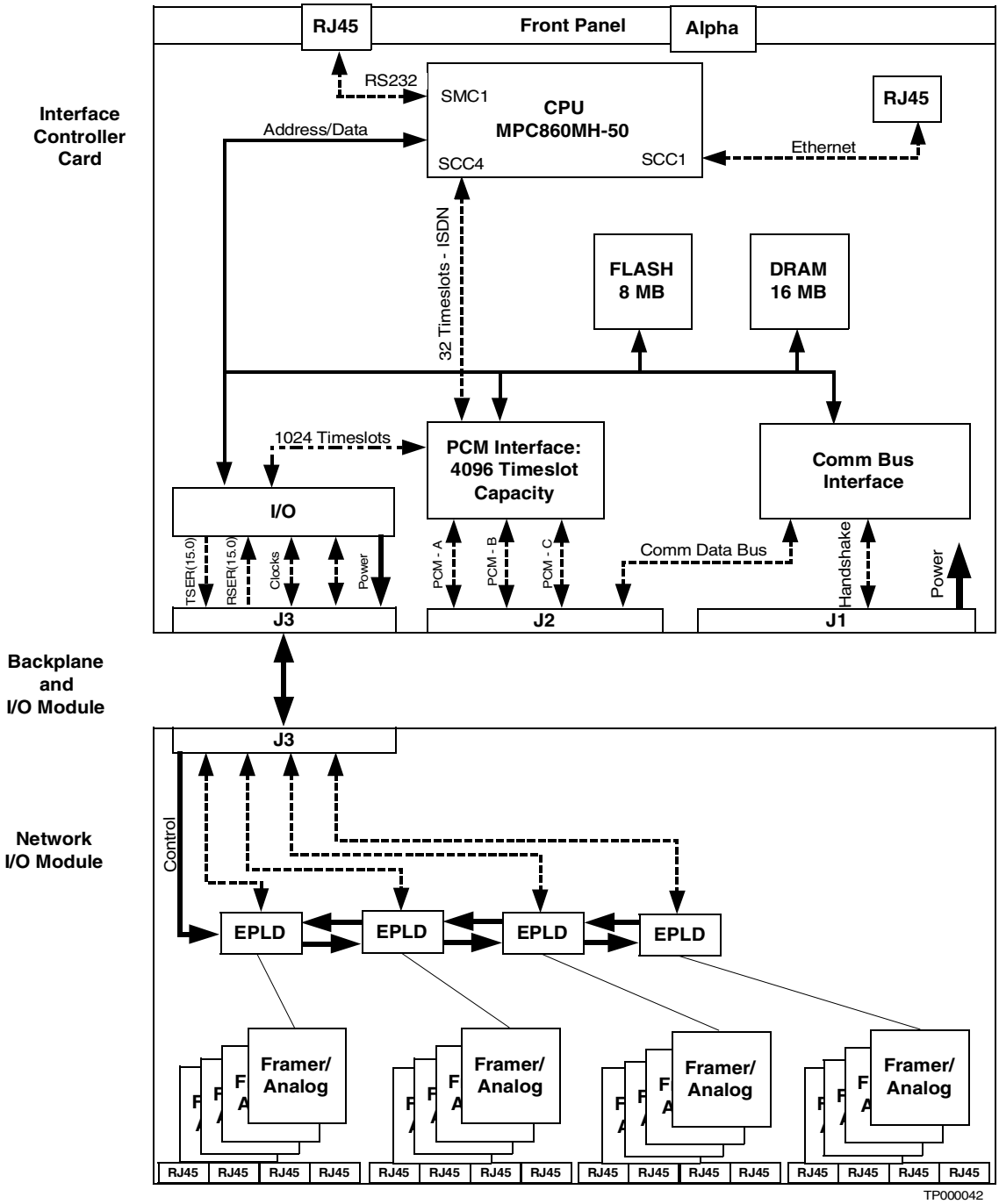
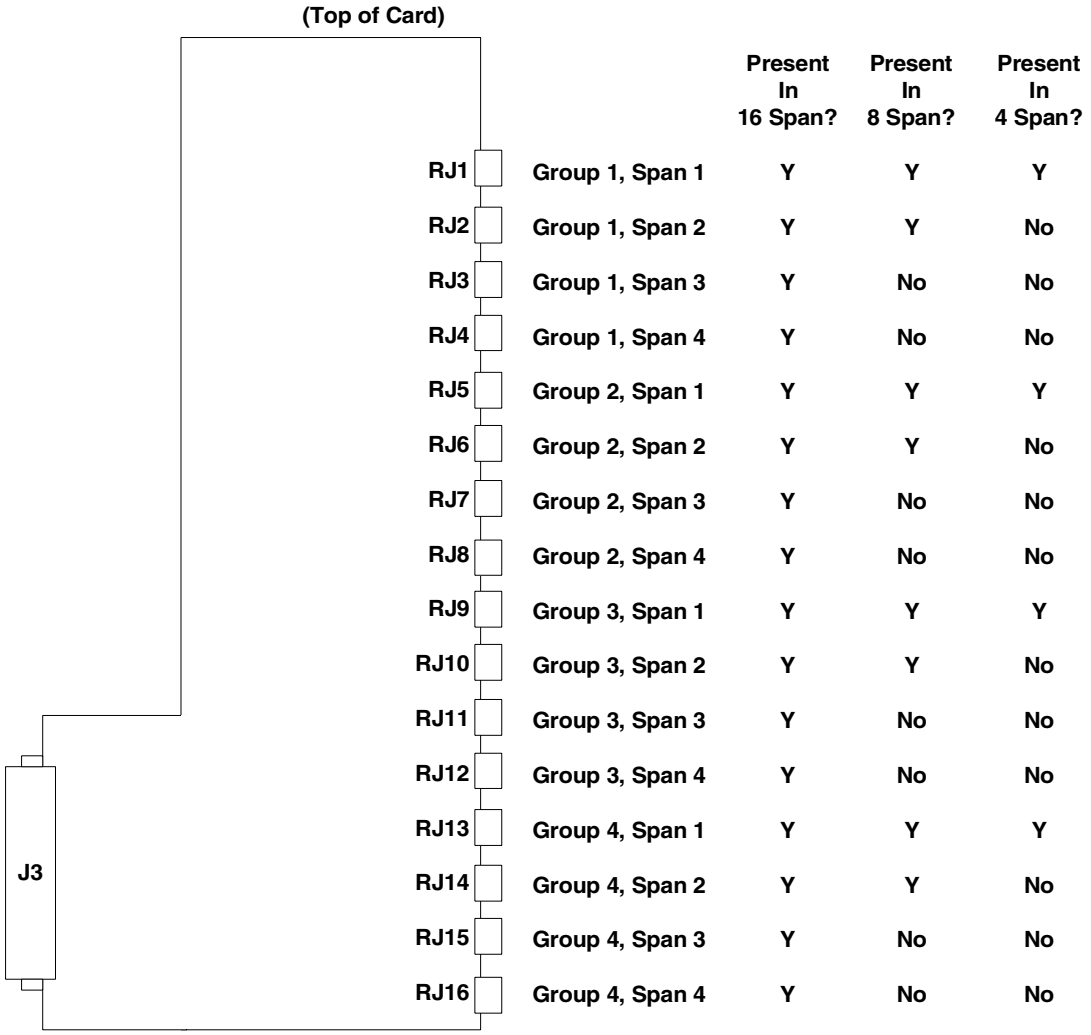


Figure 1: ICC Card and I/O Module Architecture



		Present In 16 Span?	Present In 8 Span?	Present In 4 Span?
RJ1	Group 1, Span 1	Y	Y	Y
RJ2	Group 1, Span 2	Y	Y	No
RJ3	Group 1, Span 3	Y	No	No
RJ4	Group 1, Span 4	Y	No	No
RJ5	Group 2, Span 1	Y	Y	Y
RJ6	Group 2, Span 2	Y	Y	No
RJ7	Group 2, Span 3	Y	No	No
RJ8	Group 2, Span 4	Y	No	No
RJ9	Group 3, Span 1	Y	Y	Y
RJ10	Group 3, Span 2	Y	Y	No
RJ11	Group 3, Span 3	Y	No	No
RJ12	Group 3, Span 4	Y	No	No
RJ13	Group 4, Span 1	Y	Y	Y
RJ14	Group 4, Span 2	Y	Y	No
RJ15	Group 4, Span 3	Y	No	No
RJ16	Group 4, Span 4	Y	No	No

Figure 2: I/O Module Card Layout (16-Span, Circuit Side)

NOTE: Not all components are shown.

2.2.1 EXTERNAL INTERFACES

Table 2 lists the external interfaces for the I/O Module.

Table 2: External Interfaces

Interface	Connections
I/O Module to Network	RJ45 Connector with the following pinout: Pin 1 Tx Ring Pin 8 Tx Tip Pin 4 Rx Ring Pin 5 Rx Tip

3.0 PROGRAMMABILITY

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

The ICC card supports a number of programmable parameters which allow card customization:

- T1 programmable protocol
- Line build-out
- Gain control
- Timing for system synchronization
- Transmitted timing source
- Line coding
- Frame control

Cisco Systems can assist in creating your desired parameters on a floppy diskette which you load into the VCO.

3.1 I/O INTERFACE

The J3 connector is the interface between the I/O Module and the ICC card. This includes the following functions:

- Signal buffering
- Transmit clock configuration (per Framer)
- Reference clock selection
- Framer host interface and interrupt control

4.0 I/O MODULE DESCRIPTION

The I/O Module interfaces the VCO/4K system with 4, 8, or 16 T1 digital data carrier streams. Each stream consists of a 1.544 Mbps, 24-channel, bipolar digital data stream. VCO system synchronization may be set to the receive clock of any T1 span on the I/O Module (the Master Timing Link).

The I/O module's Framers are segmented into groups of four called Framer Groups. This design approach reduces the chance of a single point of failure on the card. A hardware failure on the I/O Module normally affects only a group (1, 2 or 4 spans) and not the entire I/O Module. Figure 3 illustrates the span grouping architecture of the I/O Module.

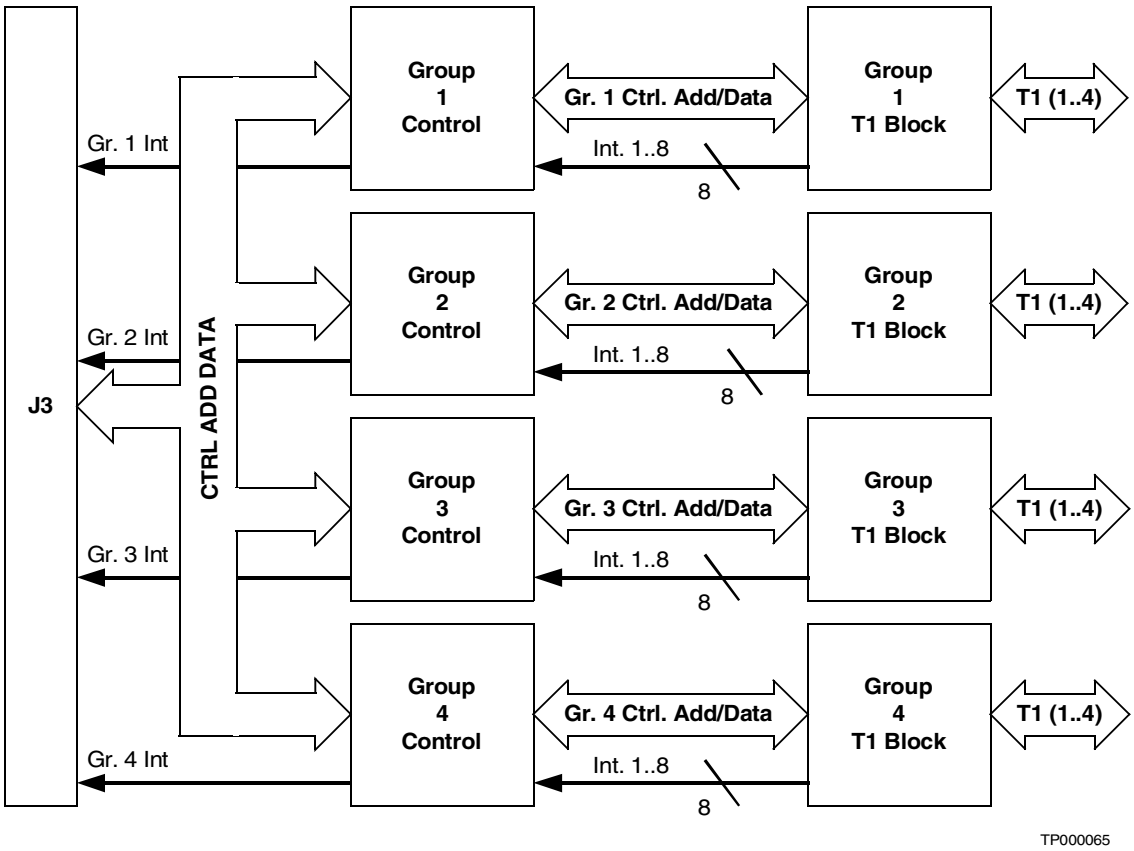


Figure 3: 16-Span I/O Module Span Grouping

The T1 Framer (Figure 4) contains a Line Interface Unit (LIU). The LIU contains three sections: 1) the receiver which handles clock and data recovery, 2) the transmitter which wave shapes and drives the T1 line, and 3) the jitter attenuator.

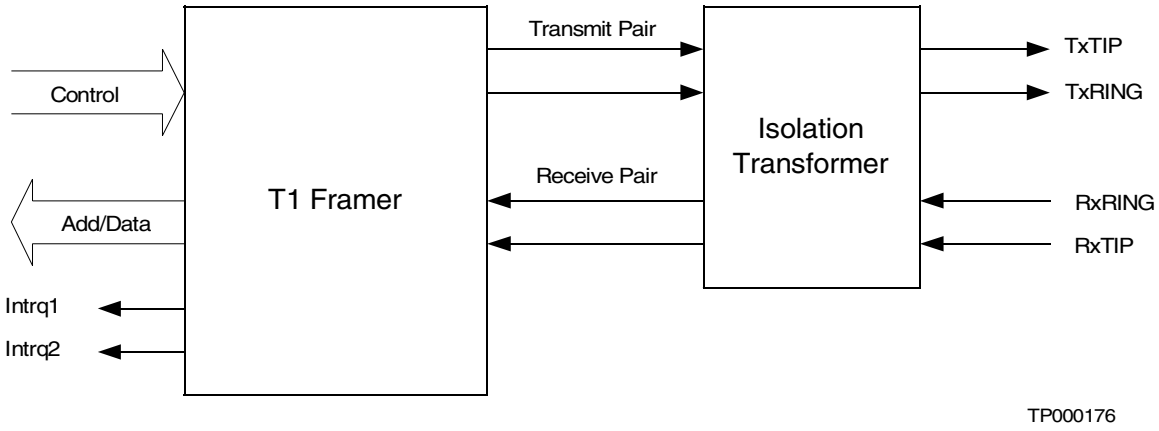


Figure 4: Framer Block Diagram

The LIU adjusts to the T1 signal being received and can handle T1 transmit line lengths from 0 to 655 ft. as configured from the Port Configuration screen (See the *System Administrators Guide*).

Circuitry on the I/O card detects loss of carrier errors, framing errors, and remote alarms on its incoming T1 stream. It also detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop-timed configurations. The ICC card contains elastic PCM data buffers to minimize slips caused the T1 stream frequency jitter.

Table 3 details the T1 I/O Module's input and output stream specifications.

Table 3: T1 Stream Specifications

Input Stream	
Format	D3/D4 or ESF
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Frequency	1.544 Mbps +/- 76 bps
Impedance	100 Ohms
Output Stream	
Format	D3/D4 or ESF
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Line Equalization (Drive)	0-655 Ft.
Frequency	1.544 Mbps +/- 76 bps
Impedance	100 Ohms %

The combined Framer/LIU performs the following functions:

- Alarm detection (Yellow, Blue, Carrier Lost, Loss of Sync)
- Alarm injection (Yellow & Blue alarms)
- Channel separation
- D4/ESF framing (D4 Superframing and Extended SuperFrame)
- Robbed bit signaling/channel (A, B, C, and D)
- Data transparency
- AMI, B8ZS data encoding

  NOTE: You can use B8ZS for T1 to maintain 1s density (and timing) while providing data transparency.
- Bipolar-to-TTL conversion on the receive side
- Electrical wave shaping on the transmit side
- Clock recovery
- Jitter attenuation, tolerance, and transfer (AT&T 62411 1990)
- Line buildout selection
- Loopback and maintenance functions
- All ones (1s) generation
- Signal monitoring (for loss of signal and quality transmission)

5.0 CONFIGURATION NOTES

There are no jumpers or replaceable PROMs on the I/O Module.

6.0 RELATED DOCUMENTS

For additional information see the ICC card technical description.

Line Test Card-8 (LTC-8)

1.0 GENERAL

The eight-line test card (LTC-8), manufactured by Cisco Systems, Inc., is a Type 1 port interface card that resides in a VCO/4K switch. Up to 3 LTC-8s can be installed in a VCO/4K switch.

Card slots 7 to 21 are assigned to the LTC-8 for a redundant VCO/4K switch, and 5 to 21 for a non-redundant VCO/4K. (An LTC-8 is automatically assigned a set of eight consecutive port addresses when it is entered into the database.)

The LTC-8 provides an interface to eight incoming or outgoing two-wire lines connected directly to telephones, each with a dedicated DTMF receiver and dial pulse detection. It also supports dry loop, dial-up connections from a CO to the systems such as OPX (the LTC-8 supplies office battery). Tip and ring leads are fused. Terminating connections to directly connected stations are supported when a ring generator is connected to the system.

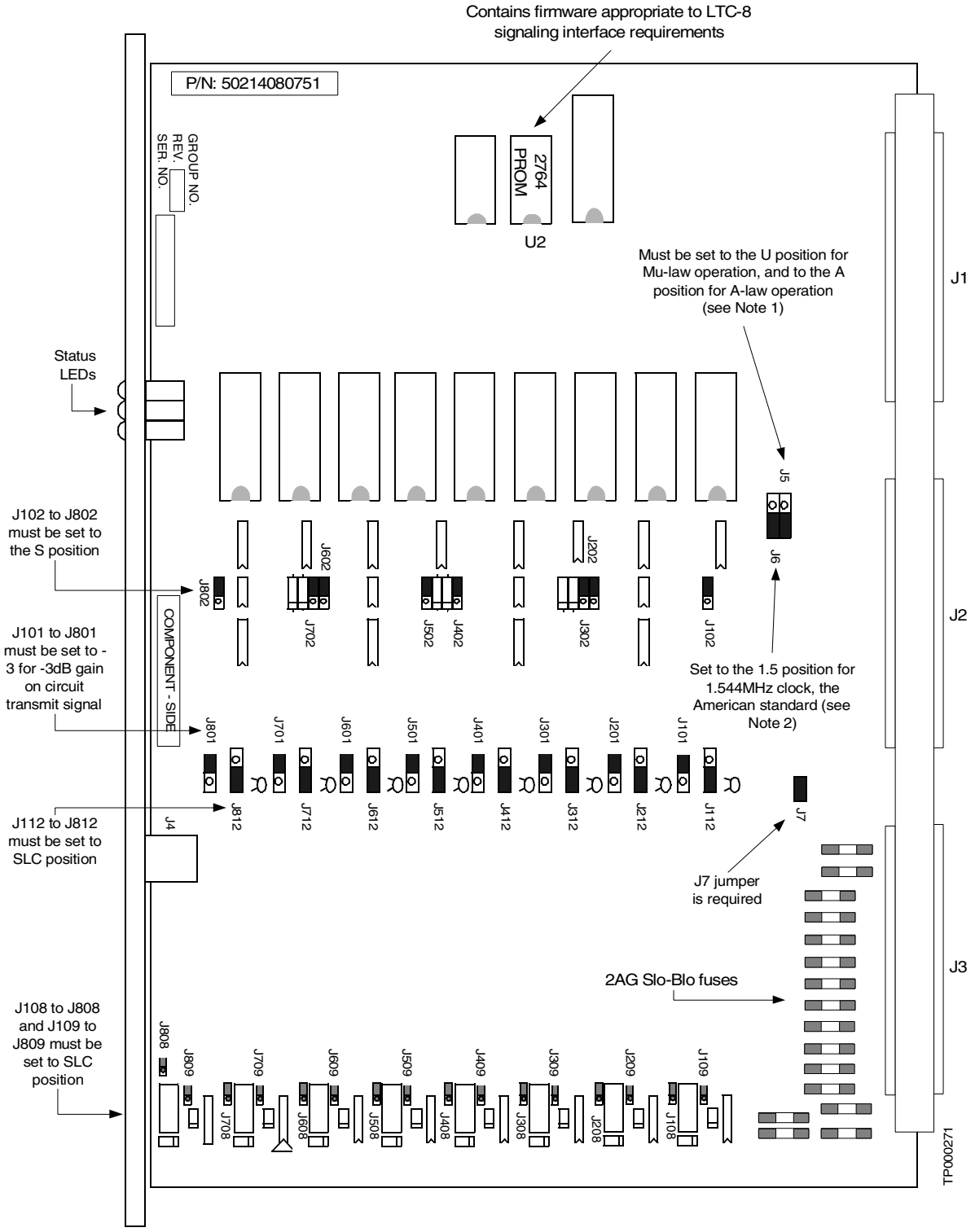
> *NOTE: The LTC-8 gives you an analog type interface for testing in either 2K and 4K mode. The LTC-8 can be used only on the A-bus and B-bus. You cannot connect a voice path to a port on the C-bus.*

2.0 PHYSICAL DESCRIPTION

Jumper plugs on the LTC-8 are factory set for use in a VCO Series switch. *Figure 1* indicates the location and correct installation of jumper plugs on an LTC-8 based on the card's printed circuit board (PCB) revision level. Use this information to verify or reset jumpers on an interface card prior to installing it in the system.

> *NOTE: The circuit card assembly part number, artwork revision level, and serial number are located on the component side of the PCB near the card front panel.*

If a card is improperly configured, it may fail to perform its interface function between external lines/trunks and the system. Therefore, it is important that you verify configuration settings before installing a replacement interface card in the switch.



Note 1: *The setting of jumper J5 to Mu-law or A-law depends on the law setting of the DTG card's tone firmware (refer to the Master Configurator release notes (63098350133). The factory default setting for the J5 jumper is Mu-law*
Note 2: *The NBC3 card is configured with a 1.544HHz clock, and this clock determines and limits the strap settings*

Figure 1: LTC-8 Jumper and PROM Locations

2.1 PCM BUS INTERFACES – J1 PIN ASSIGNMENTS

Table 1 lists the J1 pin assignments on the LTC-8.

> *NOTE: J2 pin assignments are proprietary and are, therefore, not documented for customer use.*

2.2 EXTERNAL INTERFACES - J3 PIN ASSIGNMENTS

The connections to the tip and ring leads of the eight line/trunk interfaces on the LTC-8 are made via the J3 connector (refer to *Figure 2*). A DIN to I/O module adapter attaches to the J3 and terminates the tip/ring connections of up to three LTC-8 cards to a standard RJ21X, 25-pair connector. It is expected that dry line/trunk connections be made via the RJ21X connector to the tip and ring leads of the individual lines/trunks (the LTC-8 provides battery). The J3 pin assignments for each LTC-8 are provided in *Table 2*.

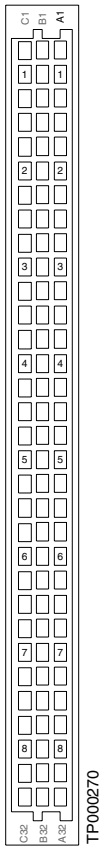


Figure 2: J3 96-PIN DIN Connector

Table 1: J1 Pin Assignments

Pin	Row A1	Row B1	Row C1
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Address Bit 1	Unused	Card Address Bit 0
23	Card Address Bit 3	Unused	Card Address Bit 2
24	Card Address Bit 5	Unused	Card Address Bit 4
25	Card Address Bit 7	Unused	Card Address Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: LTC-8 J3 Pinouts

Pin	Row A1	Row B1	Row C1
1	Unused	Unused	Unused
2	Trunk 1 – Tip	Unused	Trunk 1 – Ring
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – Tip	Unused	Trunk 2 – Ring
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – Tip	Unused	Trunk 3 – Ring
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Trunk 4 – Tip	Unused	Trunk 4 – Ring
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – Tip	Unused	Trunk 5 – Ring
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – Tip	Unused	Trunk 6 – Ring
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Trunk 7 – Tip	Unused	Trunk 7 – Ring
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – Tip	Unused	Trunk 8 – Ring
31	Unused	Unused	Unused
32	Unused	Unused	Unused

3.0 SPECIFICATIONS

Microprocessor	8031 (12 MHz)
Memory	8K Bytes EPROM / 2K Bytes RAM
Power Requirements	+5 Volts – 500 mA (typical); 900 mA (maximum) +15 Volts – 120 mA (typical); 210 mA (maximum) –15 Volts – 125 mA (typical); 230 mA (maximum) +24 Volts – 25 mA (typical); 29 mA (maximum)[a] –48 Volts – 35 mA (typical); 60 mA (maximum)
Trunk Specifications:	
Input Level	0 dB ± 0.5 dBm
Output Level	-3 dB ± 0.5 dBm
Crosstalk Attenuation	68 dB minimum
Idle Circuit Noise	23 dBmc maximum
Line Impedance	600 ohms ± 10%
Echo Return Loss	18 dB minimum (-2 dBm input)
Singing Return Loss:	
Low (200 - 500Hz)	12 dB minimum
High (2500 - 3200Hz)	15 dB minimum
Frequency Response (Signal levels relative to 1004 Hz with C Message Filter):	
60 Hz	-20 dB maximum
300 Hz	-3.0 to 1.0 dB
600 to 2400 Hz	-1.0 to 1.0 dB
3200 Hz	-3.0 to 1.0 dB
Longitudinal Balance:	
200–1000 Hz	60 dB minimum
1000–4000 Hz	50 dB minimum
Loop Current	20 mA minimum / 60 mA maximum
DTMF Receiver:	
Detectable input level	-25 dBm minimum / 1 dBm maximum
Acceptable twist	10 dB maximum
Tone or quiet duration	40 mS minimum

a. Per port current requirements

4.0 CIRCUIT DESCRIPTION

Figure 3 shows a simplified block diagram of the LTC-8. The five major elements of the LTC-8 are:

- Per port circuitry
- Packet processor
- PCM timeslot bus interface
- Control and status registers
- Protective devices

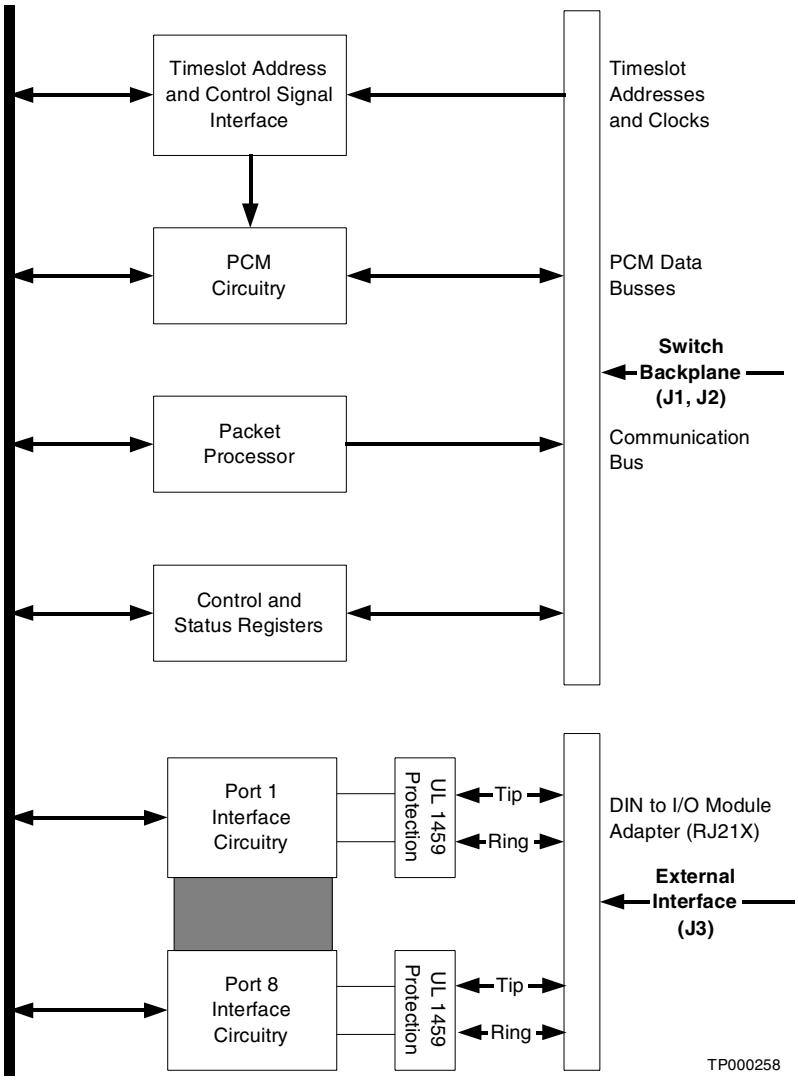


Figure 3: Block Diagram of LTC-8

4.1 PER PORT CIRCUITRY

Each of the eight ports on an LTC-8 includes the following:

- DTMF digit receiver
- Analog to digital encoding and decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On-/off-hook detection
- Relay to attach ring voltage to a line
- Automatic ring relay trip on off-hook
- Tip and ring lead fuses
- Surge protection across tip and ring leads

4.1.1 DTMF Digit Receiver

A DTMF digit receiver integrated circuit (IC) is provided for each LTC-8 port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

4.1.2 Analog to Digital Encoding and Decoding

A 2913 codec provides digital-to-analog and analog-to-digital signal conversion. A codec semi-custom interface IC performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between itself and the codec.

Data received from the PCM busses is latched into parallel in/serial out shift registers internal to the codec interface IC. The codec semi-custom interface IC supplies the data by selecting the output of one of the two internal parallel-to-serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode/decode A-law or Mu-law PCM data. Two jumper areas on the LTC-8 allow selection of the clock frequency and PCM encoding rule for all eight codecs.

4.1.3 Analog Interface

The analog interface consists of the circuitry from the tip and ring leads to the codec. An AMS 2006 Subscriber Line Interface Circuit Hybrid performs the 2-wire to 4-wire conversion, provides internal lightning protection, and drives battery onto the tip and ring leads. The hybrid also monitors the current on the tip and ring leads to determine port on-/off-hook status, and outputs an on-/off-hook status bit. When a port is not terminated (on-hook), the balance network is unbalanced. When this condition exists, an analog signal driven from the codec's receive amplifier into the hybrid is driven back to the input of the codec's transmit amplifier. Jumper area Jx01 allows selection of 0 or -3 dB analog signal outgoing gain.

A DTMF digit receiver IC is connected to the analog signal output by the hybrid and input by the codec's transmit amplifier. A 3.5795 MHz crystal oscillator generates the clock signal required by the DTMF digit receivers.

4.1.4 Control Relay

A relay is provided for each LTC-8 port. When energized, this relay connects ring voltage from the backplane to the port's ring lead, thus ringing a telephone connected to the port. When the telephone goes off-hook, the firmware automatically de-energizes and disables the ring relay to stop the ringing and prevent ring voltage from reconnecting when the telephone goes on-hook.

4.1.5 Tip and Ring Protective Devices

Tip and ring leads of the eight circuits on the LTC-8 are protected from overvoltage and overload conditions as shown in *Figure 4*.

The SIDACtor™ on each port provides transient surge protection from lightning, line transients, and other damaging voltage spikes. This single package device protects against tip-to-ring, tip-to-ground, and ring-to-ground transients. When the monitored voltage exceeds 235Vac, the SIDACtor switches on through a negative resistance region to a low on-state voltage in nanoseconds. It continues to conduct until the current is interrupted or drops below the minimum holding current of the device.

The 2AG Slo-Blo fuses are soldered on to the circuit board and are not field replaceable. If a fuse blows, contact Cisco Systems Customer Response Center to arrange for repair.

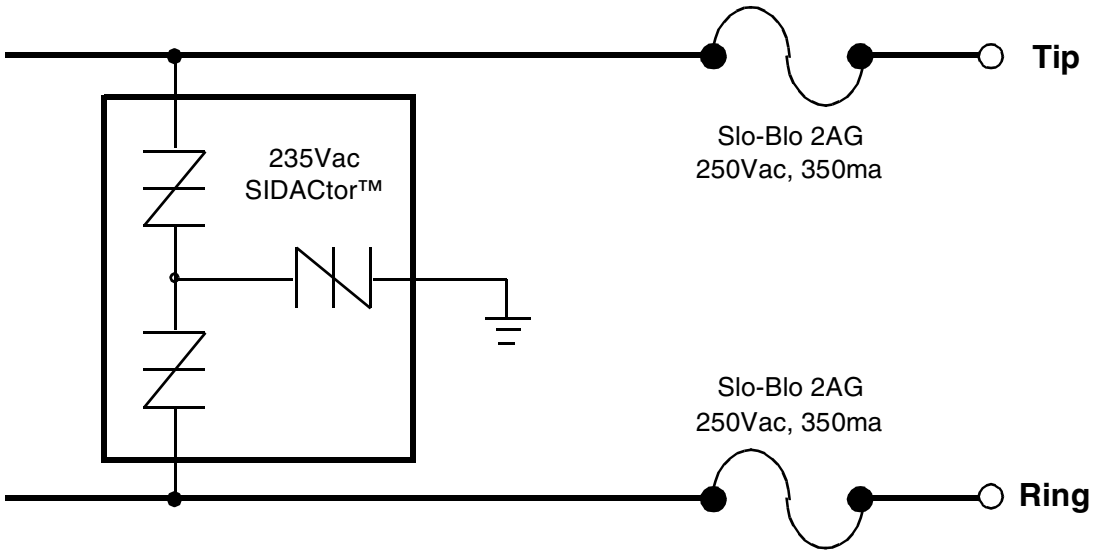


Figure 4: Schematic Diagram of Tip and Ring Protective Devices

4.2 PACKET PROCESSOR

The LTC-8 contains an 8031-based packet processor that interfaces to the communication bus (comm bus). The comm bus is the path by which the packet processor receives commands from, and sends status to, the NBC3. A packet processor is part of all cards in the switch with the exception of the Network Bus Controller (NBC3). The packet processor polls each of the eight line/trunk connections looking for an event (i.e., off-hook detection or valid DTMF digit reception). When polled by the NBC3, the packet processor reports any status change. The packet processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The packet processor also controls three status LEDs (red, yellow, and green) which are visible from the card's front panel.

The packet processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry, the comm bus interface, an asynchronous serial port, and the LED register. The 8031 provides the intelligence for the packet processor and, therefore, for the LTC-8.

4.3 PCM TIMESLOT BUS INTERFACE

All voice data within a system is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the LTC-8 translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The LTC-8 interfaces to the PCM timeslot busses with bus interface circuitry common to several port-oriented circuit cards. Each of the eight port interfaces on the LTC-8 can listen to any timeslot on either PCM data bus.

An LTC-8 is automatically assigned a set of eight consecutive port addresses when it is entered into the database. The PCM data and timeslot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive timeslots. They also control the capture of the correct PCM data for transmission by a particular LTC-8 port.

The PCM busses are functionally equivalent. The transmit timeslot and PCM data bus for a particular port is also used to identify the port when selecting to which timeslot and bus a given port listens.

5.0 SOFTWARE CONFIGURATION

Port configuration refers to the process of specifying appropriate data for each port in the system database. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring an LTC-8 in the system database, refer to the *System Administrator's Guide*.

Class of Service (COS) also greatly affects operation of the card. A COS of T, 2, or A2 sees inward seizures as call originations. A COS of O interprets inward seizures as the port being busied out by the far end. If calls are not being properly processed, check the COS. Refer to the *System Administrator's Guide* for detailed information regarding COS.

> *NOTE: Because of differences in firmware, an LTC-8 cannot be converted to a DID-2 card by reconfiguring jumper settings. Nor can individual ports be set for LTC-8 or DID-2 operation.*

6.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation, and maintenance of the LTC-8 in a VCO/4K switch, refer to the following publications:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- VCO/4K Mechanical Assemblies: VCO Port Subrack
- VCO/4K Card Technical Description: I/O Module

MVDC Programmable T1 Interface Card (MVDC)

1.0 GENERAL

The MVDC Programmable T1 Interface (MVDC-T1) card is a standard port interface circuit card for VCO/4K systems. The MVDC-T1 resides in the master or expansion port subrack. It supports four spans of 24 voice and data channels at 56 Kbps or 64 Kbps, and complies with Bell System DS-1 specifications for transmission at 1.544 Mbps. You can assign incoming, outgoing, and two-way service to 24 individual non-blocking channels on a span.

One or more spans of the MVDC-T1 may be used as an incoming master timing source. For more information about any of the features on the MVDC-T1 card, refer to the *VCO/4K System Administrator's Guide.*

2.0 SPECIFICATIONS

Microprocessor:	(1) MC68360
Memory:	1M DRAM 128K EPROM
Power Requirements:	30 Watts @ 5VDC Max
Input/Output T1 Stream	
Format:	D4 or ESF
Data Encoding:	Alternate Mark Inversion (AMI)
Data Transparency:	Selectable bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, or none
Frequency:	1.544 MHz ± 76 Hz
Impedance:	100 ohms ± 10 ohms

2.1 PROGRAMMABILITY

The application software is downloaded to each span controller enabling independent provisioning of each span as well as each channel. For more information about provisioning spans or channels, refer to the *System Administrator's Guide.*

3.0 CIRCUIT DESCRIPTIION

The MVDC-T1 card controls all 4 spans with one Motorolla MC68360 QUICC (Quad Integrated Communications Controller).

Each span circuit consists of a combination framer/LIU (Line Interface Unit) device. The system controller passes internal commands to the QUICC, which provisions all four framer/ LIU devices. The QUICC monitors the framer and LIU circuitry for alarms or signaling transitions and reports these events back to the system controller.

The LIU section provides both line termination for the received T1 stream, and transmission control (including programmable line buildout) for the outbound T1 stream. Information contained within the T1 channels is passed onto the PCM circuitry.

Figure 1 illustrates a simplified block diagram of the MVDC T1 card.

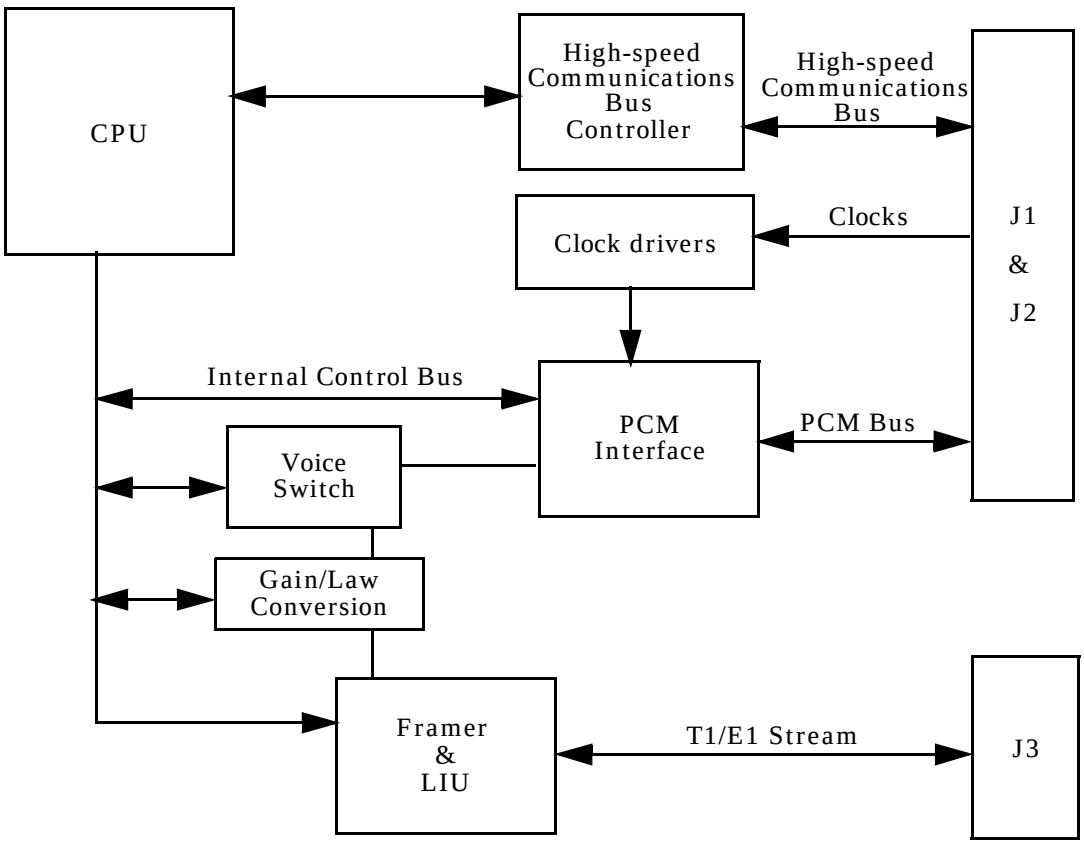


Figure 1: Block Diagram of the MVDC T1 Card

3.1 SHARED CIRCUITRY

The MVDC-T1 card includes the following shared circuitry.

- **Clock drivers:** Provides clock synchronization and reference clock functionality for all four T1 spans.
- **PCM interface:** Provides a common interface to the VCO/4K backplane for all four T1 spans.
- **Gain/Law conversion circuitry:** Provides gain control and law conversion (A- and µ-law) for each span independently for receive and transmit channels.
- **Voice switch:** Provides per timeslot switching capability internal to the MVDC for timeslot routing purposes.
- **High-speed communications bus:** Provides automatic high-speed communications to the system controller when used in conjunction with the NBC-3.

3.2 INDIVIDUAL SPAN CIRCUITRY

The MVDC-T1 card interfaces the VCO/4K system with four T1 digital data carrier streams. Each stream consists of a 1.544 Mbps, 24-channel, bipolar digital data stream. The J3 connector and a compliant connector configuration (RJ45, DB15, and RJ48H types) on the back of the system interface with the digital data stream. You can synchronize the stream with the system clock, the receive clock, or an on-board crystal.

The MVDC-T1 card detects loss of carrier errors, framing errors, and remote alarms on its incoming T1 stream. It detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different, such as in loop timed configurations. The MVDC-T1 card contains elastic PCM data buffers to minimize slips caused the T1 stream frequency jitter.

The combined Line Interface Unit (LIU) and T1 framer provides electronically compliant signal levels.

3.2.1 COMBINED FRAMER/LIU (PER SPAN)

The DS2151 framer/LIU interfaces to a T1, 1.544Mbps digital trunk through the J3 connector.

The interface supports full-duplex transmission of digital data over a 100Ω (T1) balanced T1 transmission line. The interface supports Stratum 4 clocking and also requires a transmit clock of 1.544 MHz ±76 Hz to maintain clock integrity (and therefore data integrity; i.e., 0 bit errors). The combined framer/LIU performs

- Alarm detection (Yellow, Blue, Carrier Lost, Loss of Sync)
- Alarm injection (Yellow & Blue alarms)
- Channel separation
- D4/ESF framing and D4 superframing (in-band, robbed-bit signaling transmission)
- Robbed bit signaling/channel (A, B, C & D)
- Data transparency
- AMI, B8ZS, data encoding

  NOTE: You can use B8ZS for T1 to maintain 1's density (and timing) while providing data transparency.
- Bipolar-to-TTL conversion on the transmit side
- Electrical wave shaping on the receive side
- Clock recovery
- Jitter attenuation
- On board Stratum 4 clocking - AT&T 62411 1990 Stratum 4, Type 2
- Line buildout selection
- Loopback and maintenance functions
- All ones (1s) generation
- Signal monitoring (for loss of signal and quality transmission)

3.3 STANDARDS COMPLIANCE

The MVDC framer/LIU and associated circuitry comply with the following standards:

- AT&T Publication 62411
- Bellcore PUB43801
- TR-NPL-000054
- TR-TSY-000510
- TR-TSY-000191
- ANSI T1.403

3.4 LED STATES

LED indicators appear on the front panel of the MVDC-T1 card.

Table 1 lists the LED states on the MVDC-T1 card.

Table 1: LED States on the MVDC-T1 Card

Card Status	Green	Yellow	Red
Self Test	On	Blinking	Off
Receiving Download	Blinking	Off	Off
Card Failure	On	Off	On
Card OOS[ab]	On	Off	Off
Major Alarm[a]	Off	Off	On
Minor Alarm[a]	Off	On	Off
Card Active	Off	Off	Off

[a] *If one span is OOS and another span has a major alarm, the OOS status takes precedence and the green LED illuminates.*

[b] *If the span status is diagnostics, remote, or payload, the green LED is illuminated.*

3.5 PIN ASSIGNMENTS

Table 2 lists the J3 pin assignments on the MVDC-T1 card.

Table 2: J3 Pin Assignments on the MVDC-T1 Card

Pin	Row A	Row B	Row C
1	Reserved	Unused	Reserved
2	Reserved	Unused	Reserved
3	Reserved	Unused	Reserved
4	Reserved	Unused	Reserved
5	Reserved	Unused	Reserved
6	Reserved	Unused	Reserved
7	Reserved	Unused	Reserved
8	Reserved	Unused	Reserved
9	Reserved	Unused	Reserved
10	Reserved	Unused	Reserved
11	Reserved	Unused	Reserved
12	Reserved	Unused	Reserved

Table 2: J3 Pin Assignments on the MVDC-T1 Card (Continued)

Pin	Row A	Row B	Row C
13	Reserved	Unused	Reserved
14	Reserved	Unused	Reserved
15	Reserved	Unused	Reserved
16	Reserved	Unused	Reserved
17	Reserved	Unused	Reserved
18	Reserved	Unused	Reserved
19	Reserved	Unused	Reserved
20	Reserved	Unused	Reserved
21	Unused	Unused	Unused
22	Rx Line Ring Span 1[a]	Unused	Tx Line Ring Span 1[b]
23	Rcv Line Tip Span 1[a]	Unused	Tx Line Tip Span 1[b]
24	Unused	Unused	Unused
25	Rx Line Ring Span 2[a]	Unused	Tx Line Ring Span 2[b]
26	Rcv Line Tip Span 2[a]	Unused	Tx Line Tip Span 2[b]
27	Unused	Unused	Unused
28	Rx Line Ring Span 3[a]	Unused	Tx Line Ring Span 3 [b]
29	Rcv Line Tip Span 3[a]	Unused	Tx Line Tip Span 3 [b]
30	Unused	Unused	Unused
31	Rx Line Ring Span 4[a]	Unused	Tx Line Ring Span 4 [b]
32	Rcv Line Tip Span 4[a]	Unused	Tx Line Tip Span 4 [b]

[a] *Signal to MVDC-T1 Card.*

[b] *Signal from MVDC-T1 Card*

4.0 REMOVAL/REPLACEMENT PROCEDURES

Follow the directions in the VCO/4K Card Overview to remove or replace an MVDC-T1 card.

CAUTION: Due to the memory retention feature of the MVDC-T1, if you pull the card out and reinsert it in less than one minute, or the NBC-3 resets the card and it becomes operational, the MVDC-T1 may perform one or both of the following:

- **Skip the diagnostics and download**
- **Resume execution where it left off in the application**

Primary Rate Interface/NFAS Card (PRI/N)

1.0 GENERAL

The Primary Rate Interface/NFAS card (PRI/N) is a standard system port interface circuit card that resides in the master or any expansion port subrack. The PRI/N card supports North American Primary Rate connectivity with D-channel protocol handling of the user side and user side symmetrical. It is compatible with Northern Telecom and AT&T implementations of CCITT Q.921 Layer 2 and Q.931 Layer 3 protocols.

> *NOTE: In order to use the PRI/N interface, the system must be equipped with the optional ISDN software package. Refer to the* ISDN Supplement *for more information on this option.*

Standard ISDN PRI consists of 23 B+D channels, where a single signaling channel (D-channel) controls the remaining 23 bearer channels (B-channels) on the interface. Ports 1 through 23 on the PRI/N card (B-channels) are controlled by port 24 (D-channel).

Systems equipped with PRI/N cards can also be installed with optional Non-Facility Associated Signaling (NFAS) software. This option extends D-channel control to B-channels not resident on the same interface. This allows a single D-channel to control up to 20 PRI/N interfaces (a maximum of 479 B-channels). Refer to the *ISDN Supplement* for more information on the NFAS option.

> *NOTE: Users operating V2.04 and V3.00 ISDN software received Primary Rate Interface (PRI) cards to support 23 B+D PRI functionality. As of November 9, 1992, PRI/N cards are shipped as the standard ISDN interface for use with V3.1 and later software. Users can operate both PRI and PRI/N cards within a system. However, PRI cards only support 23 B+D interfaces, while PRI/N cards can be used for 23 B+D and/or NFAS signaling.*

System timing can be synchronized to an internal reference, a selected PRI/N span or an external reference. The system ISDN software option allows administrators to designate primary and secondary master timing links to which the system will be synchronized. If both links fail or the external reference signal is lost, the system defaults to its internal reference clock.

2.0 SPECIFICATIONS

Integrated Multi-Protocol (IMP) Processor
Microprocessor:MC68302 (16 MHz)
Memory:32K Bytes EPROM
4 MBytes DRAM

Power Requirements:	**Typical**
+5 Volts:	1500 mA

Input PRI/N Stream Specifications
Format:D3/D4 or ESF
Data Transparency:B8ZS or none
Frequency:1.544 MHz ± 200 Hz
Impedance:100 ohms ± 10 ohms

Output PRI/N Stream Specifications
FormatD3/D4, ESF
Data Transparency:B8ZS or none
Drive Capability:0 - 655 Feet
Impedance:100 ohms +/- 10 ohms

3.0 CIRCUIT DESCRIPTION

The PRI/N card interfaces a system with a PRI digital data carrier stream. The PRI/N card transmits a D3/D4 or ESF format, 1.544 MHz, 24-channel (23 bearer channels and 1 D-Channel) bipolar or ESF digital data stream. The stream can be synchronized with the system clocks or loop-timed. The PRI/N card receives a data stream of 1.544 MHz (±200 Hz) and can drive a reference clock onto the switch backplane, which the NBC uses synchronization the system clock.

The functions of the PRI/N card are consistent with Layers 1, 2, and 3 of the OSI model to provide the interface with the ISDN D-channel protocols. The NFAS option allows users to designate primary and backup D-channels (D-channel redundancy) for control of an NFAS group.

The PRI/N card detects loss of carrier errors, framing errors, and remote alarms on its incoming PRI stream. It detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop-timed configurations. The PRI/N card contains elastic PCM data buffers to minimize slips caused by PRI/N stream frequency jitter.

Figure 1 is a simplified block diagram of the PRI/N card.

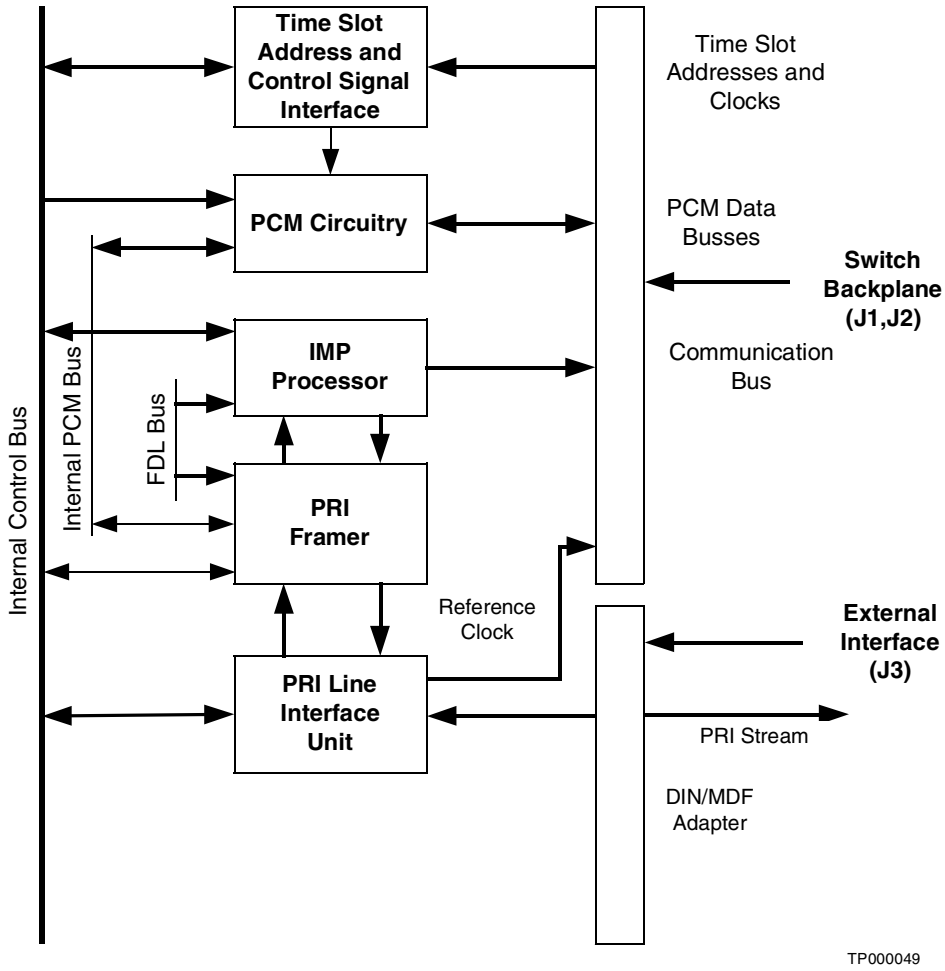


Figure 1: Block Diagram Of PRI/N Card

3.1 OVERVIEW OF CIRCUIT OPERATION

The PRI/N card interfaces with a PRI/N stream. It then frames incoming and outgoing PCM data in accordance with the 23 B+D requirements. All internal operations are controlled by an intelligent processor which is downloaded with ISDN application software upon card power-up. All framing is synchronized to internal or external clock sources as selected in the system data base via the Master Timing Link screen (refer to the *System Administrator's Guide* for more information).

Physical interface to the PRI/N stream is accomplished via a screw-in adapter (proprietary wiring) or an ISO-compliant plug-in adapter that mounts on the rear of the port subrack. The plug-in adapter supports ISO 4903, DA-15S as well as 8-pin modular jack connections to J3 of the PRI/N card.

3.2 PHYSICAL INTERFACE

Physical interface with the PRI/N stream is accomplished through a line interface unit (LIU) and a PRI framer. The Link Layer Task controls and maintains the operation of the LIU and PRI framer.

The LIU performs the following functions:

- Lightening and short-circuit protection
- Clock recovery
- Jitter attenuation
- Bipolar to TTL conversion
- Wave shaping
- Line buildout selection
- Loopback and maintenance functions
- All ones (1s) generation

The PRI/N card supports 23 B+D Extended Super Frame (ESF) or D3/D4 mode. Associated channel signaling is replaced by Common Channel Signaling (CCS) contained in the D-channel. The D-channel contains network and signaling information about the other 23 channels on the span (and additional spans within an NFAS group).

Framing functions are implemented under IMP control via the framer. The framer performs the following functions:

- Alarm detection
- Alarm mode selection
- Channel separation
- FDL maintenance
- Microprocessor interface to link layer statistics
- Serial outputs of D-channels and FDL
- Data transparency

Data transparency is provided by the B8ZS method which requires end-to-end support.

3.3 IMP PROCESSOR

The IMP processor consists of an MC68302 Integrated Multi-Protocol (IMP) processor, memory and Communication Bus circuitry. The IMP controls Link Layer and framer tasks, and coordinates communications along the internal system Communication bus.

3.3.1 MC68302 PROCESSOR

The MC68302 integrates a closely coupled MC68000 microprocessor core with a flexible communications architecture. This processor supports concurrent operation of different protocols through a combination of architectural and programmable features.

A serial communication port (SCP) controls the operation of external line interface unit and PRI framer devices. Its three serial communications controllers (SCCs) are used for ISDN D-channel (HDLC, SCC1), ESF Facility Data Link (HDLC, SCC2) and card front panel port (UART, SCC3).

OSI Layer 2 (Link Layer) and portions of Layer 3 (Network Layer) tasks are executed on the IMP Processor. Figure 2 shows the function/task assignments on PRI/N cards.

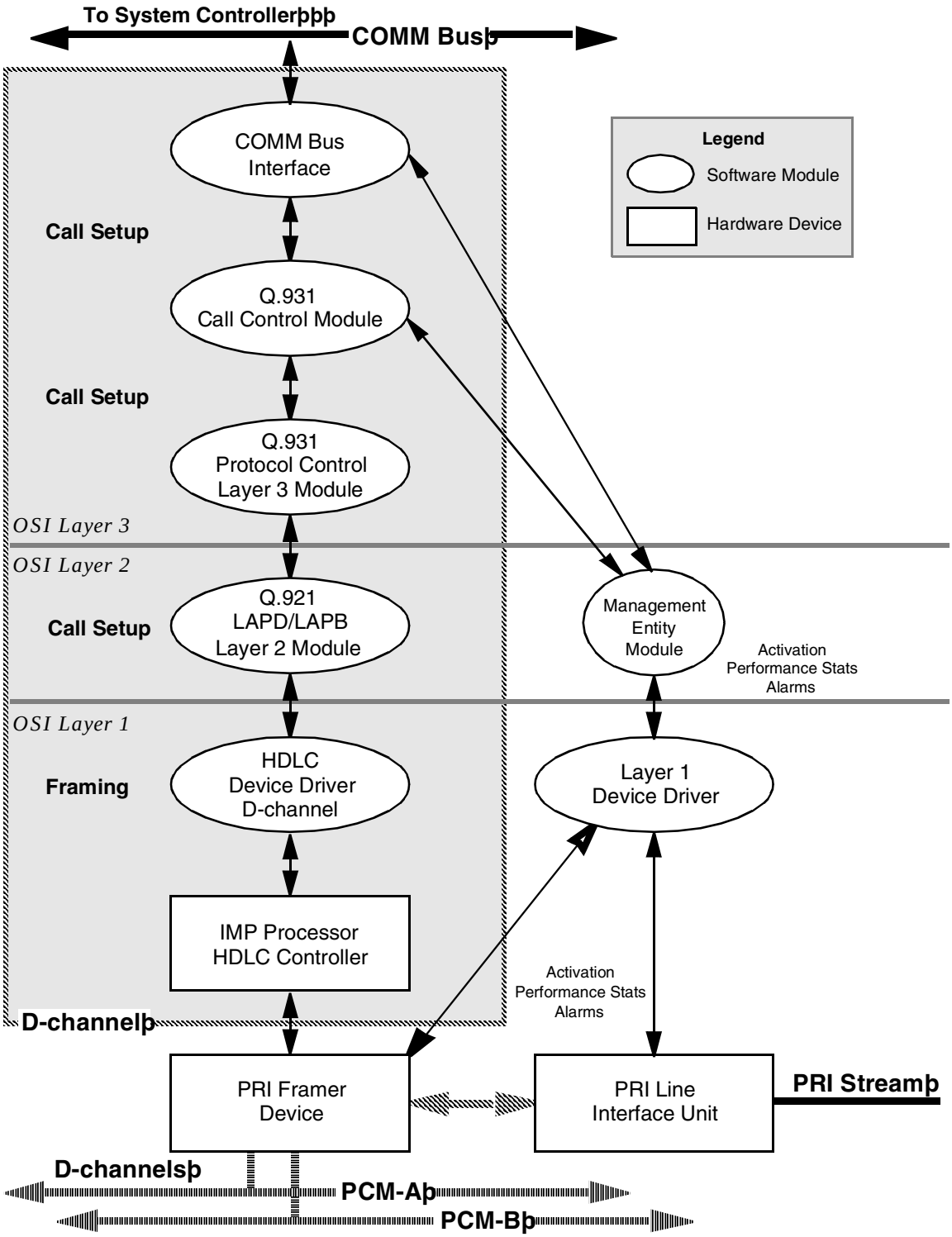


Figure 2: PRI/N Card Hardware Devices & Software Modules

3.3.2 MEMORY

The PRI/N card includes 32 Kbytes of PROM. This nonvolatile memory holds boot firmware, including card initialization and self-diagnostics.

The card also includes 4Mbytes of 80ns dynamic RAM (DRAM). Following power up, application software controlling OSI Layer 2 and Layer 3 is downloaded over the system communication bus to DRAM. The IMP executes these programs from static memory.

3.3.3 SERIAL COMMUNICATION CONTROLLERS

SCC1 is configured as a full duplex HDLC (High Level Data Link Control) port for handling the ISDN D-channel data. Data is synchronously transmitted and clocked at an effective data rate of 64 Kbps. The SCC1 transmitter is always enabled so as to keep the outbound data buffer loaded with D-channel data or flag sequences. The receiver is always enabled and synchronized with a receive clock at 1.544 Mbps. The receive clock is also gated to receive 8 bits of data from the D-channel every 125µS for an effective data rate of 64 Kbps.

SCC2 is configured as a full duplex HDLC port for handling the 4 Kbps facility data link (FDL) used for ESF maintenance information.

SCC3 is configured as a half-duplex, 2400 bps UART port connected to the front panel (J4) jack. It serves as an RS-232C diagnostic port.

> *NOTE: The front panel jack on the PRI/N card is not intended for customer use. This jack provides a diagnostic port used by Cisco Systems Technical Support only.*

3.3.4 OSI LAYER 2 FUNCTIONS

The PRI/N card uses one HDLC channel (SCC1) as the D-channel. D-channel termination at Layer 2 requires implementation of CCITT Link Access Procedure – D-Channel Q.921, commonly referred to as LAPD. LAPD is downloaded to the PRI/N card on power up and run as a Link Layer task on the IMP processor.

LAPD functions include:

- HDLC protocol communications
- Parameter negotiation
- Data link establishment
- Sequenced I-frame transfer
- Error handling

3.3.5 OSI LAYER 3 FUNCTIONS

The D-channel termination at Layer 3 requires the implementation of CCITT Q.931 Protocol/-Call Control. Q.931 is run as a Network Layer task on the IMP processor. The following functions are implemented by the Network Layer task:

- Data link establishment
- Call setup/teardown
- Call reference selection
- Application interface

Some portions of Q.931, such as D-channel selection, are performed in the system controller. Messages received through Layer 3 are passed via the communication bus to higher layers implemented in the generic software and/or host application. Signaling and maintenance commands sent down from the system controller are transmitted over the communication bus and through Layer 3 and the lower layers for ultimate transmission on the D-channel.

A management task runs parallel to the protocol tasks and collects link statistics. These statistics are sent via the communications bus for use by the generic software. The following statistics are monitored by the management task:

- Out-Of-Frame (OOFs) and slips
- D-channel in-service, out-of-service, and maintenance modes
- D-channel in-service and out-of-service modes
- Alarming (Yellow)

3.3.6 IMP SOFTWARE

For compatibility with a specific type of switching equipment, such as AT&T 4ESS or Northern Telecom DMS-100, the PRI/N software is configured with the correct command set. A run-time switch that defines the PRI/N card's personality is set through the PRI Card Configuration and PRI Card Protocol system administration screens (refer to the *System Administrator's Guide* for more information). Various digital switch personalities are accommodated by the PRI/N download software.

3.4 PRI FRAMER

The DS2180 framer interfaces to a DS1, 1.544 Mbps digital trunk through the LIU. It supports the D3/D4 and Extended Superframe (ESF) standards and provides clear channel capability through appropriate zero suppression and signaling modes. System 1s density is maintained through B8ZS (Bipolar Eight Zero Substitution) coding. B8ZS coding replaces eight consecutive outgoing zeros with a B8ZS code word.

The transmit framer/formatter circuits generate appropriate framing bits, supervise zero suppression, generate alarms, and provide output clocks for data conditioning and decoding. The receiver/synchronizer circuits establish frame and multiframe boundaries, extract signaling data, and report alarms and signaling formats.

3.5 LINE INTERFACE UNIT

The LIU employed on the PRI/N card (CS61575 or LXT305) is a fully integrated transceiver designed for North American (μ-law), T1 (1.544 Mbps) operation. It performs line driver, data recovery, and clock recovery functions. The LIU supports full-duplex transmission of digital data over twisted-pair installations. Programmable equalization via the PRI Configuration Screen is provided for line length of 0 to 655 feet (refer to the *System Administrator's Guide* for more information).

3.6 PRI/N CARD LED STATES

Table1 lists front panel LED states for PRI/N cards and their meaning. Note that these states are unique to ISDN interface cards. The following general signaling conditions apply to each LED.

- *Red (top) LED* – illuminates continuously to signal a problem with an inward PRI/N stream (carrier loss, OOF or D-channel failure).
- *Yellow (center) LED* – illuminates to signal that a Yellow Alarm has been detected on the incoming PRI/N stream (remote alarm), or that the card has not been polled for two seconds by the NBC.
- *Green (bottom) LED* – not used for alarming. Illuminates continuously until the base address of the card has been assigned by the system.

Table 1: PRI/N Card LED States

PRI Card LEDs			System Alarm	Condition	Card State	Outward Action
Red	Yellow	Green				
OFF	OFF	OFF	None	Normal	Active	Call processing is occurring
			Minor (FRM287)	Slip threshold exceeded	*Maintenance*[a]	None
			Minor (FRM292)	OOF threshold exceeded	*Maintenance*[a]	None
OFF	**ON**	OFF	Minor (FRM286)	Remote Alarm	Maintenance	None
			Minor	COMM Bus Polling Failure	Normal	None
ON	OFF	OFF	Major (FRM285)	Loss fo Carrier	Maintenance	Sending Yellow Alarm
			Minor (FRM284)	OOF Error	Maintenance	Sending Yellow Alarm
			None (FRM295)	D Channel Failure	Maintenance	None
			Major (FRM296)	T309 Timeout	Maintenance	None
ON	**ON**	OFF	Major	Following Card Reset	Maintenance	None
OFF	OFF	**ON**	Minor (FRM281)	Out-Of-Service (OOS)	OOS	None

a. Applies to system with Manual Intervention for SLIP/OOFS feature flag set to Y (Yes).

- *If an Active PRI/N card is placed into Maintenance via master console, any calls in progress are completed and no new calls are accepted. Calls are not torn down unless the individual port is taken out of service, Restart is received, T309 expires, or there is a loss of carrier condition.*
- *If multiple conditions force a card into Maintenance state, the card will not become active until all error conditions are cleared.*
- *If the Manual Intervention for SLIP/OOFS flag is set to "N", slips may be occurring even though the card is Active and no LEDS are illuminated. The maintenance threshold for OOFs is ignored and the PRI/N card will cycle in and out of Maintenance as the OOF condition is detected and cleared.*
- *Slip and OOF counters are automatically zeroed at midnight.*

3.7 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 2 lists the pin assignments for J1 on the PRI/N card.

NOTE: J2 pin assignments are proprietary and are, therefore, not documented for customer use.

Table 2: PRI/N Card J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	–24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4

Table 2: PRI/N Card J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	Unused	Unused	Unused
30	AGND	Unused	AGND
31	AGND	Unused	AGND
32	DGND	Unused	DGND

3.8 EXTERNAL INTERFACES

Connections to the incoming and outgoing PRI/N digital data streams are made via the J3 connector. A DIN to MDF adapter attaches to the J3 connector and allows external connection to the PRI/N card via a 15-position, sub-D type connector or an RJ45. A male sub-D type connector is provided on the system MDF Adapter. J3 connector pinouts are listed in Table 3.

Table 3: PRI/N Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Digital Ground
2	Unused	Unused	Reserved
3	Unused	Unused	Rcv Line Tip[1]
4	Unused	Unused	Rcv Line Ring[1]
5	Unused	Unused	Xmt Line Tip[2]
6	Unused	Unused	Xmt Line Ring[2]
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Unused	Unused	Unused
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused

Table 3: PRI/N Card J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
14	Unused	Unused	Unused
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Unused	Unused	Unused
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Unused	Unused	Unused
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Unused	Unused	Unused
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	GND
30	Unused	Unused	SCC3 UART Xmt
31	Unused	Unused	SCC3 UART Rcv
32	Unused	Unused	Unused

1 Signal to PRI/N Card.

2 Signal from PRI/N Card

The J3 to D connector pinouts are shown in Figure 4 and Table 4.

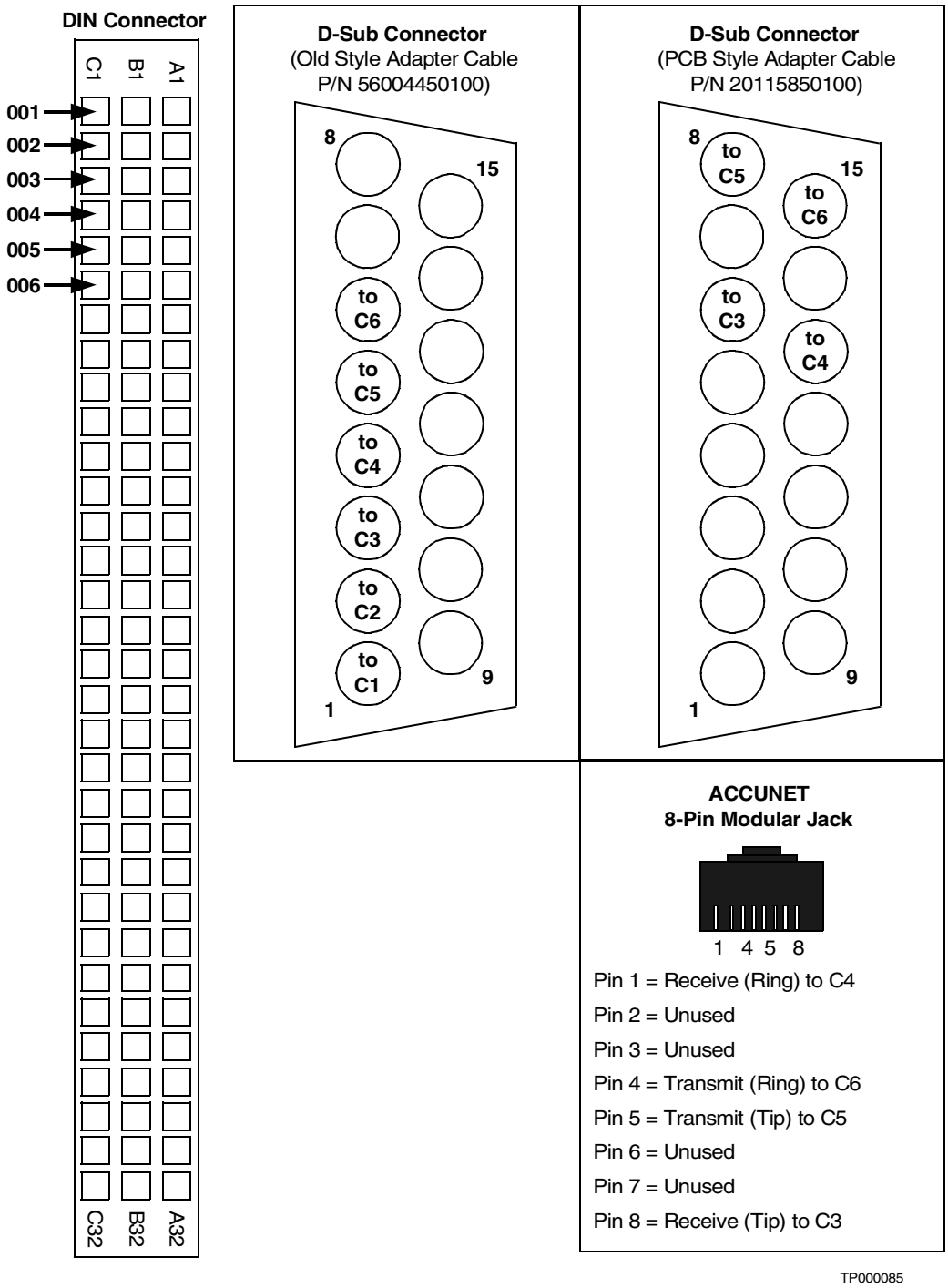


Figure 3: Pin Out diagram of T1 & PRI/N Adapters

NOTE: *20115850100 is the part number for the entire PCB Style Adapter assembly. A different number (50191050100) may be etched on the Adapter's PCB. The etched number is the part number for the PCB only. Use the assembly number when ordering a new Adapter.*

Table 4: PRI/N Card J3 To D-Connector/Modular Jack Pinouts

Screw-In T1 & PRI/N Adapter Cable P/N 56004450100 (Old style cable for 2-row back plane)			
J3 Pin	**D-Connector Pin**	**Signal Name**	
1C	1	Digital Ground	
2C	2	Reserved	
3C	3	Receive Line Tip (to card)	
4C	4	Receive Line Ring (to card)	
5C	5	Transmit Line Tip (from card)	
6C	6	Transmit Line Ring (from card)	
Plug-In T1 & PRI/N Adapter P/N 20115850100 (PCB style for 3-row back plane)			
J3 Pin	**D-Connector Pin[a]**	**Modular Jack**	**Signal Name**
1C	Not Connected	Not Connected	Digital Ground
2C	Not Connected	Not Connected	Reserved
3C	1	8	Receive Line Tip (to card)
4C	9	1	Receive Line Ring (to card)
5C	3	5	Transmit Line Tip (from card)
6C	11	4	Transmit Line Ring (from card)

a. DA-15S, ISO 4903

3.9 LINE EQUALIZATION

The PRI/N card provides a programmable pre-emphasis equalizer to balance its transmit stream according to the length of the cable being driven. The equalization factors apply to ABAM cable comprised of two individually-shielded twisted pairs, 22AWG conductors.

The ISDN software supplied with the PRI/N card includes a configuration screen for setting line equalization on a per card basis. Refer to the *ISDN Supplement* supplied with the software for details.

3.10 DIP SWITCH

An eight-position DIP switch on the PRI/N card is not used for this application. All eight switches should be set to the **Open** position.

4.0 CONFIGURATION NOTES

The PRI/N card is manufactured by Cisco Systems, Inc. Figure 5 indicates the location of factory set jumpers.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

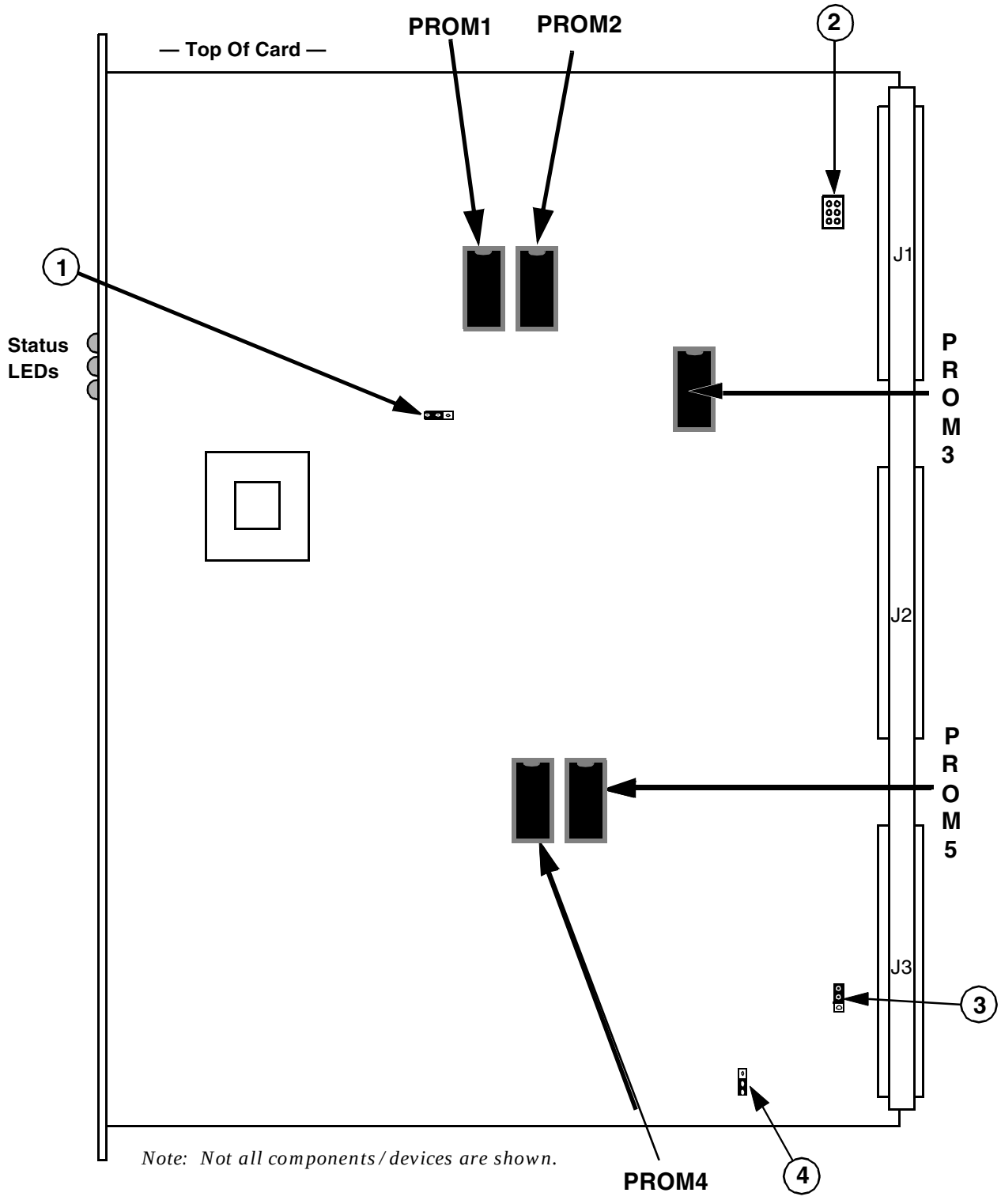
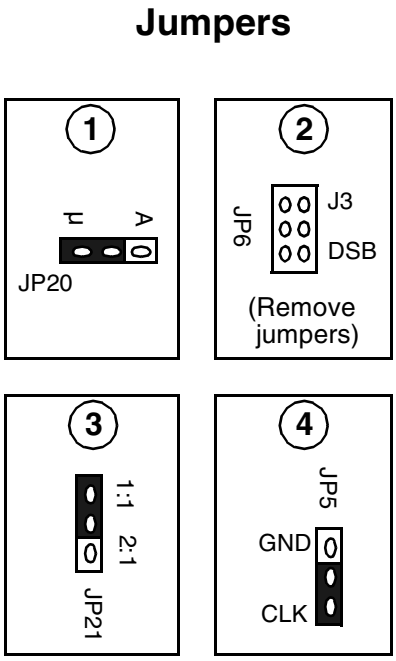


Figure 4: PRI/N Card Jumper Locations

Refer to Figure 5 to verify jumper settings prior to installing the PRI/N card in a Port Subrack.



PROM Listing

PROM1
PRI F/W EVEN

PROM2
PRI F/W ODD

PROM3
32-CH PATH SETUP

PROM4
TX PCM GAIN/LAW

PROM5
RX PCM GAIN/LAW

Figure 5: PRI/N Jumper Settings

If a card is improperly configured, it may fail to perform its interface function between external spans and the system. Therefore, be sure to verify configuration settings, hardware jumpers, and data base entries, before installing a replacement interface card in the system.

Port configuration refers to the process of specifying appropriate data for each port in the system data base, including line equalization. If the port is improperly configured, the system may improperly interpret the incoming PRI stream. For additional information on configuring a PRI/N card in the system data base, refer to the *ISDN Supplement*.

5.0 REMOVAL/REPLACEMENT PROCEDURES

Follow the directions in the VCO/4K Card Overview to remove or replace a PRI/N card.

> *NOTE: When a PRI/N card is replaced in the port subrack, it begins a self-test. The only Out of Service indication is a green LED. Use the Card Maintenance screen to change the card to Active status. A directed download of the application now occurs. When the download is complete, the card is automatically brought into service. Appropriate system messages are displayed on the master console and logged in the system error log.*

6.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the PRI/N card, refer to the following publications.

- ISDN Supplement
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide

Subscriber Line Interface Card (SLIC-2)

1.0 GENERAL

The Subscriber Line Interface Card (SLIC-2) is a standard port interface circuit card that resides in the Master or any Expansion Port Subrack. The SLIC-2 provides interface to eight incoming or outgoing 2-wire lines connected directly to telephones, each with a dedicated DTMF receiver and dial pulse detection. It also supports dry loop, dial-up connections from a CO to the systems such as OPX, the SLIC-2 supplies office battery. Tip and Ring leads are fused. Terminating connections to directly connected stations are supported when a ring generator is connected to the system.

2.0 SPECIFICATIONS

Microprocessor	8031 (12 MHz)
Memory	8K Bytes EPROM 2K Bytes RAM
Power Requirements	+5 Volts – 500 mA (typical); 900 mA (maximum) +15 Volts – 120 mA (typical); 210 mA (maximum) –15 Volts – 125 mA (typical); 230 mA (maximum) +24 Volts – 25 mA (typical); 29 mA (maximum)[a] –48 Volts – 35 mA (typical); 60 mA (maximum)
Trunk Specifications	þþ
Input Level	0 dB ± 0.5 dBm
Output Level	-3 dB ± 0.5 dBm
Crosstalk Attenuation	68 dB minimum
Idle Circuit Noise	23 dBmc maximum
Line Impedance	600 ohms ± 10%
Echo Return Loss	18 dB minimum (-2 dBm input)
Singing Return Loss	
Low (200 - 500Hz)	12 dB minimum
High (2500 - 3200Hz)	15 dB minimum

Frequency Response (Signal levels relative to 1004 Hz with C Message Filter)	
60 Hz	-20 dB maximum
300 Hz	-3.0 to 1.0 dB
600 to 2400 Hz	-1.0 to 1.0 dB
3200 Hz	-3.0 to 1.0 dB
Longitudinal Balance	
200–1000 Hz	60 dB minimum
1000–4000 Hz	50 dB minimum
Loop Current	20 mA minimum 60 mA maximum
DTMF Receiver	
Detectable input level	-25 dBm minimum 1 dBm maximum
Acceptable twist	10 dB maximum
Tone or quiet duration	40 mS minimum

a. Per port current requirements

CAUTION: This version of the SLIC-2 may be used interchangeably in listed (UL 1459) and non-listed systems. However, earlier versions of the SLIC (P/N 50174060300 or 50174080300) cannot be used in listed systems.

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the SLIC-2. The five major elements of the SLIC-2 are:

- Per Port Circuitry
- PCM Time Slot Bus Interface
- Packet Processor
- Control & Status Registers
- Protective Devices

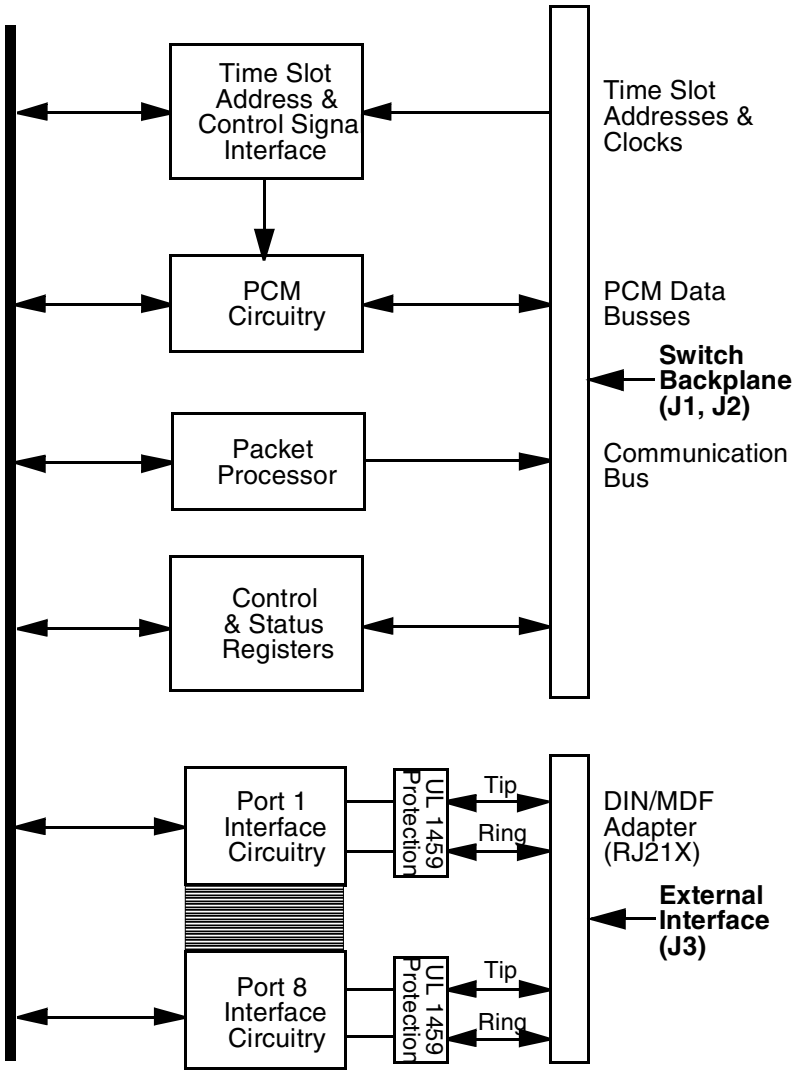


Figure 1: Block Diagram Of SLIC-2

3.1 PER PORT CIRCUITRY

Each of the eight ports on a SLIC-2 includes the following:

- DTMF Digit Receiver
- Analog to Digital Encoding and Decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On/Off hook detection
- Relay to attach ring voltage to a line
- Automatic ring relay trip on off-hook
- Tip and Ring lead fuses
- Surge protection across Tip and Ring leads.

3.1.1 DTMF DIGIT RECEIVER

DTMF digit receiver integrated circuit (I.C.) is provided for each SLIC-2 port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

3.1.2 ANALOG TO DIGITAL ENCODING & DECODING

A 2913 codec provides digital-to-analog and analog-to-digital signal conversion. A codec semi-custom interface I.C. performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between itself and the codec.

Data received from both PCM busses is latched into parallel in/serial out shift registers internal to the codec interface I.C. The codec semi-custom interface I.C. supplies the data by selecting the output of one of the two internal parallel-to-serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode/decode A-law or µ-law PCM data. Two jumper areas on the SLIC-2 allow selection of the clock frequency and PCM encoding rule for all eight codecs.

3.1.3 ANALOG INTERFACE

The analog interface consists of the circuitry from the tip and ring leads to the codec. An AMSþ2006 Subscriber Line Interface Circuit Hybrid performs the 2-wire to 4-wire conversion, provides internal lightning protection, and drives battery onto the tip and ring leads. The hybrid also monitors the current on the tip and ring leads to determine port on/off hook status, and outputs an on/off hook status bit. When a port is not terminated (on hook), the balance network is unbalanced. When this condition exists, an analog signal driven from the codec's receive amplifier into the hybrid is driven back to the input of the codec's transmit amplifier. Jumper area Jx01 is provided to allow analog signal outgoing gain selection of 0 or -3 dB.

A DTMF digit receiver I.C. is connected to the analog signal output by the hybrid and input by the codec's transmit amplifier. A 3.5795 MHz crystal oscillator is provided to generate the clock signal required by the DTMF digit receivers.

3.1.4 CONTROL RELAY

A relay is provided for each SLIC-2 port. When energized, this relay connects ring voltage from the backplane to the port's Ring lead thus ringing a telephone connected to the port. When the telephone goes offhook, the firmware automatically de-energizes and disables the ring relay to stop the ringing and prevent ring voltage from reconnecting when the telephone goes onhook.

3.1.5 TIP & RING PROTECTIVE DEVICES

Tip and Ring leads of the eight circuits on the SLIC-2 are protected from overvoltage and overload conditions as shown in Figure 2 below.

The SIDACtor™ on each port provides transient surge protection from lightning, line transients and other damaging voltage spikes. This single package device protects against Tip to Ring, Tip to Ground, and Ring to Ground transients. When the monitored voltage exceeds 235Vac, the SIDACtor switches on through a negative resistance region to a low on-state voltage in nanoseconds. It continues to conduct until the current is interrupted or drops below the minimum holding current of the device.

The 2AG Slo-Blo fuses are soldered into the circuit board and are not field replaceable. If a fuse blows, contact Cisco Systems Technical Support to arrange for repair.

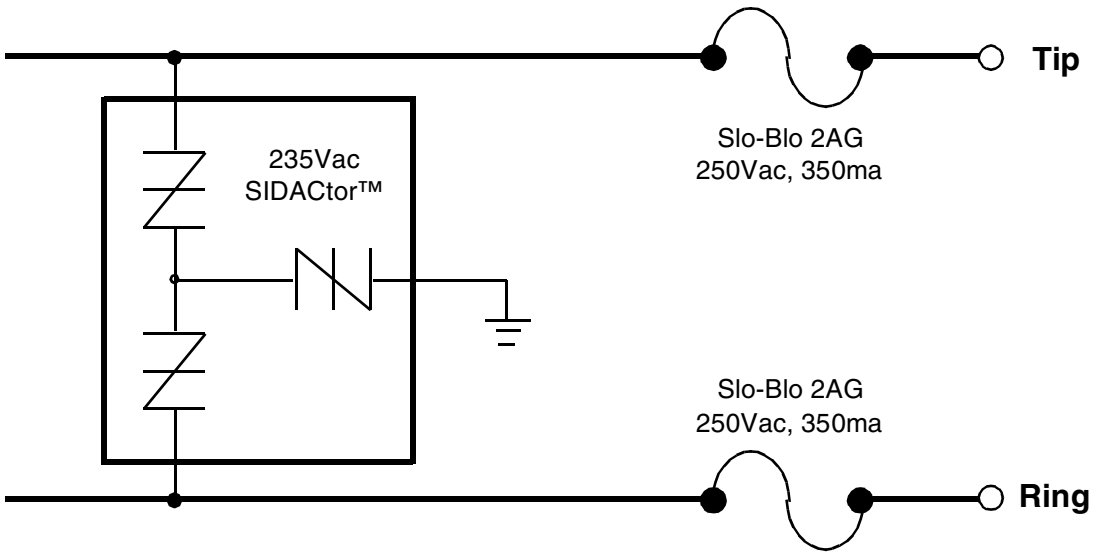


Figure 2: Schematic Diagram Of Tip & Ring Protective Devices

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within a system is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the SLIC-2 translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The SLIC-2 interfaces to the dual PCM time slot busses with bus interface circuitry common to several port-oriented circuit cards. Each of the eight port interfaces on the SLIC-2 can listen to any time slot on either PCM data bus.

A SLIC-2 is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular SLIC-2 port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The SLIC-2 contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC). The Packet Processor polls each of the eight line/trunk connections looking for an event (i.e. off hook detection or valid DTMF digit reception). When polled by the NBC, the Packet Processor reports any status change. The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry, the Communication Bus Interface, an asynchronous serial port, and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the SLIC-2

The Communication Bus is the path by which the Packet Processor receives commands from and sends status to the Network Bus Controller.

3.4 PCM BUS INTERFACES – J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the SLIC-2.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.5 EXTERNAL INTERFACES

The connections to the Tip and Ring leads of the eight line/trunk interfaces on the SLIC-2 are made via the J3 connector. A DIN to MDF adapter attaches to J3 and terminates the tip/ring connections of up to three SLIC-2s to a standard RJ21X, 25-pair connector. It is expected that dry line/trunk connections be made via the RJ21X connector to the tip and ring leads of the individual lines/trunks (SLIC-2 provides battery). The J3 pin assignments for each SLIC-2 card are provided in Table 2. J3 to RJ21X pinouts are shown in Table 3 and Figure 4.

Table 1: J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2

Table 1: J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: SLIC-2 J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Unused
2	Trunk 1 – Tip	Unused	Trunk 1 – Ring
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – Tip	Unused	Trunk 2 – Ring
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – Tip	Unused	Trunk 3 – Ring
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Trunk 4 – Tip	Unused	Trunk 4 – Ring
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – Tip	Unused	Trunk 5 – Ring
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – Tip	Unused	Trunk 6 – Ring
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused

Table 2: SLIC-2 J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
26	Trunk 7 – Tip	Unused	Trunk 7 – Ring
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – Tip	Unused	Trunk 8 – Ring
31	Unused	Unused	Unused
32	Unused	Unused	Unused

Table 3: J3 To RJ21X Pinouts

Card	Trunk	Tip Lead	Ring Lead
1	1	J3-2A to RJ21X-26	J3-2C to RJ21X-1
1	2	J3-6A to RJ21X-27	J3-6C to RJ21X-2
1	3	J3-10A to RJ21X-28	J3-10C to RJ21X-3
1	4	J3-14A to RJ21X-29	J3-14C to RJ21X-4
1	5	J3-18A to RJ21X-30	J3-18C to RJ21X-5
1	6	J3-22A to RJ21X-31	J3-22C to RJ21X-6
1	7	J3-26A to RJ21X-32	J3-26C to RJ21X-7
1	8	J3-30A to RJ21X-33	J3-30C to RJ21X-8
2	1	J3-2A to RJ21X-34	J3-2C to RJ21X-9
2	2	J3-6A to RJ21X-35	J3-6C to RJ21X-10
2	3	J3-10A to RJ21X-36	J3-10C to RJ21X-11
2	4	J3-14A to RJ21X-37	J3-14C to RJ21X-12
2	5	J3-18A to RJ21X-38	J3-18C to RJ21X-13
2	6	J3-22A to RJ21X-39	J3-22C to RJ21X-14
2	7	J3-26A to RJ21X-40	J3-26C to RJ21X-15
2	8	J3-30A to RJ21X-41	J3-30C to RJ21X-16
3	1	J3-2A to RJ21X-42	J3-2C to RJ21X-17
3	2	J3-6A to RJ21X-43	J3-6C to RJ21X-18
3	3	J3-10A to RJ21X-44	J3-10C to RJ21X-19
3	4	J3-14A to RJ21X-45	J3-14C to RJ21X-20
3	5	J3-18A to RJ21X-46	J3-18C to RJ21X-21
3	6	J3-22A to RJ21X-47	J3-22C to RJ21X-22
3	7	J3-26A to RJ21X-48	J3-26C to RJ21X-23

Table 3: J3 To RJ21X Pinouts (Continued)

Card	Trunk	Tip Lead	Ring Lead
3	8	J3-30A to RJ21X-49	J3-30C to RJ21X-24

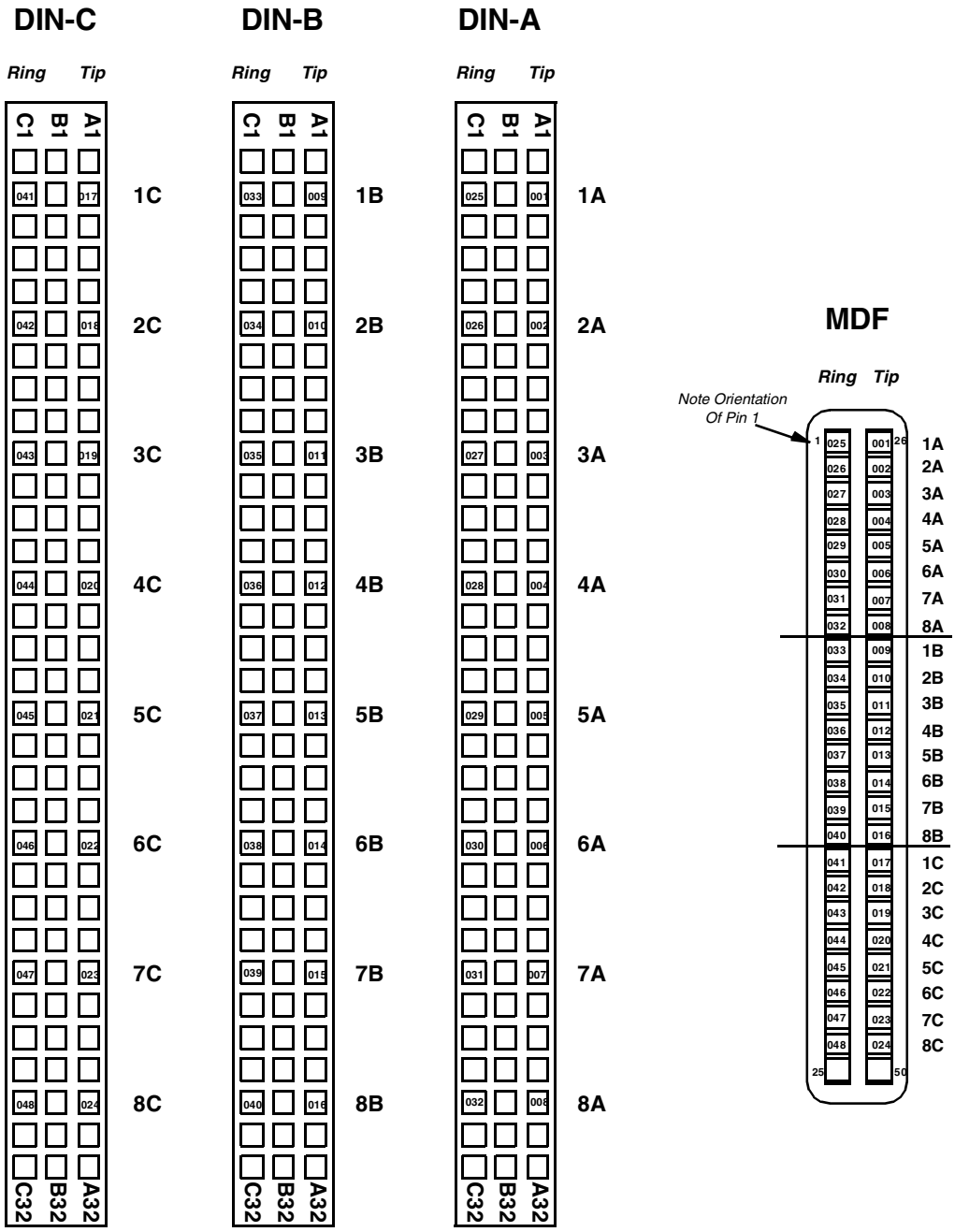


Figure 3: Pin-Out Diagram Of DIN–RJ21X MDF Adapter

4.0 CONFIGURATION NOTES

The SLIC-2 is manufactured by Cisco Systems, Inc. Jumper plugs on the SLIC-2 are factory set for use in systems. Figure 5 indicates the location and correct installation of jumper plugs on a SLIC-2 based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it in a Port Subrack.

> *NOTE: The artwork revision level for the PCB itself (unpopulated) is etched on the solder side of the board near the front panel. The circuit card assembly part number, revision level and serial number appear on the component side of the PCB near the card front panel. The assembly part number includes four characters indicating the revision level. The first three characters are the actual revision level. The final letter "R" indicates that the PCB is at Release level. For example, a revision level A0L card is marked as Rev. "A0LR".*

If a card is improperly configured, it may fail to perform its interface function between external lines/trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a SLIC-2 in the system data base, refer to the *System Administrator's Guide.*

Class of Service (COS) also greatly affects operation of the card. A COS of T, 2, or A2 sees inward seizures as call originations. A COS of O interprets inward seizures as the port being busied out by the far end. If calls are not being properly processed, check the COS.

> *NOTE: Because of differences in firmware, a SLIC-2 cannot be converted to a DID-2 card by reconfiguring jumper settings. Nor can individual ports be set for SLIC-2 or DID-2 operation.*

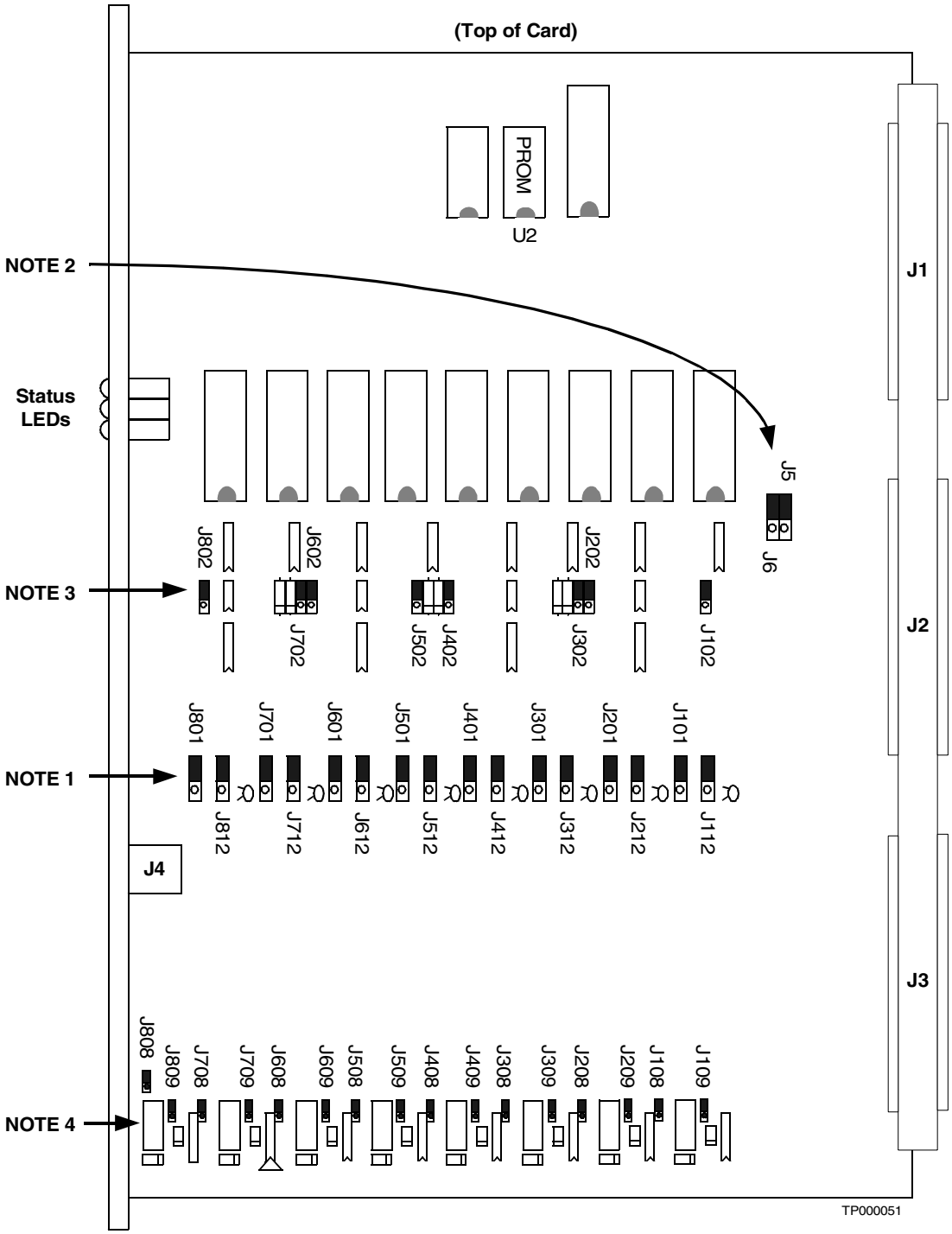


Figure 4: SLIC-2 Jumper & PROM Locations

Subscriber Line Interface Card-2 – PCB P/N 50214200000 Rev. 0AR

Jumper Locations

NOTE 1

- Jumpers at J101 through J801 must be set to -3 for -3dB gain on circuit transmit signal (8þjumpers).
- Jumpers at J112 through J812 must be set to SLC for SLIC-2 operation (8þjumpers).

NOTE 2

- Install jumper plug at J5 in the U position for codec µlaw operation (North American standard).
- Install jumper plug at J5 in the A position for codec A-law operation (European standard). Position U (µlaw) is the factory default setting for J5.
- Install the jumper plug at J6 in the 1.5 position for 1.544MHz codec clock (North American standard).
- Install the jumper plug at J6 in the 2.0 position for 2.048MHz codec clock (European standard). Position 1.5 (1.544MHz) is the factory default setting for J6.

NOTE 3

- Jumpers at J102 through J802 must be set to S position for SLIC-2 operation (8þjumpers).

NOTE 4

- Jumpers at J108 through J808 and J109 through J809 must be set to SLC position for SLIC-2 operation (2 X 8 =16 jumpers).

PROM

The 2764 PROM in location U2 contains firmware appropriate to SLIC-2 signalling interface requirements.

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the SLIC-2, refer to the following publications.

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- VCO/4K Mechanical Assemblies: VCO Port Subrack
- VCO/4K Technical Description: VCO Plug-In MDF Adapters

T1 Interface Card (T1)

1.0 GENERAL

The T1 Interface (T1) card is a standard port interface circuit card that resides in the master or any expansion port subrack. It supports 24, 56Kbps voice channels and complies with Bell System DS-1 specifications for transmission at 1.544Mps. Each T1 card may have up to 24 non-blocking channels assigned to incoming, outgoing and/or 2-way service on a channel-by-channel basis using administrative software.

System timing can be synchronized to an internal reference, a selected T1 span or an external reference. Generic software allows administrators to designate primary and secondary master timing links (T-spans) to which the system will be synchronized. If both links fail or the external reference signal is lost, the system defaults to its internal reference clock.

2.0 SPECIFICATIONS

Table 1: T1 Card Specifications

Specification	Description or Value
packet processor	
Microprocessor	8032 (12 MHz)
Memory	8K Bytes EPROM 2K Bytes RAM
auxiliary processor	
Microprocessor	8031 (12 MHz)
Memory	8K Bytes EPROM
Power Requirements	+5 Volts – 1500 mA (typical) +24 Volts – 40 mA (typical)
Input T1 Stream Specifications	
Format	Bipolar, D3
Frequency	1.544 MHz ± 200 Hz
Impedance	100 ohms ± 10 ohms
Framing Time	10 mS maximum

Table 1: T1 Card Specifications(Continued)

Specification	Description or Value
Output T1 Stream Specifications	
Format	Bipolar, D3
Drive Capability	0 - 655 Feet
Impedance	100 ohms ± 10 ohms

3.0 CIRCUIT DESCRIPTION

The T1 card interfaces a VCO/4K system with a T1 digital data carrier stream. The T1 card transmits a 1.544 MHz, 24-channel, bipolar digital data stream synchronized with the system clocks. The T1 card receives a T1 data stream of frequency 1.544 MHz +200 Hz and can drive a reference clock onto the switch backplane. The NBC uses the reference clock as an input to its system synchronization circuitry.

The T1 card detects loss of carrier errors, framing errors, signaling bit errors, and remote alarms on its incoming T1 stream. It also detects slips which occur when the rate at which data is sent on the incoming T1 stream is different from the rate at which data is transmitted onto a PCM data bus. The T1 card contains an elastic PCM data buffer to minimize slips caused by incoming T1 stream frequency jitter.

Figure 1 is a simplified block diagram of the T1 card.

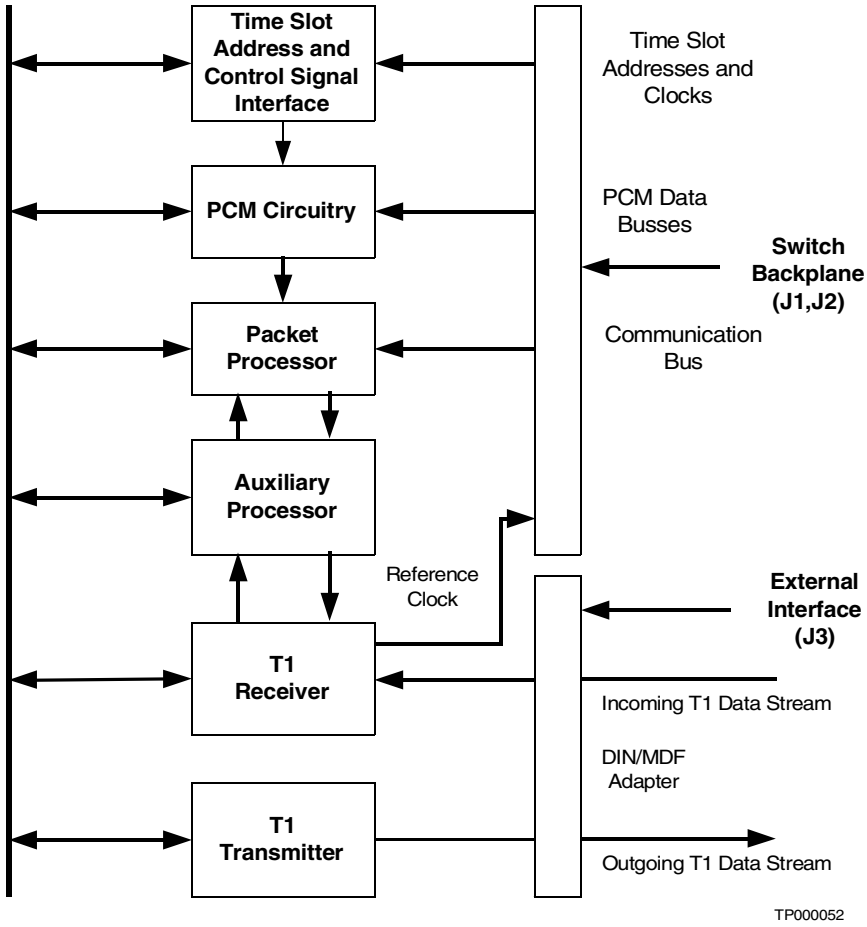


Figure 1: T1 Card Block Diagram

3.1 AUXILIARY PROCESSOR

The T1 card contains an auxiliary 8031 processor (auxiliary processor) to recover the A and B signaling bits from the T1 receiver and report the signaling bit states to the packet processor. The auxiliary processor is required to load the packet processor's data buffer whenever a valid change in a channel's signaling bit states occur.

The A and B signaling bits from the incoming T1 data stream are loaded into shift registers every master frame and are read before they are overwritten by the signaling bits from the next master frame. In addition, a moving average of the signaling bit values for each of the 24 T1 channels is performed to minimize the effects of an incorrect signaling bit transition caused by noise on the T1 data stream. The auxiliary processor performs this function, and interfaces to the packet processor to supply it information about valid signaling bit transitions.

3.2 T1 RECEIVER

The T1 receiver receives the incoming T1 data stream, synchronizes the receiver circuitry with the stream, provides an interface between the auxiliary processor and the received A and B signaling bits, and allows the packet processor to monitor the incoming T1 data stream.

The T1 receiver recovers a 1.544 MHz clock from the incoming T1 data stream. This clock can be placed on the backplane REF.CLK signal line. The NBC can synchronize the system clocks to the REF.CLK signal line to prevent slipping. If a carrier alarm occurs, the T1 receiver stops driving the REF.CLK signal.

3.3 T1 TRANSMITTER

The T1 transmitter inputs PCM data from the switch backplane and formats the data into an outgoing T1 data stream. A number of signals are provided to allow the packet processor to control the T1 transmitter.

The signaling method used to indicate the status (i.e. on/off hook) of each of the 24 T1 channels is called "robbed" bit signaling. One byte of PCM data for each channel is transmitted every frame. A frame occurs every 125 microseconds and consists of a framing bit and eight bits of PCM data for each of the 24 T1 channels.

Every sixth frame, the least significant data bit of every channel is replaced with the state of the A signaling bit for that channel. Every twelfth frame, the least significant data bit of every channel is replaced with the state of the B signaling bit for that channel. Twelve frames constitute a master frame. The framing bit embedded in the T1 data stream allows each frame of a master frame to be individually identified.

One bits (1s) are represented by pulses on the T1 data lines; zero bits (0s) are represented by the absence of a pulse. If too many zeros are sent in a row, a T1 receiver may lose synchronization with the T1 data stream. The T1 transmitter automatically outputs a one in the second least significant bit of the channel if the channel PCM data is all zeros. During T1 power up, loopback is enabled.The output of the T1 transmitter is input to the T1 receiver, and a stream of all ones is output on the T1 transmitter output tip and ring leads. When in loopback, the status of the T1 transmitter output stream (including signaling bits and remote alarming) should be correctly identified by the T1 receiver.

The T1 transmitter sends an alarm signal (called remote alarm) to the far end of the T1 connection when it cannot recover the received T1 stream.

3.4 PACKET PROCESSOR

The T1 card contains an 8032-based packet processor that interfaces to the communication bus. A packet processor is part of all cards in the master or expansion port subracks with the exception of the network bus controller (NBC). The packet processor polls the T1 transmitter and T1 receiver looking for an event (i.e. error condition or signaling bit transition). When polled by the NBC, the packet processor reports any status change. The packet processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The packet processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The packet processor consists of the 8032 microcomputer and associated RAM, EPROM, and address decode circuitry; the communication bus Interface; an asynchronous serial port; and the LED register. The 8032 provides the intelligence for the packet processor, and therefore for the T1 card.

The communication bus is the path by which the packet processor receives commands from and sends status to the NBC.

3.5 T1 CARD LED STATES

Table 2 lists front panel LED states for T1 cards and their meaning. Note that these states differ significantly from those for analog interface cards, such as the SLIC-2 and UTC-2. The following general signaling conditions apply to each LED.

- *Red (top) LED* – illuminates to signal a problem with an inward T1 stream (carrier loss, OOF or signaling bit error).
- *Yellow (center) LED* – illuminates to signal that a Yellow Alarm has been detected on the incoming T1 stream (remote carrier loss).
- *Green (bottom) LED* – not used for alarming.

Table 2: T1 Card LED States

T1 card LEDs			System Alarm	Condition	Card State	Outward Action
Red	**Yellow**	**Green**				
OFF	OFF	OFF	None	Normal	Active	Call processing is occurring
			Minor (FRM114)	Slip threshold exceeded	Maintenance[a]	None
			Minor (FRM 120)	OOF threshold exceeded	Maintenance[a]	None
OFF	**ON**	OFF	Minor (FRM112)	Loss of Remote Carrier	Maintenance	None
ON	OFF	OFF	Major (FRM 112)	Loss of Carrier	Maintenance	All ports seized out, sending Yellow alarm.
			Minor (FRM121)	Signaling Bit Error	Maintenance	Sending Yellow Alarm.
			Minor (FRM120)	OOF Error	Maintenance	Sending Yellow Alarm
OFF	**ON**	**ON**	Minor (FRM096)	Out-of-Service (OOS)	OOS	None

a. Applies to system with Manual Intervention for SLIP/OOFS feature flag set to Y (Yes).

- *If an Active T1 card is placed into Maintenance via master console or alarm condition, any calls in progress are torn down and no new seizures are accepted. On-hooks are also not processed in Maintenance state.*
- *If multiple conditions force the card into the Maintenance state, the card will not become active until all error conditions are cleared.*
- *If the Manual Intervention for SLIP/OOFS flag is set to "N", slips may be occurring even though the card is Active and no LEDS are illuminated. The maintenance threshold for OOFs is ignored and the T1 card will cycle in and out of Maintenance as the OOF condition is detected and cleared.*
- *Slip and OOF counters are automatically set to zero at midnight.*

3.6 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 4 lists the pin assignments for J1 on the T1.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.7 EXTERNAL INTERFACES

Connections to the incoming and outgoing T1 digital data streams are made via the J3 connector. A DIN to MDF adapter attaches to the J3 connector and allows external connection to the T1 card by a 15-position, sub-D type connector or an Accunet® 8-pin modular jack. A male sub-D type connector is provided on the MDF Adapter. J3 connector pinouts are listed in Table 5. The J3 to D connector pinouts are shown in Figure 2 and Table 5 and Table 6.

3.8 T1 LINE EQUALIZATION

The T1 card provides a pre-emphasis equalizer to balance its transmit stream according to the length of the cable being driven. DIP Switch S1 provides line equalization for the span line to a channel bank. The equalization factors apply to ABAM cable comprised of two individually shielded twisted pairs, 22AWG conductors.

S1 settings are approximate for span line lengths up to 650 feet. For critical applications, Cisco Systems recommends using an oscilloscope across the channel bank end of the span to view the waveform. S1 settings can then be manipulated to obtain a satisfactory waveform.

A ten-position DIP switch is provided for easy selection of the required pre-emphasis. The DIP switch settings are shown in Table 3.

Table 3: T1 DIP Switch Settings

Span Length	S1-1	S1-2	S1-3	S1-4	S1-5	S1-6	S1-7	S1-8	S1-9	S1-10
0 to 150 ft. (0 to 45.7m)	Open	Open	Open	Clsd	Clsd	Clsd	Clsd	Open	Open	Open
150 to 450 ft. (45.7 to 137m)	Clsd	Open	Open	Clsd	Clsd	Clsd	Clsd	Open	Open	Clsd
450 to 655ft (137 to 200m)	Open	Open	Clsd	Clsd	Clsd	Clsd	Clsd	Clsd	Open	Open

Table 4: T1 Card J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus

Table 4: T1 Card J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 5: T1 Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Digital Ground
2	Unused	Unused	Reserved
3	Unused	Unused	Rcv Line Tip[a]
4	Unused	Unused	Rcv Line Ring[a]
5	Unused	Unused	Xmit Line Tip[b]
6	Unused	Unused	Xmit Line Ring[b]
7 – 32	Unused	Unused	Unused

a. Signal to T1 card

b. Signal from T1 card

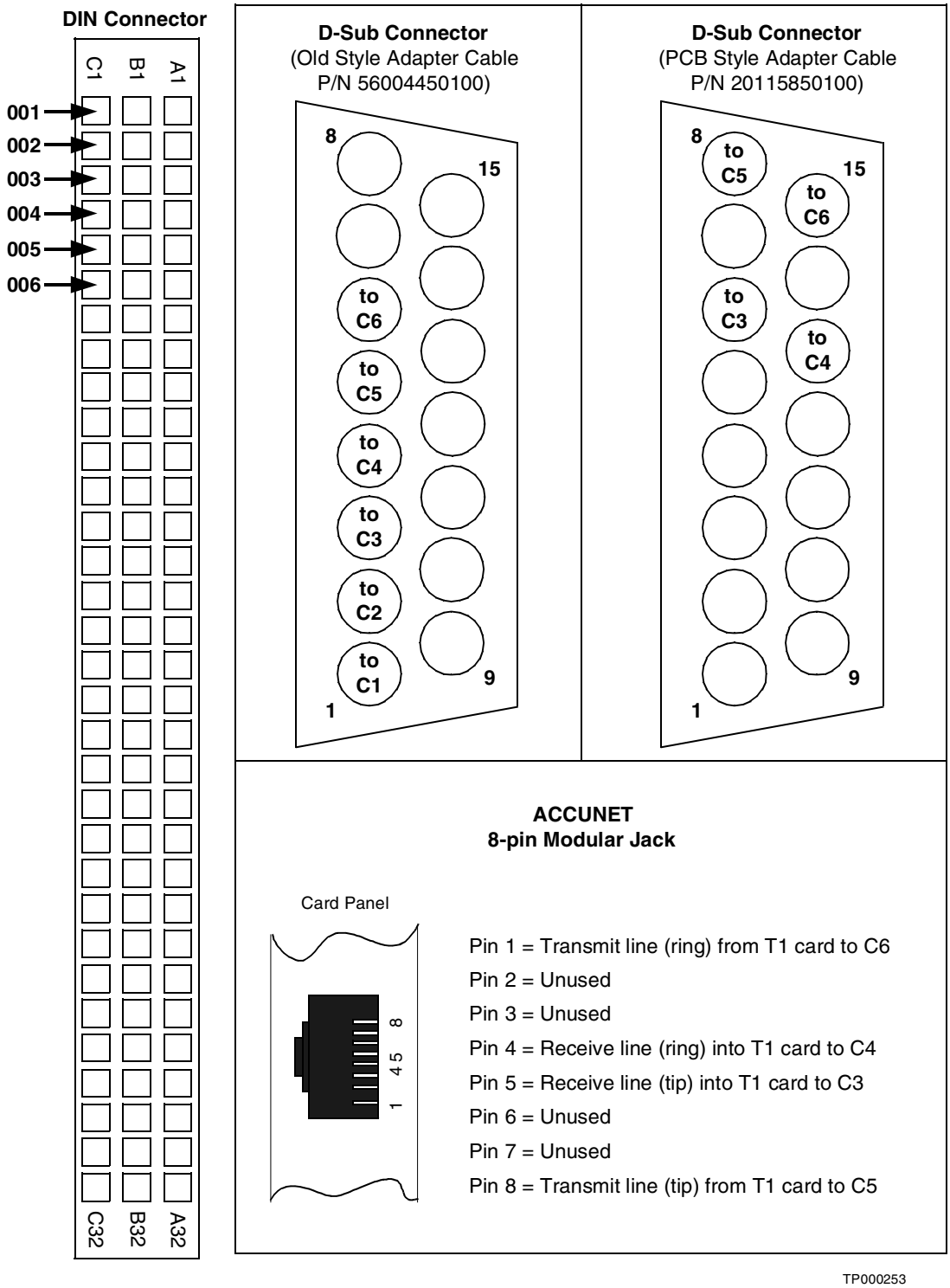


Figure 2: T1 Adapter Pinout Diagram

NOTE: 20115850100 is the part number for the entire PCB Style Adapter assembly. A different number (50191050100) may be etched on the Adapter's PCB. The etched number is the part number for the PCB only. Use the assembly number when ordering a new adapter.

Table 6: T1 Card J3 to D-Connector/Modular Jack Pinouts (Plug-In Type)[a]

J3 Pin	D-Connector Pin[b]	Modular Jack	Signal Name
1C	*Not Connected*	*Not Connected*	Digital Ground
2C	*Not Connected*	*Not Connected*	Reserved
3C	1	8	Receive Line Tip (to card)
4C	9	1	Receive Line Ring (to card)
5C	3	5	Transmit Receive Line Tip (from card)
6C	11	4	Transmit Line Ring (from card)

a. Plug-In T1 and PRI/N adapter (PCB style for 3-row backplane)

b. DA-15S, ISO 4903

4.0 CONFIGURATION NOTES

The T1 card is manufactured by Cisco Systems, Inc. Figure 4 shows the location of the equalization DIP Switch and the PROM containing the T1 firmware. Refer to this figure and the switch settings in Section 3.08 to configure the interface card prior to installing it in a port subrack.

NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.

If a card is improperly configured, it may fail to perform its interface function between external trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a T1 card in the system data base, refer to the *System Administrator's Guide.*

Class of Service (COS) also greatly affects the operation of the card. A COS of "T", "2", or "A2" sees inward seizures as call originations. A COS of "O" interprets inward seizures as the port being busied out by the far end. If calls are not being properly processed, check the COS.

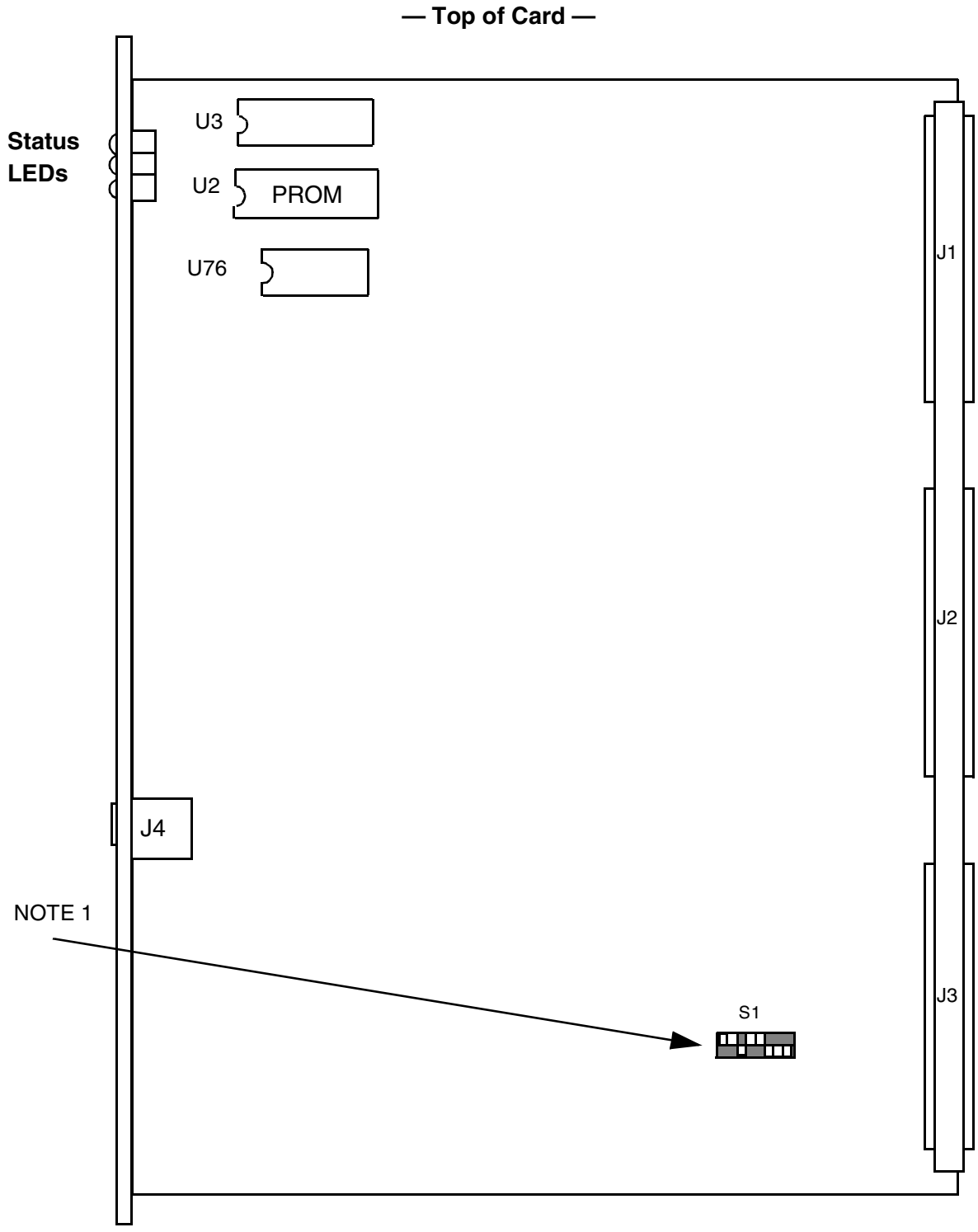


Figure 3: T1 Card DIP Switch & PROM Locations

5.0 RELATED DOCUMENTATION

For additional information regarding the operation, application, installation and maintenance of the T1, refer to the following publications.

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- Technical Description: Port Subrack

Universal Trunk Card (UTC-2)

1.0 GENERAL

The Universal Trunk Card (UTC-2) is a standard system port interface circuit card that resides in the Master or any Expansion Port Subrack. It supports eight 2-wire, originating and terminating trunk connections; the CO must supply office battery. Terminating characteristics include: 2-wire interface with ringdown detect; ring trip capability; dedicated DTMF receiver. Originating characteristics include: 2-wire, dry loop or ground start; with battery reversal detection and wink detect. Tip and Ring leads are fused and surge protected.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM 2K Bytes RAM
Power Requirements:	**Typical**
	+5 Volts: 700 mA +15 Volts: 150 mA –15 Volts: 160 mA +24 Volts: 192 mA *
	* *all relays energized*
Trunk Specifications	
Input Level:	0 dB ± 0.5 dBm
Output Level:	0 dB ± 0.5 dBm *or* -3 dB ± 0.5 dBm (jumper selectable)
Line Impedance:	600 ohms, ± 10% *or* 900 ohms, ± 10% (jumper selectable)
Crosstalk Attenuation:	75 dB minimum
Idle Circuit Noise:	23 dBrnc maximum
Ringer Equivalence:	0.7B
Echo Return Loss:	20 dB minimum
(Line to Trunk)	
Singing Return Loss:	12 dB minimum (low) to 15 dB minimum (high)
(Line to Trunk)	
Single Freq. Return Loss:	12 dB minimum, 300 to 3400 Hz
(Line to Trunk)	
Frequency Response:	
(Signal levels relative to 1004 Hz with C Message Filter)	
60 Hz:	-20 dB maximum
200 Hz:	-3 to 0.0 dB
300 to 3000 Hz:	-1 to 0.5 dB
3400 Hz:	-3 to 0.0 dB

Longitudinal Balance:	
200–4000 Hz	60 dB minimum
Operating Loop Current:	16 mA to 100 mA
DTMF Receiver:	
Detectable input level	-25 dBm minimum 1 dBm maximum
Acceptable twist:	10 dB maximum
Tone or quiet duration:	40 mS minimum

CAUTION: This version of the UTC-2 may be used interchangeably in listed (UL 1459) and non-listed systems in applications not requiring on-board call progress tone detection. However, earlier versions of the UTC (P/Ns 50149060200 or 50149080200) cannot be used in listed systems.

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the UTC-2. The five major elements of the UTC-2 are:

- Per Port Circuitry
- PCM Time Slot Bus Interface
- Packet Processor
- Control & Status Registers
- Protective Devices

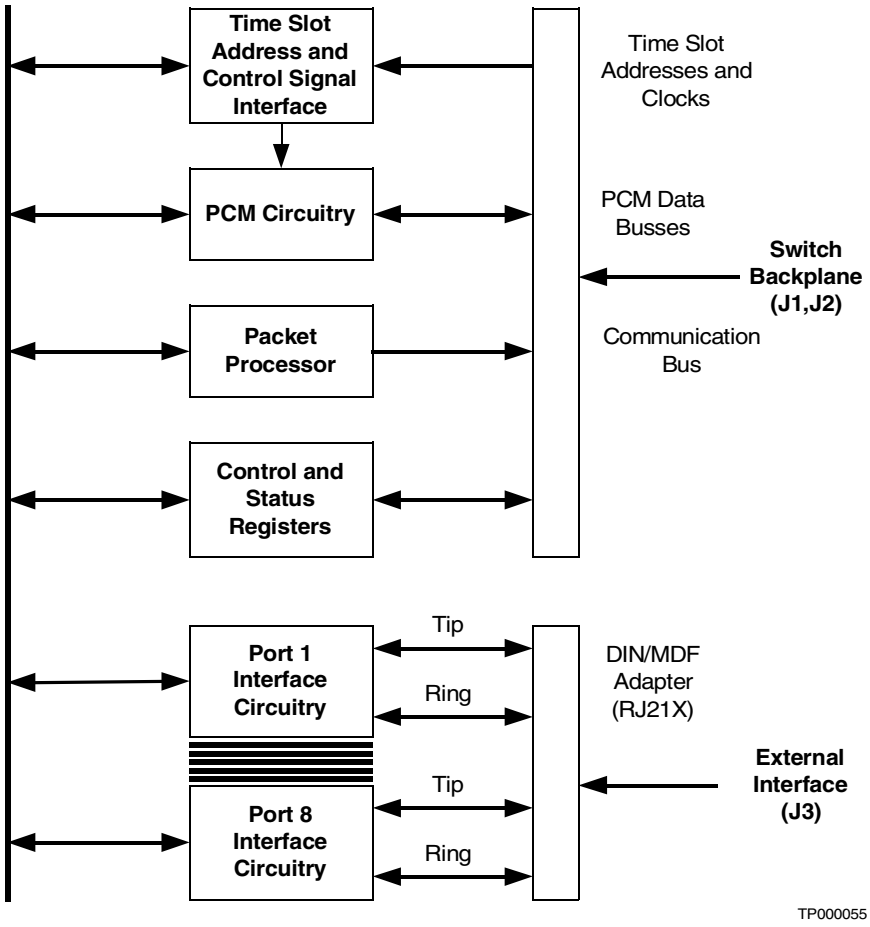


Figure 1: Block Diagram Of UTC-2

3.1 PER PORT CIRCUITRY

Each of the eight ports on a UTC-2 includes the following:

- DTMF Digit Receiver
- Analog to Digital Encoding and Decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On/Off hook detection
- Ground start relay (grounds ring lead)
- Incoming ring voltage detection
- Battery reversal and current detection
- Tip and Ring lead fuses
- Surge protection across Tip and Ring leads.

3.2 DTMF DIGIT RECEIVER

A DTMF digit receiver integrated circuit (I.C.) is provided for each UTC-2 card port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

3.3 ANALOG TO DIGITAL ENCODING & DECODING

A 2913 codec provides digital-to-analog and analog-to-digital signal conversion. A codec semi-custom interface I.C. performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between itself and the codec.

Data received from both PCM busses is latched into parallel in/serial out shift registers internal to the codec interface I.C. The codec semi-custom interface I.C. supplies the data by selecting the output of one of the two internal parallel-to-serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode and decode A-law or μ-law PCM data. Two jumper areas on the UTC-2 allow selection of the clock frequency and PCM encoding rule for all eight codecs.

3.4 ANALOG INTERFACE

The analog interface consists of circuitry from the Tip and Ring leads to the input of the codec device. A high-impedance op-amp circuit detects battery reversal conditions. The ring voltage detector is connected across the tip and ring leads; the normally open relay contacts are connected to the ring lead and to battery ground. When the relay is energized, battery ground is applied to the ring lead for ground start trunk seizing.

Voiceband energy presented to the tip and ring leads is coupled to the negative input of the codec's transmit amplifier via the transformer and the hybrid circuit. Voice and energy driven by the codec's receive amplifier is coupled to the tip and ring leads via the hybrid circuit and transformer. This energy is prevented from being output by the codec's transmit amplifier using active cancellation techniques. This cancellation (called transhybrid balance) is optimized when the trunk impedance matches that of the two wire port. Line impedance is jumper selectable for either 600 or 900 ohm impedance.

The DTMF digit receiver I.C. is connected to the output of the codec transmit amplifier. A single 3.5795 MHz crystal oscillator package provides the clock input required by the DTMF receivers.

3.5 ON/OFF HOOK & GROUND START RELAYS

Before a call can be initiated or answered on a trunk connected to a UTC-2 port, the trunk must first be set off-hook. On-board relays control the off-hook process. Call processing software causes the appropriate port to go off-hook allowing current to flow. The current (if battery is being provided by an external source such as a Central Office trunk) is detected by one of the two current detectors. The ground start relay seizes a ground start trunk by grounding the ring lead of the trunk.

3.6 RING VOLTAGE & CURRENT FLOW DETECTORS

Ring voltage, battery reversal and current detectors are provided for each UTC-2 port. The ring voltage detector alerts the Packet Processor to answer an incoming call.

Current flow detectors allow the Packet Processor to determine winks and other port activity. When a port is set off hook a control register bit goes low to indicate that current is flowing in the normal direction. If an open circuit or reverse battery wink occurs, this bit goes high for the duration of the wink. The on/off hook relay must be set off hook to detect current, but need not be off hook to detect ring voltage.

3.7 TIP & RING PROTECTIVE DEVICES

Tip and Ring leads of the eight circuits on the UTC-2 are protected from overvoltage and overload conditions as shown in Figure 2.

The SIDACtor™ on each port provides transient surge protection from lightning, line transients and other damaging voltage spikes. This single package device protects against Tip to Ring transients. When the monitored voltage exceeds 235Vac, the SIDACtor switches on through a negative resistance region to a low on-state voltage in nanoseconds. It continues to conduct until the current is interrupted or drops below the minimum holding current of the device. Series resistors limit incoming current to the rest of the interface.

The 2AG Slo-Blo fuses are soldered into the circuit board and are not field replaceable. If a fuse blows, contact Cisco Systems Technical Support to arrange for repair.

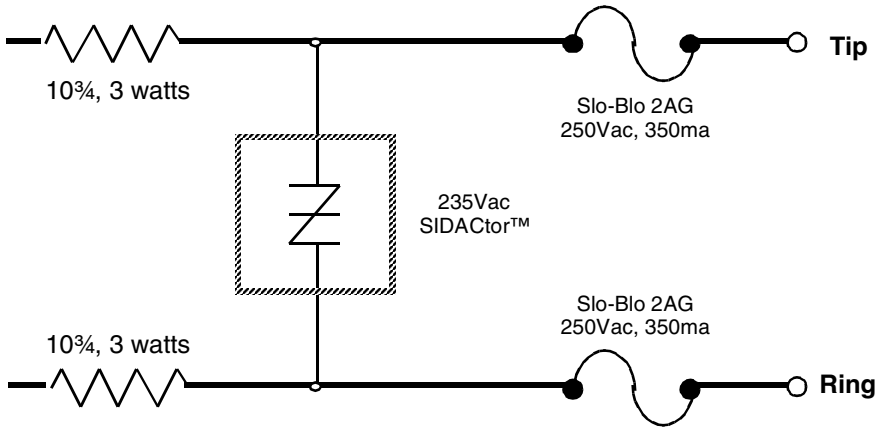


Figure 2: Schematic Diagram Of Tip & Ring Protective Devices

4.0 PCM TIME SLOT BUS INTERFACE

All voice data within a system is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the UTC-2 translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The UTC-2 interfaces to the dual PCM time slot busses with bus interface circuitry common to several system port-oriented circuit cards. Each of the eight port interfaces on the UTC-2 can listen to any time slot on either PCM data bus.

A UTC-2 is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular UTC-2 port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

5.0 PACKET PROCESSOR

The UTC-2 contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC). The Packet Processor polls each of the eight trunk connections looking for an event (i.e. ring detection or valid DTMF digit reception). When polled by the NBC, the Packet Processor reports any status change.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the UTC-2. The Communication Bus is the path by which the Packet Processor receives commands from and sends status to the Network Bus Controller.

6.0 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the UTC-2.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

7.0 EXTERNAL INTERFACES

The connections to the Tip and Ring leads of the eight line/trunk interfaces on the UTC-2 are made via the J3 connector. A DIN to MDF adapter attaches to J3 and terminates the tip/ring connections of up to three UTC-2s to a standard RJ21X, 25-pair connector. It is expected that wet trunk connections be made via the RJ21X connector to the tip and ring leads of the individual trunks. The J3 pin assignments for each UTC-2 are provided as Table 2. J3 to RJ21X pinouts are shown in Table 3 and Figure 3.

Table 1: UTC-2 J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	*Unused*	DGND
2	DGND	*Unused*	DGND
3	DGND	*Unused*	DGND
4	DGND	*Unused*	DGND
5	Battery Return	*Unused*	Battery Return
6	Battery Return	*Unused*	Battery Return
7	Battery Return	*Unused*	Battery Return
8	Unused	*Unused*	Unused
9	Ring Voltage	*Unused*	Ring Voltage
10	Unused	*Unused*	Unused
11	Digital +5V	*Unused*	Digital +5V
12	Digital +5V	*Unused*	Digital +5V
13	Digital +5V	*Unused*	Digital +5V
14	+24V	*Unused*	+24V
15	Battery (-48V)	*Unused*	Battery (-48V)
16	Battery (-48V)	*Unused*	Battery (-48V)
17	Battery (-48V)	*Unused*	Battery (-48V)
18	Analog -15V	*Unused*	Analog -15V
19	Analog -15V	*Unused*	Analog -15V
20	Analog +15V	*Unused*	Analog +15V
21	Analog +15V	*Unused*	Analog +15V
22	Card Addr. Bit 1	*Unused*	Card Addr. Bit 0
23	Card Addr. Bit 3	*Unused*	Card Addr. Bit 2
24	Card Addr. Bit 5	*Unused*	Card Addr. Bit 4
25	Card Addr. Bit 7	*Unused*	Card Addr. Bit 6
26	SRV	*Unused*	AB1
27	DID	*Unused*	AB2
28	RST	*Unused*	Serial Bus

Table 1: UTC-2 J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
29	CTV	*Unused*	CTT
30	GND	*Unused*	GND
31	GND	*Unused*	GND
32	DGND	*Unused*	DGND

Table 2: UTC-2 J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Unused
2	Trunk 1 – Tip	Unused	Trunk 1 – Ring
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – Tip	Unused	Trunk 2 – Ring
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – Tip	Unused	Trunk 3 – Ring
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Trunk 4 – Tip	Unused	Trunk 4 – Ring
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – Tip	Unused	Trunk 5 – Ring
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – Tip	Unused	Trunk 6 – Ring

Table 2: UTC-2 J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Trunk 7 – Tip	Unused	Trunk 7 – Ring
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – Tip	Unused	Trunk 8 – Ring
31	Unused	Unused	Unused
32	Unused	Unused	Unused

Table 3: J3 to RJ21X Pinouts

Card	Trunk	Tip Lead	Ring Lead
1	1	J3-2A to RJ21X-26	J3-2C to RJ21X-1
1	2	J3-6A to RJ21X-27	J3-6C to RJ21X-2
1	3	J3-10A to RJ21X-28	J3-10C to RJ21X-3
1	4	J3-14A to RJ21X-29	J3-14C to RJ21X-4
1	5	J3-18A to RJ21X-30	J3-18C to RJ21X-5
1	6	J3-22A to RJ21X-31	J3-22C to RJ21X-6
1	7	J3-26A to RJ21X-32	J3-26C to RJ21X-7
1	8	J3-30A to RJ21X-33	J3-30C to RJ21X-8
2	1	J3-2A to RJ21X-34	J3-2C to RJ21X-9
2	2	J3-6A to RJ21X-35	J3-6C to RJ21X-10
2	3	J3-10A to RJ21X-36	J3-10C to RJ21X-11
2	4	J3-14A to RJ21X-37	J3-14C to RJ21X-12
2	5	J3-18A to RJ21X-38	J3-18C to RJ21X-13
2	6	J3-22A to RJ21X-39	J3-22C to RJ21X-14
2	7	J3-26A to RJ21X-40	J3-26C to RJ21X-15
2	8	J3-30A to RJ21X-41	J3-30C to RJ21X-16
3	1	J3-2A to RJ21X-42	J3-2C to RJ21X-17
3	2	J3-6A to RJ21X-43	J3-6C to RJ21X-18
3	3	J3-10A to RJ21X-44	J3-10C to RJ21X-19
3	4	J3-14A to RJ21X-45	J3-14C to RJ21X-20
3	5	J3-18A to RJ21X-46	J3-18C to RJ21X-21
3	6	J3-22A to RJ21X-47	J3-22C to RJ21X-22
3	7	J3-26A to RJ21X-48	J3-26C to RJ21X-23
3	8	J3-30A to RJ21X-49	J3-30C to RJ21X-24

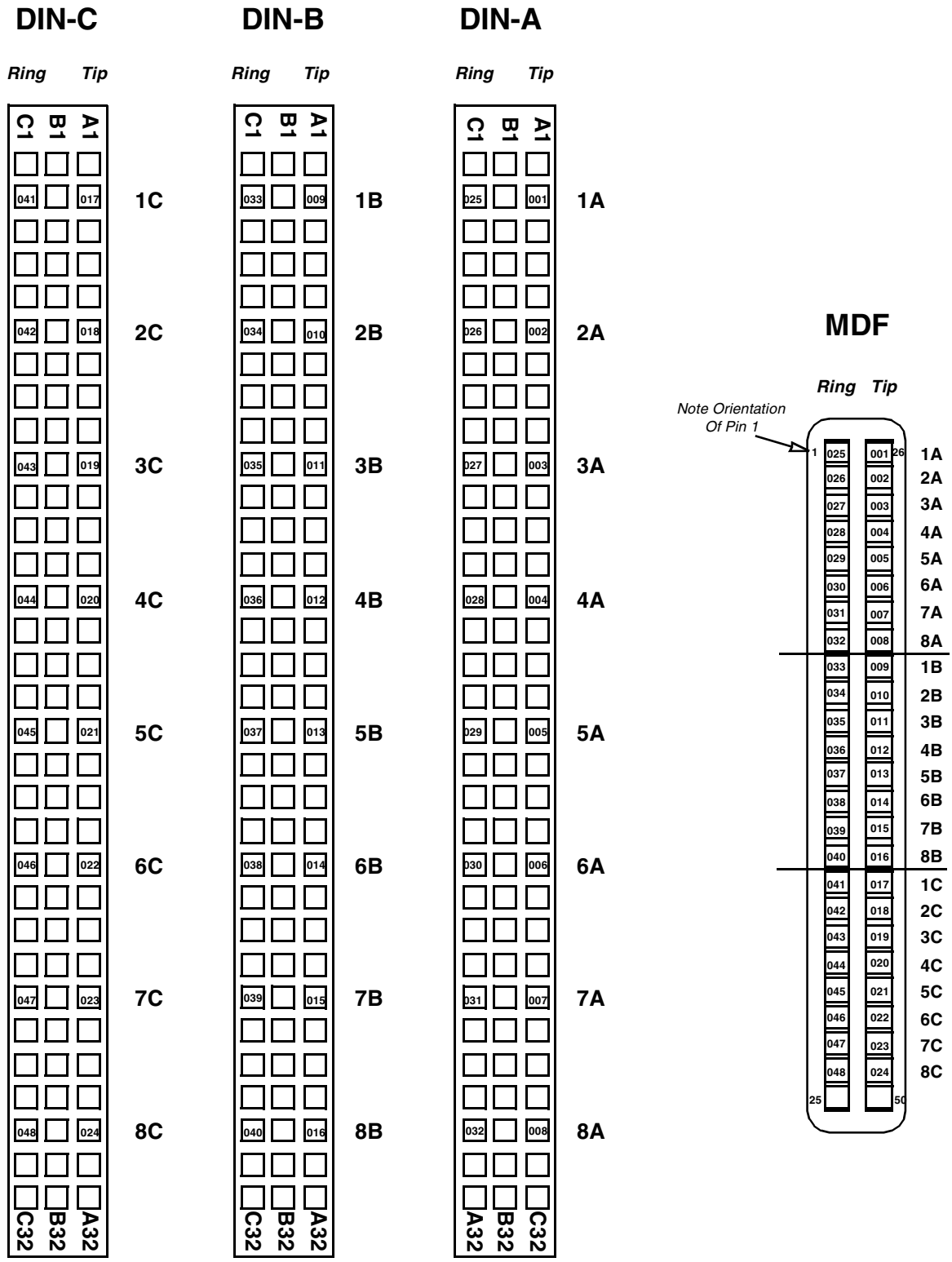


Figure 3: Pin-Out Diagram of DIN–RJ21X MDF Adapter

8.0 CONFIGURATION NOTES

The UTC-2 is manufactured by Cisco Systems, Inc. Jumper plugs on the UTC-2 are factory set for use in systems. Figure 4 indicates the location and correct installation of jumper plugs and wires on UTC-2s based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it in a Port Subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the component side of the PCB near the card front panel. The PCB is etched with four characters indicating the revision level. The first three characters are the actual revision level. The final letter "R" indicates that the PCB is at Release level. For example, a revision level A0L card is marked as Rev. "A0LR".*

If a card is improperly configured, it may fail to perform its interface function between external trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a UTC-2 in the system data base, refer to the *VCO/4K System Administrator's Guide*.

Class of Service (COS) also greatly affects operation of the card. A COS of "T", "2" or "A2" sees inward seizures as call originations. A COS of "O" interprets inward seizures as the port being busied out by the far end. If calls are not being properly processed, check the COS.

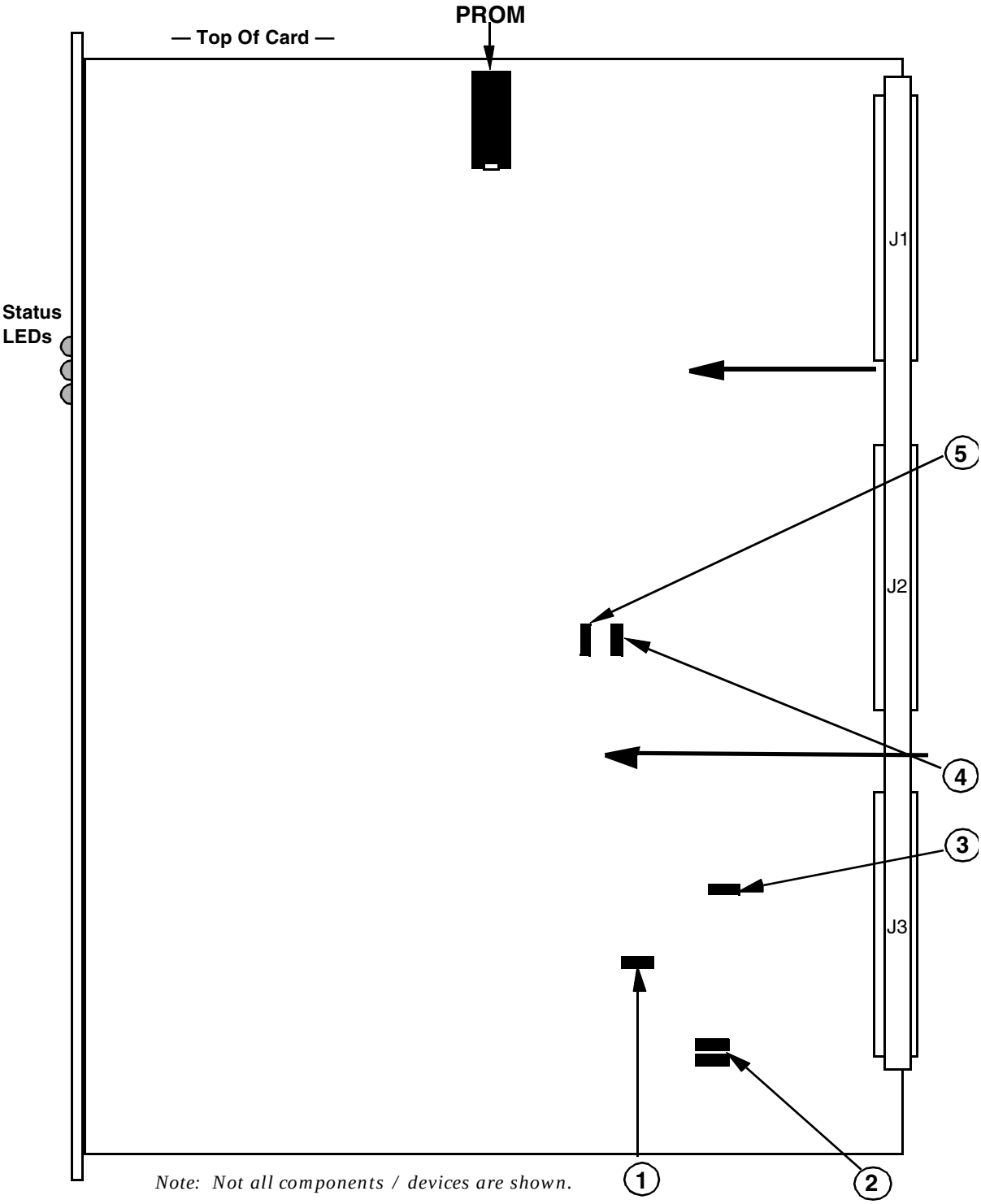


Figure 4: UTC-2 Jumper & Prom Locations

8.0.1 JUMPER LOCATIONS

Refer to Figure 6 for the following jumper settings.

NOTE 1

The jumpers at locations JX03 (X = circuits 1 through 8) support 600- or 900-ohm trunks for each circuit.

- Install jumper plugs in position 6 for 600-ohm trunks (default).
- Install jumper plugs in position 9 for 900-ohm trunks.

NOTE 2

The jumpers at location JX01 and JX02 (X = circuits 1 through 8) let you choose between loop start (LS) and ground start (GS) operation for each circuit.

- Install jumper plugs in JX01 and JX02, pins 1-2, for GS operation.
- Install jumper plugs in JX01 and JX02, pins 2-3, for LS operation (default).
- Move both jumpers towards JX03 for GS operation.

NOTE 3

The jumpers at location JX04 (X = circuits 1 through 8) support 0db or -3db output for each circuit.

- Install jumper plugs in position 0 for 0 db output.
- Install jumper plugs in position -3 for -3 db output (default).

NOTE 4

- Install the jumper plug at J5 in the a position (pins 1-2) for 2.048 MHz codec clock.
- Install the jumper plug at J5 in the b (pins 2-3) position for 1.544 MHz codec clock (default).

NOTE 5

- Install jumper plug at J6 in the a position for codec A-law operation (European standard).
- Install jumper plug at J6 in the b position for codec μ-law operation (North American standard). The b position is the default for J6.

8.0.2 PROM LOCATION

The 2764 PROM in location U2 contains firmware appropriate to the UTC-2 signaling interface requirements.

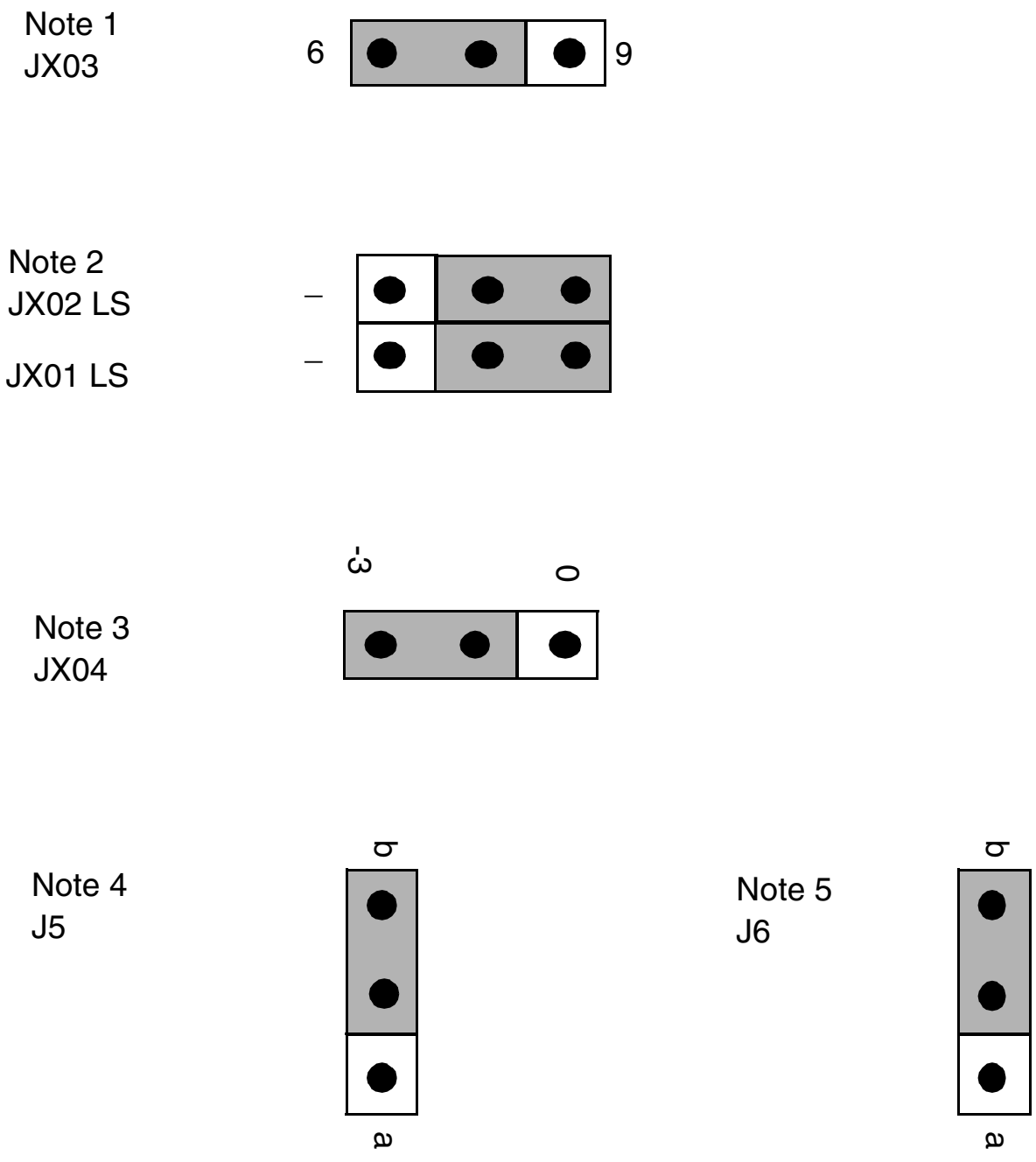


Figure 5: Default Jumper Positions for UTC-2

9.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the UTC-2, refer to the following publications.

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- Technical Description: Plug-in MDF Adapters

Call Progress Analyzer Card (CPA)

1.0 GENERAL

The Call Progress Analyzer (CPA) is a standard system service circuit card that resides in the Master or any Expansion Port Subrack. When downloaded with application software under V2.03 Generic (or later) software, the CPA performs call progress tone detection. The CPA is available as a resource for all system trunk types and replaces the progress tone detectors on Universal Trunk Cards (UTCs).

The CPA is based on a single, high speed Digital Signal Processor (DSP) with associated high speed (25ns) memory. Each CPA card supports 24 service circuit channels. The Call Progress Analyzer application is downloaded from hard disk to the CPA card via the system COMM bus.

This document describes the general hardware configuration of the CPA. For additional information about the CPA application, refer to the *Generic Release Notes*.

2.0 SPECIFICATIONS

Digital signal processor

Microprocessor:	(1) AT&T 32C (50MHz)
Memory:	128 KB, 25ns high speed SRAM

Packet processor

Microprocessor:	(1) 8031 CPU (12MHz)
Memory:	2 KB RAM 8 KB EPROM

Power requirements:	Typical -5 Volts: 800 mA
Channels per card:	24
Standard CPA call progress tones:	Dial Tone Audible Ringback Busy Tone Reorder tone
Other tones/events:	Special Information Tones (SITs) Human Voice (presence/cessation) Pager Cue Tones

3.0 CIRCUIT DESCRIPTION

The Call Progress Analyzer card is a high performance, signal processing platform for running application software requiring direct access to the system PCM busses. Two types of processors are employed on the CPA.

- *Digital Signal Processor (DSP)* interfaces directly with the system PCM busses and processes the PCM samples to detect call progress events.
- P*acket Processor* is a generic term for the interface between the CPA and the Network Bus Controller (NBC-3). Its functions include the management of command and message packets passed between the CPA and NBC, and high level control over the DSP.

Figure 1 shows a simplified block diagram of the CPA.

3.1 DIGITAL SIGNAL PROCESSOR

The CPA utilizes an AT&T 32C DSP running at 50MHz. The 32C incorporates the following features:

- 80ns cycle times
- 32-bit floating point arithmetic
- Single precision floating point IEEE compatibility
- 16 Mbps serial interface
- 32-bit external data bus

High speed, 128 KB, 25ns SRAM memory is associated with the DSP.

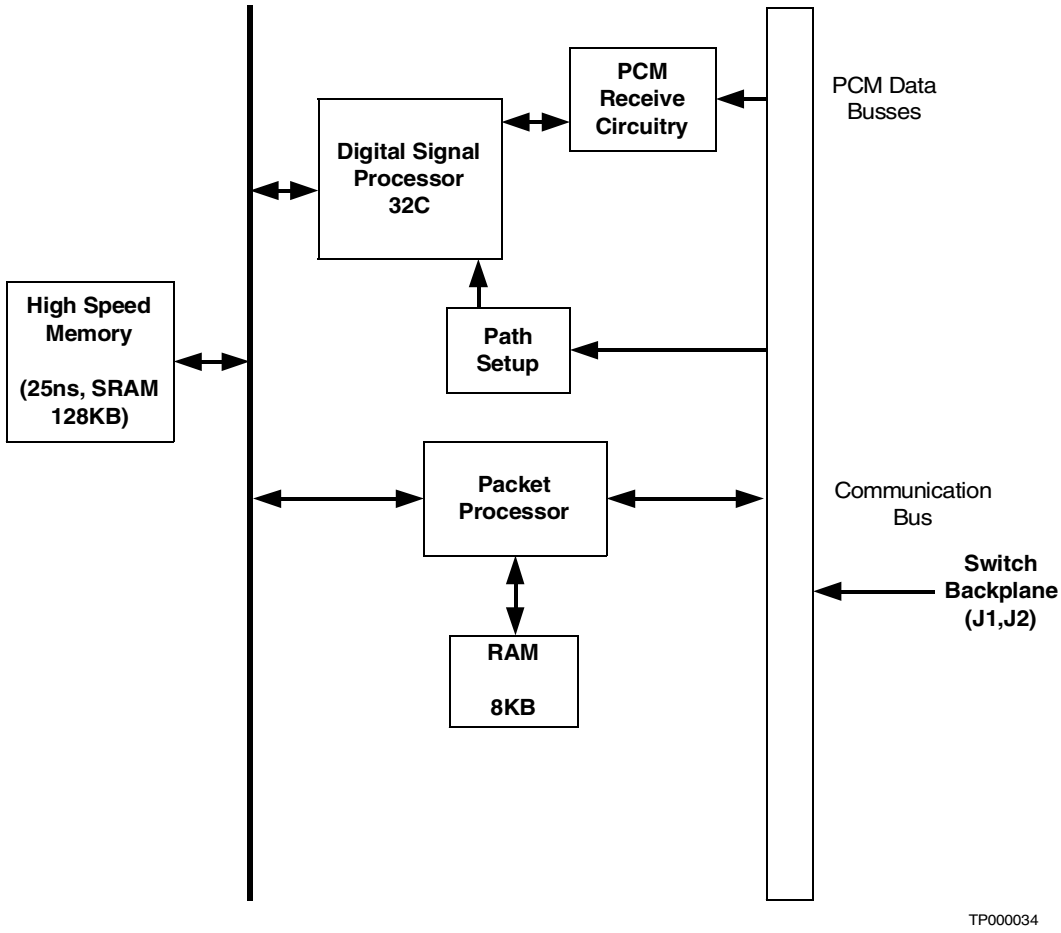


Figure 1: Block Diagram Of CPA

3.2 PACKET PROCESSOR

The CPA contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC).

The Packet Processor consists of the 8031 microcomputer, program and data memory, the Communication Bus Interface, an asynchronous serial port, and the LED register. The NBC issues commands and downloads application software to the CPA via the COMM Bus in the form of data packets. The 8031 uses a variable system clock to slow down the bus cycles during accesses to the DSP.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green), which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry (the Communication Bus Interface, an asynchronous serial port, and the LED register).

3.3 COMMUNICATION BUS INTERFACE

The Communication Bus Interface on the Packet Processor interfaces to the Communication (COMM) Bus. There are two types of data transfer cycles over the COMM Bus – Individual Card Cycles and Broadcast Cycles. Individual Card Cycles are used when the NBC desires two-way communication with a single card. Broadcast Cycles are used when the NBC needs to send data (broadcast) to all cards or all cards of a particular type.

3.4 PCM RECEIVE CIRCUITRY

All PCM data is directly addressable by the DSP. The CPA uses Dual Port RAM (DPR) to interface with the PCM buses. Each of the DPRs holds two frames of PCM. The frames switch on the system frame signal which occurs during the first timeslot.

The DSP gets the PCM data for each of its 24 channels during a single 125 µs frame. The DSP is interrupted every 125µs by the system frame signal and enters a PCM acquisition subroutine. Each DSP has up to 24 ports for addressing PCM data. Under software command the DSP reads the PCM data through an assigned port and stores it in memory.

The port address is converted into an actual timeslot address. This timeslot address directly addresses the stored PCM and enables the data onto the DSP data bus. Because the DSP setup RAM is shared by three resources – the DSP, the serial path setup circuitry, and the Packet Processor – access to the RAM is made on a request and grant basis.

The path setup RAM provides the gateway for access to the PCM data. Access is granted if none of the other resources are using or requesting it. Path setups can originate from the NBC or the Packet Processor. The NBC serial path setup circuitry has highest priority and the Packet Processor has second-highest priority in any contended access.

3.5 CPA STATUS LEDS

A red, a yellow, and a green LED are visible through the CPA's front panel to indicate the status of the card. Each LED is turned on when the software generic sets a bit low in an external memory register. Typically an illuminated red LED indicates a major card failure, an illuminated yellow LED indicates a minor card failure, and an illuminated green LED indicates the card is in standby or diagnostic mode.

3.6 BACKPLANE CONNECTOR PIN ASSIGNMENTS

The CPA does not require connection to external devices. Pin assignments for backplane connectors J1 through J3 on the CPA are proprietary and, therefore, not documented for customer use.

4.0 CONFIGURATION NOTES

The CPA is manufactured by Cisco Systems, Inc. Jumper plugs on the CPA are factory set for use. Figure 2 indicates the location and correct installation of jumper plugs on a CPA, based on the card's PCB revision level. Use this information to verify or reset jumpers on the CPA prior to installing it in a Port Subrack.

If a card is improperly configured, it may fail to operate. Therefore, great care must be taken to verify configuration settings before installing a replacement service circuit card in the system.

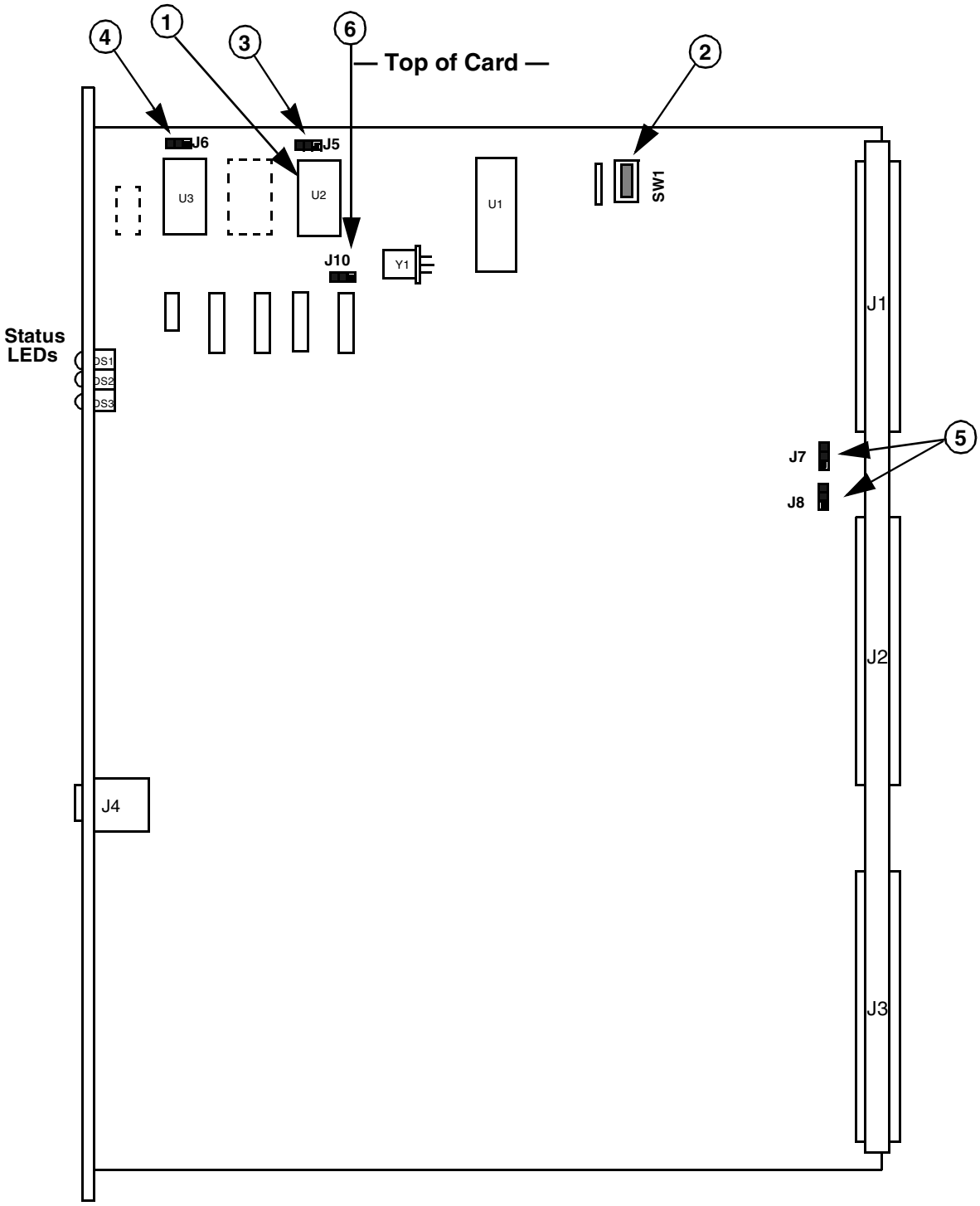


Figure 2: CPA Jumper & PROM Locations

4.0.1 NOTE 1

The PROM1(2764 PROM) in location U2 contains firmware appropriate to CPA processing requirements.

NOTE: Version 1.01 of the CPA firmware does not support PCB, Revision D or later. Version 1.03 of the CPA firmware does not support PCB, Revision C and earlier.

4.0.2 NOTE 2

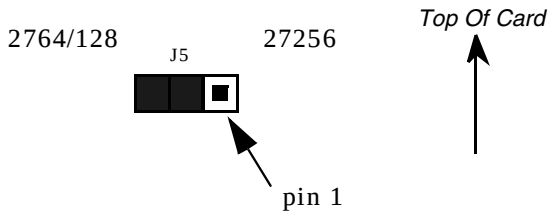
SW1 DIP switches SW1-1 through SW1-8 must be set as follows:

1-11-21-31-41-51-61-71-8

ClsdClsdClsdClsdClsdClsdClsdClsd

4.0.3 NOTE 3

The J5 jumper must be set at pins 2 and 3 as shown in the following illustration:

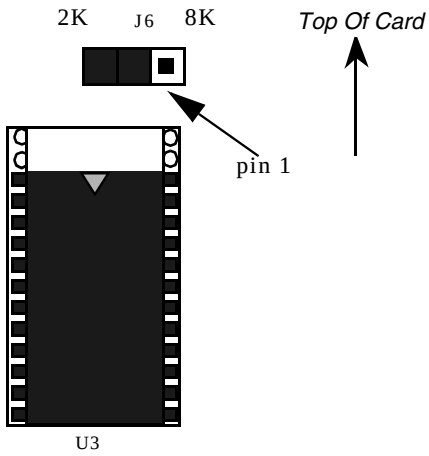


NOTE: *For readability, "2764/128," "J5," and "27256" are rotated 180° from the orientation of the printed text on the card.*

4.0.4 NOTE 4

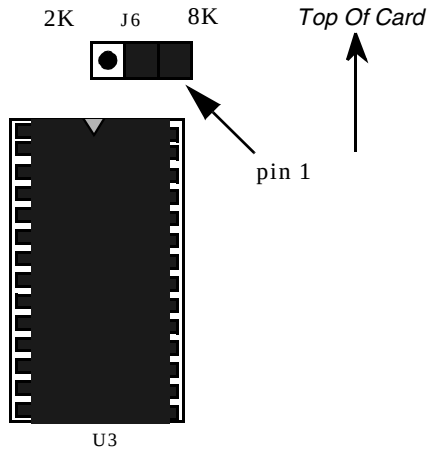
The setting of J6 jumper is dependent on the size of the card's SRAM. The SRAM is installed at location U3 and is either 2K or 8K. The J6 jumper settings are shown in the following illustration:

Setting for 2K SRAM



Set J6 to pins 2 and 3 for 2K SRAM

Setting for 8K SRAM



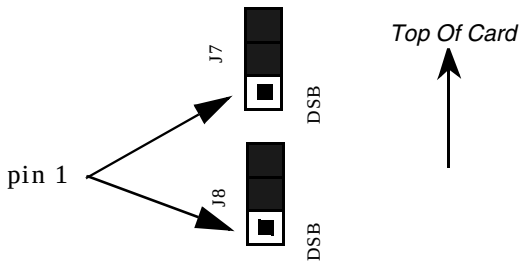
Set J6 to pins 1 and 2 for 8K of SRAM

NOTE: For readability, "2K," "J6," and "8K" are rotated 180° from the orientation of the printed text on the card.

To identify which SRAM device is installed on the card, observe how the SRAM chip sits in the U3 socket. The U3 socket can accommodate a 28 pin device. However, 2K SRAM is a 24 pin device. When 2K SRAM is installed at U3, the top two rows of the socket are left empty as shown in Figure 2. The 8K SRAM is a 28 pin device, therefore, when an 8K SRAM is installed, all rows in the socket are used.

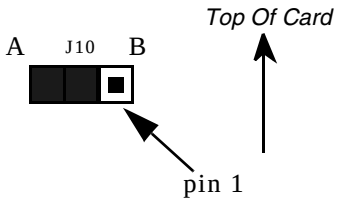
4.0.5 NOTE 5

J7 and J8 jumpers must be set at pins 2 and 3 as shown in the following illustration:



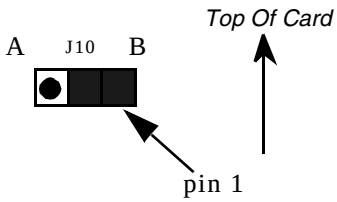
4.0.6 NOTE 6

For revisions prior to Rev D, J10 jumper must be set at pins 2 and 3 (position A) as shown in the following illustration:



NOTE: For readability, "A," "J10," and "B" are rotated 180° from the orientation of the printed text on the card.

For Rev D or later, J10 jumper must be set at pins 1 and 2 (position B) as shown in the following illustration:



NOTE: For readability, "A," "J10," and "B" are rotated 180° from the orientation of the printed text on the card.

5.0 REMOVAL/REPLACEMENT PROCEDURES

Follow the directions in the VCO/4K Card Overview to remove or replace a CPA card.

NOTE: At least one CPA must be in-service for the system to support call progress tone detection.

6.0 TROUBLESHOOTING

The following subsections discuss various troubleshooting situations.

6.1 FAILURE TO DOWNLOAD

On system reset, the Call Progress Analyzer application software is broadcast to all CPAs in the system. If an individual CPA fails to complete the download, it is taken out of service and a directed download is performed to the failed card after the broadcast download has been completed. Those CPAs which complete the download come into service and become available to process call progress tone detection requests.

A directed download to an individual CPA takes longer to complete. The affected CPA comes into service only after the directed download is successfully completed.

6.2 LOSS OF CPA — EFFECT ON SERVICE

A system can have CPAs mounted in any Port Subrack. Depending on the application, loss of the only CPA in a system may block call originations through the switch. If one CPA fails in a system with multiple CPAs, grade of service performance will suffer but calls can be processed. Call set-up time may increase as delays in mapping call progress tone monitor ports occur.

NOTE: All CPAs must be put into a single system Resource Group.

Refer to the *VCO/4K System Administrator's Guide* for information on accessing and using the Service Circuit Test Utility.

7.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the CPA, refer to the following publications.

7.1 VCO/4K SYSTEMS

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference
- VCO/4K Host Application Development Series
- VCO/4K Maintenance Manual

Digital Conference Card (DCC)

1.0 GENERAL

The Digital Conference Card (DCC) is a standard system service circuit card that resides in the Master or any Expansion Port Subrack. It allows voice paths to be bridged together for conference calling purposes. The DCC performs all tasks associated with adding callers under host control and tearing down the conference as callers leave the conference bridge. The system supports a maximum of eight two-way conferences, and an unlimited number of listeners.

Each DCC has 64 ports and an on-board processor. By mapping the third and subsequent interface ports (up to seven), conference calls with up to eight callers can be established through the system. Each party in the call will hear all the other participants in the call. Callers are automatically removed from the bridge as they disconnect, or may be removed and optionally idled by host command.

To allow adjustment of transmission levels, the DCC provides scaling factors which may be applied to each of the input ports individually and to each output sum as a whole. These scaling factors are controlled by host command.

2.0 SPECIFICATIONS

Optional Front Panel Kit:	45002350100 *(without extractors)*
Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM
	2K Bytes RAM
Power Requirements:	+5 Volts – 1400 mA (typical) -15 Volts: – 5 mA (typical)

3.0 DESCRIPTION

The DCC provides the system with conference call capability. The DCC has 64 independent output channels, also referred to as conference channels. Each channel adds up to seven PCM data values received from the PCM busses.

Scaling is provided independently for each of the seven inputs, and a second scaling factor can be applied to the resultant output for each channel. Three output channels are required for a three-party conference, four channels for a four-party conference, and so on. Conference call listeners require an additional output channel.

Figure 1 shows a simplified block diagram of the DCC.

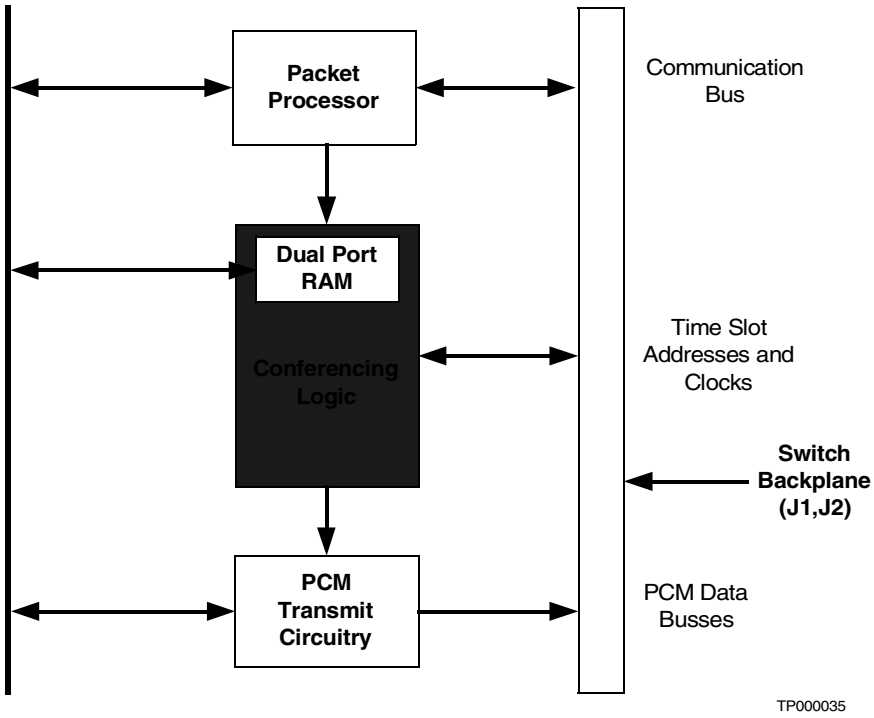


Figure 1: Block Diagram Of DCC

The following example shows a three-party conference setup with parties A, B, and C.

Channel 1 Add B+C

Channel 2 Add A+C

Channel 3 Add A+B

Party A Listen to the output of Channel 1 *(B+C)*

Party B Listen to Channel 2 *(A+C)*

Party C Listen to Channel 3 *(A+B)*

3.1 CONFERENCING LOGIC

Each frame, the Conferencing Logic reads all the PCM data from the switch backplane, selects the appropriate input PCM data for each conference channel, linearizes the selected PCM values, adds the linearized data values, converts the linear result back to PCM data, and outputs the data to the PCM Transmit Circuitry. A 13 MHz crystal oscillator provides the clock required for the Conferencing Logic state machine.

3.1.1 LINEARIZATION

The PCM data read from the Dual Port RAM (DPR) is converted to a linear value. The upper bits output by the channel setup RAM determine if any gain or attenuation is to be applied simultaneous with the linearization. The linearized data is input to the 16-bit, bit-slice processor. Seven linearized data values are read for each conference channel.

A scaling factor read from the channel setup RAM determines if gain or attenuation is to be applied during the conversion. The resulting PCM value is then loaded into the PCM Transmit Circuitry output DPR.

3.1.2 OUTPUT TO PCM TRANSMIT CIRCUITRY

The PCM-to-Linear EPROMs can output 14-, 15-, or 16-bit two's complement linear values. The Linear to PCM EPROMs are programmed to accept linear values of the same bit length. Different EPROM sets are required for µ-law and A-law PCM encoding methods. Jumper areas J7 and J8 allow configuration for different linear value bit widths.

The 8031 loads the channel setup RAMs with the information required for each channel. This information is retrieved as eight sixteen-bit values for each of the 64 conference channels. The input side address lines of the channel setup RAMs are directly connected to the 8031's address bus.

3.2 PCM TRANSMIT CIRCUITRY

The PCM Transmit Circuitry accepts PCM data from the Conferencing Logic and outputs the PCM data onto the selected PCM bus during the correct time slot addresses. The PCM Transmit Logic consists of: the output PCM data latches; the PCM output DPR; the input address counters; the time slot address and clock receivers; and the logic which compares the base address and time slot addresses to generate the output PCM data latch enable signals).

3.3 PACKET PROCESSOR

The DCC contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC).

The Packet Processor consists of the 8031 microcomputer, program and data memory, the Communication Bus Interface, an asynchronous serial port, and the LED register. The NBC issues commands to the DCC via the Communication Bus in the form of data "packets".

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the DCC.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

3.4 DCC STATUS LEDS

A red, a yellow, and a green LED are visible through the DCC's front panel to indicate the status of the card. Each LED is turned on when the software generic sets a bit low in an external memory register. Typically an illuminated red LED indicates a major card failure, an illuminated yellow LED indicates a minor card failure, and an illuminated green LED indicates the card is out of service or in the wrong, or an undefined, slot. (Refer to Section 6.01.)

3.5 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the DCC.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

Table 1: DCC J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused

Table 1: DCC J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

4.0 CONFIGURATION NOTES

The DCC is manufactured by Cisco Systems, Inc. Jumper plugs on the DCC are factory set for use in systems. Section 2 shows the location of jumper plugs and the PROM settings on a DCC card. Use this information to verify or reset jumpers on an interface card before installing it in a Port Subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

If a card is improperly configured, it may fail to operate. Therefore, great care must be taken to verify configuration settings before installing a replacement service circuit card in the system.

4.0.1 PROM LOCATIONS

NOTE 1

- Install jumper plug at J7 positions 1 and 4.
- Install jumper plug at J8 positions 3 and 6.
- Install jumper plug at J9 positions 1 and 8.
- Install jumper plug at J10 positions 1 and 8.

4.0.2 PROM1

The 2764 PROM in location U2 contains firmware appropriate to DCC polling and call processing requirements.

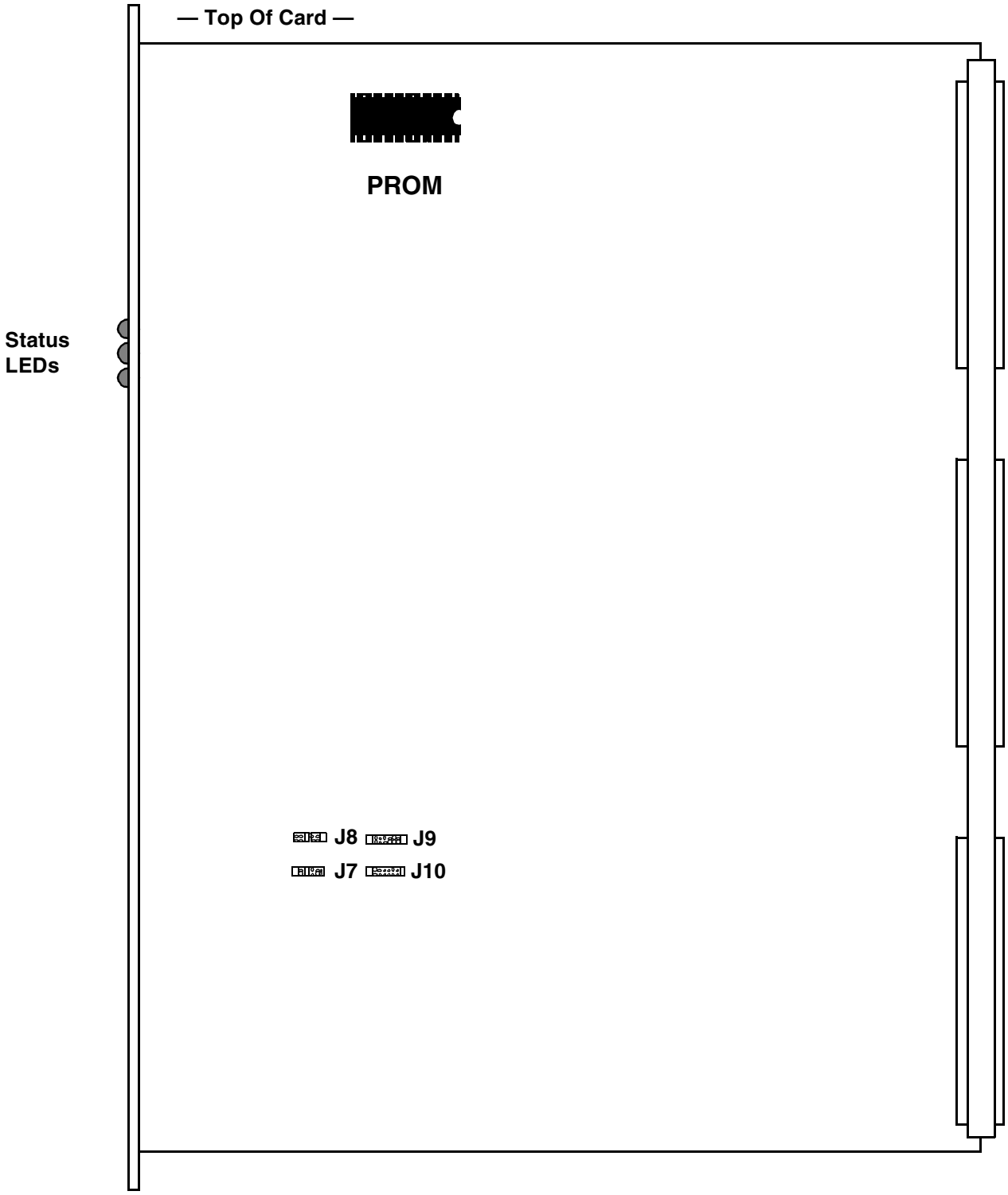


Figure 2: DCC Jumper and PROM Locations

5.0 TROUBLESHOOTING

The following subsection discusses troubleshooting the DCC.

5.1 LOSS OF DCC—EFFECT ON SERVICE

You can mount up to eight DCCs in any Port Subrack. Depending on the application, loss of the only DCC in a system may block call originations through the switch. If there are multiple DCCs in a system and one fails, service performance suffers but calls can be originated. Call set-up time may increase as delays in mapping conference ports occur.

NOTE: DCCs must be put into system Resource Groups.

6.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the DCC, refer to the following publications:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference
- VCO/4K Host Application Development Series: Conferencing
- VCO/4K Hardware Planning
- VCO/4K System Maintenance Manual

Digital Tone Generator Card (DTG)

1.0 GENERAL

The Digital Tone Generator (DTG) card is a standard service circuit card that resides in the master or expansion port subrack. It sources Dual Tone Multi-Frequency (DTMF), Multi-Frequency (MF), and call progress tones for in-band signalling. This card supports 63 outpulsing channels and 64 static tone channels that you can simultaneously access by any system port.

Individual tones are output in reserved port addresses (PA) that the system controller maps to another PA assigned to an interface circuit.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM2K Bytes RAM
Power Requirements:	**Typical** +5 Volts:1500 mA
Tone Channels Per Card:	127 (63 outpulse, 64 static)

Table 1 lists the tones provided with a DTG card. All tone levels are relative to 0 TLP.

Table 1: DTG Card Tones

Frequencies	Level	Tone
941 Hz + 1336 Hz	-7 dBm/freq	DTMF 0
697 Hz + 1209 Hz	-7 dBm/freq	DTMF 1
697 Hz + 1336 Hz	-7 dBm/freq	DTMF 2
697 Hz + 1447 Hz	-7 dBm/freq	DTMF 3
770 Hz + 1209 Hz	-7 dBm/freq	DTMF 4
770 Hz + 1336 Hz	-7 dBm/freq	DTMF 5
770 Hz + 1447 Hz	-7 dBm/freq	DTMF 6
852 Hz + 1209 Hz	-7 dBm/freq	DTMF 7
852 Hz + 1336 Hz	-7 dBm/freq	DTMF 8
852 Hz + 1447 Hz	-7 dBm/freq	DTMF 9
697 Hz + 1633 Hz	-7 dBm/freq	DTMF A

Table 1: DTG Card Tones (Continued)

Frequencies	Level	Tone
770 Hz + 1633 Hz	-7 dBm/freq	DTMF B
852 Hz + 1633 Hz	-7 dBm/freq	DTMF C
941 Hz + 1633 Hz	-7 dBm/freq	DTMF D
941 Hz + 1209 Hz	-7 dBm/freq	DTMF *
941 Hz + 1477 Hz	-7 dBm/freq	DTMF #
1300 Hz + 1500 Hz	-7 dBM/freq	MF 0
700 Hz + 900 Hz	-7 dBM/freq	MF 1
700 Hz + 1100 Hz	-7 dBM/freq	MF 2
900 Hz + 1100 Hz	-7 dBM/freq	MF 3
700 Hz + 1300 Hz	-7 dBM/freq	MF 4
900 Hz + 1300 Hz	-7 dBM/freq	MF 5
1100 Hz + 1300 Hz	-7 dBM/freq	MF 6
700 Hz + 1500 Hz	-7 dBM/freq	MF 7
900 Hz + 1500 Hz	-7 dBM/freq	MF 8
1100 Hz + 1500 Hz	-7 dBM/freq	MF 9
1100 Hz + 1700 Hz	-7 dBM/freq	MF KP
1500 Hz + 1700 Hz	-7 dBM/freq	MF ST
700 Hz + 1700 Hz	-7 dBM/freq	MFSTP3P
900 Hz + 1700 Hz	-7 dBM/freq	MFSTP
1300 Hz + 1700 Hz	-7 dBM/freq	MFST2P
–	–	Quiet
350 Hz + 440 Hz	-13 dBm/freq	Dial tone
440 Hz + 480 Hz	-19 dBm/freq	Ringback (steady)
480 Hz + 620 Hz	-24 dBm/freq	Busy tone
380 Hz	-10 dBm	Digit trip
440 Hz	-13 dBm	
480 Hz	-17 dBm	High tone
920 Hz	-13 dBm	
1400 Hz	-24 dBm	

Table 1: DTG Card Tones (Continued)

Frequencies	Level	Tone
1760 Hz	-10 dBm	Pay phone trigger tone
1000 Hz	0 dBm	CCITT tone
1000 Hz	Maximum output	Test tone
404 Hz	0 dBm	Test tone
1004 Hz	0 dBm	Test tone
2804 Hz	0 dBm	Test tone
440 Hz + 480 Hz	-19 dBm/freq	Ringback (2 sec ON/ 4 sec OFF)
480 Hz + 620 Hz	-24 dBm/freq	Busy (.5 sec ON/ .5 sec OFF)
480 Hz + 620 Hz	-24 dBm/freq	Reorder (.25 sec ON/ .25 sec OFF)
380 Hz		NAK (1 sec ON/ 1 sec OFF)
–	-10 dBm/freq starting level	Cyclic bong tone (repeated every 3.25 sec)
1780 Hz	-12 dBm	ISUP continuity test tone
2010 Hz	-12 dBm	ISUP continuity test tone

3.0 CIRCUIT DESCRIPTION

DTG cards are typically located in the third and fourth slots of the Master Port Subrack. The DTG provides the necessary call processing tones, including DTMF and MF, call progress (dial tone, quiet, busy, audible ring), and test. All tones are generated as PCM data and output on a PCM data bus. The DTG supports 128 channels. The tone output by each channel can be programmed. Once a channel is programmed, it outputs the selected tone until reprogrammed.

Figure 1 shows a simplified block diagram of the DTG.

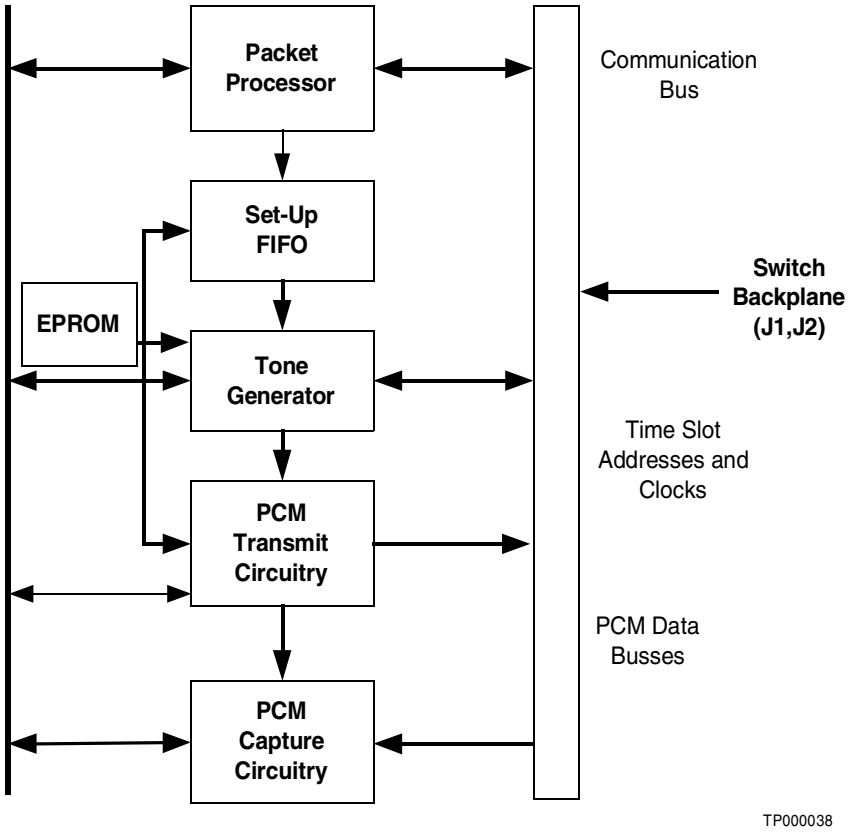


Figure 1: DTG Block Diagram

3.1 TONE GENERATOR OPERATION

Any tone channel can output a constant tone or a constantly changing tone, such as a busy signal. Additionally, a tone can be used as an outpulse channel for outpulsing MF or DTMF digits. After power-up or card reset, the DTG is initialized. The following limitations apply to tone setups:

- At least five microseconds must elapse between each tone setup.
- A channel must not be repeatedly programmed with the same tone number. The quiet tone is the only exception to this rule. Repeatedly setting up the same tone causes a clicking sound in the tone.

3.1.1 TONE GENERATOR CIRCUITRY

The Tone Generator Circuitry consists of vector RAMs, vector RAM address counters, a bank of up/down counters for address calculation, EPROMs for storing each tone's PCM data values, and a state machine that controls the tone generator.

The vector RAM has a 16-bit location for each tone channel enabled. Each vector RAM address location contains the EPROM address of the PCM data byte to be transmitted for the current frame during the time slot assigned to the tone channel. The PCM data generated by the tone generator is stored in the PCM data output FIFO for transmission onto the tone or voice PCM data bus.

3.1.2 STATE MACHINE

The state machine controls each action of the tone generator. States are identified by the output of the state machine counter. The state machine counter is incremented every clock pulse. A 16 MHz crystal oscillator module's output is divided by to yield the 8 MHz clock used by the state machine.

3.1.3 PCM TRANSMIT CIRCUITRY

The PCM Transmit Circuitry consists of the PCM data output FIFO and the logic necessary to output the contents of the FIFO onto the selected PCM bus during the correct time slots. It also includes the circuitry required to allow the DTG to operate 8, 16, 32, 64, or 128 tone channels.

The vector RAM address signals are also used to address the PCM output FIFO when PCM data is being written from the Tone Generator. The time slot address is modified to allow ample time to get data from the FIFO, through the buffer register, and into the output registers.

3.1.4 PCM TONES

Tones are stored in the EPROM as a series of PCM values. The tones listed in *Section 2.0* are generated using µ-law PCM encoding. Different versions of the PCM data storage EPROM are required to support A-law PCM encoded tones. The number of values to define a tone is determined by the characteristics of that tone. For each PCM value, a corresponding counter reference value is stored in the EPROM.

Refer to the *Programming Reference* for additional details on accessing DTG tones.

3.2 PACKET PROCESSOR

The DTG contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC).

The Packet Processor consists of the 8031 microcomputer, program and data memory, the Communication Bus Interface, an asynchronous serial port, and the LED register. The NBC issues commands to the DTG via the Communication Bus in the form of data packets.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry, the Communication Bus Interface, an asynchronous serial port, and the LED register. The 8031 provides the intelligence for the Packet Processor and the DTG.

3.3 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 2 lists the J1 pin assignments on the DTG card.

NOTE: J2 pin assignments are proprietary and not included in customer documentation.

Table 2: DTG J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return

Table 2: DTG J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24 V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog (-15V)	Unused	Analog (-15V)
19	Analog (-15V)	Unused	Analog (-15V)
20	Analog (+15V)	Unused	Analog (+15V)
21	Analog (+15V)	Unused	Analog (+15V)
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

4.0 CONFIGURATION NOTES

The DTG is configured by Cisco Systems, Inc. Figure 2 shows the location of the PROM chips that controlling DTG operation. Use this information to verify the correct positioning of the PROMs on the circuit board prior to installing it in a Port Subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

PROM Locations

> *NOTE: There are no jumper options on the DTG card that must be set to meet customer requirements.*

PROM 1

The 2764 PROM in location U2 contains firmware appropriate to DTG polling and call processing requirements.

PROM 2

The 27128 PROM in location U53 contains firmware labelled "Tone `Even`".

PROM 3

The 27128 PROM in location U54 contains firmware labelled "Tone `Odd`".

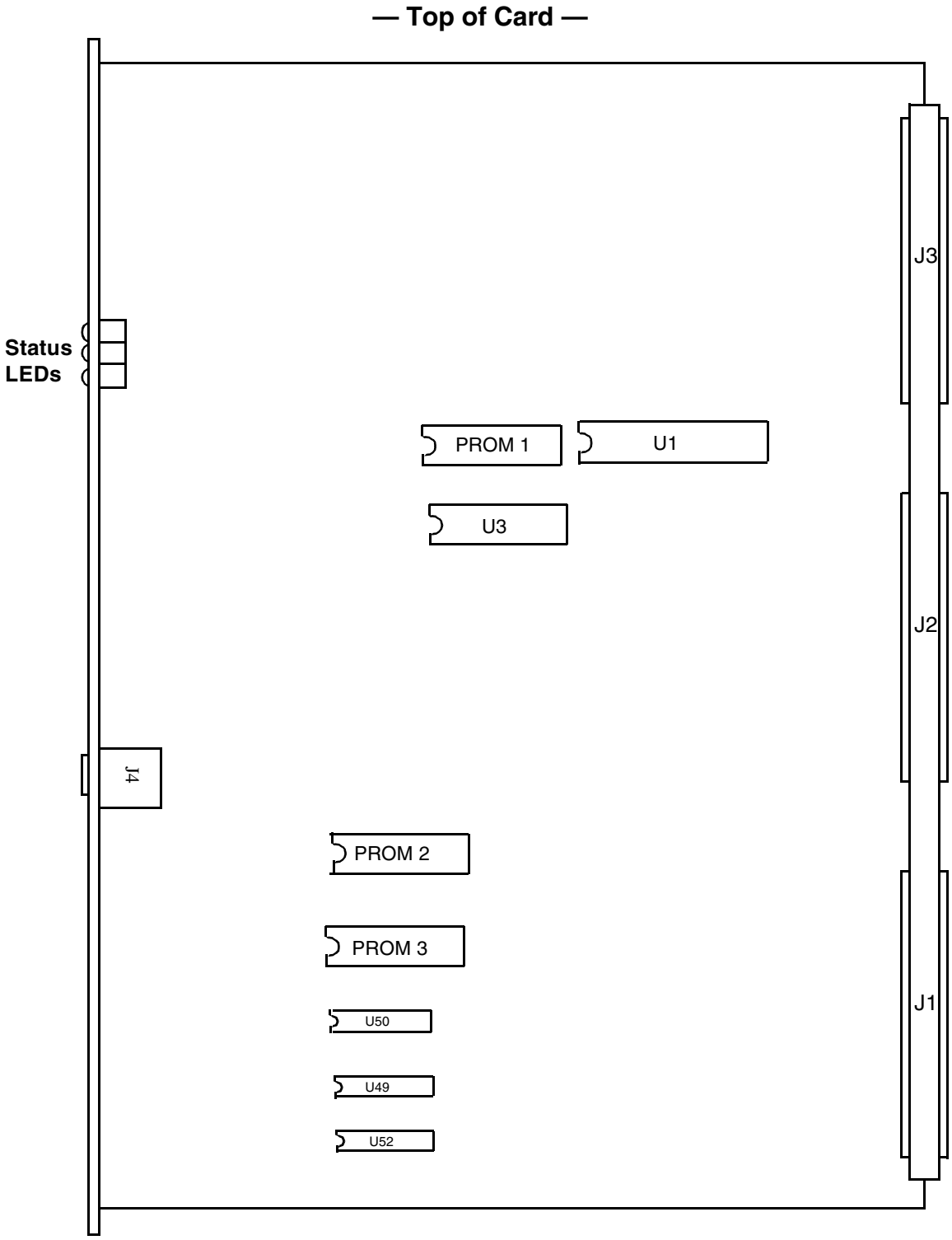


Figure 2: DTG PROM Locations

The DTG can be safely removed and replaced with the system powered-up and operating normally. It should be in Out-of-Service (OOS) status to assure that in-progress calls are not affected when the card is removed from a Port Subrack.

CAUTION: At least one DTG must be in-service for the system to process calls.

NOTE: The procedures for removing and replacing the DTG card assume that the cards are being replaced with identical cards meeting the data base parameters.

5.0 TROUBLESHOOTING

The following section discusses troubleshooting guidelines for the DTG card.

5.1 RESETTING A DTG CARD

A redundant system has two or more DTG cards mounted in Slot 3 and 4 of the Master Port Subrack. One DTG is active while the other remains in standby mode. The current DTG status is displayed on the Card Maintenance Menu

If the Yellow LED illuminates, on a DTG, during normal system operation, reset the card using the Card Maintenance Menu. Select that DTG and change the card status to Out-of-Service.

NOTE: If there is only one DTG card currently in service, you cannot change the card status to Out -of-Service.

The system automatically activates a standby DTG card, and switches the active DTG to Out-of-Service. A minor alarm occurs; the alarm clears when the DTG cards assume the new operating status.

To reset the Out-of-Service DTG card, change the status to Active on the Card Maintenance menu. The DTG is placed in Standby mode for approximately four minutes.

6.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the DTG, refer to the following publications:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference
- VCO/4K Hardware Planning Guide
- VCO/4K System Maintenance Manual

Digital Tone Generator 2 Card (DTG-2)

1.0 GENERAL

The Digital Tone Generator 2 (DTG-2) card is a mezzanine card for the NBC-3. The DTG-2 has the same functionality as the full size DTG card, but is smaller and does not require a card slot.

The DTG-2 mezzanine card can coexist with the full size DTG card to allow redundant tone generation in a nonredundant system. The two cards exist in a modified n+1 redundant scheme, which allows the two cards to be present in the system database. However, only one of the DTG or DTG-2 cards can be active and generating tones at any one time.

The NBC-3 supports one DTG-2 mezzanine card. Therefore, the maximum number of DTG-2 cards in a nonredundant system is one, and the maximum number in a redundant system is two.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM 2K Bytes RAM
Power Requirements:	+5 Volts:1500 mA (Typical)
Tone Channels Per Card:	127 (63 outpulse, 64 static)

3.0 CIRCUIT DESCRIPTION

The DTG-2 provides all tones required for call processing, including Dual Tone Multi-Frequency (DTMF), Multi-Frequency (MF), and call progress tones for in-band signaling. The DTG-2 supports 63 outpulsing channels and 64 static tones that can be simultaneously accessed by any system port.

Individual tones are output in reserved Port Addresses (PAs), which the system controller maps to another PA assigned to an interface circuit.

DTG-2 tones are generated as pulse code modulation (PCM) data and output on a PCM data bus. The tone output by each channel can be programmed. Once a channel is programmed, it outputs the selected tone until reprogrammed.

Figure 1 is a block diagram of the DTG-2.

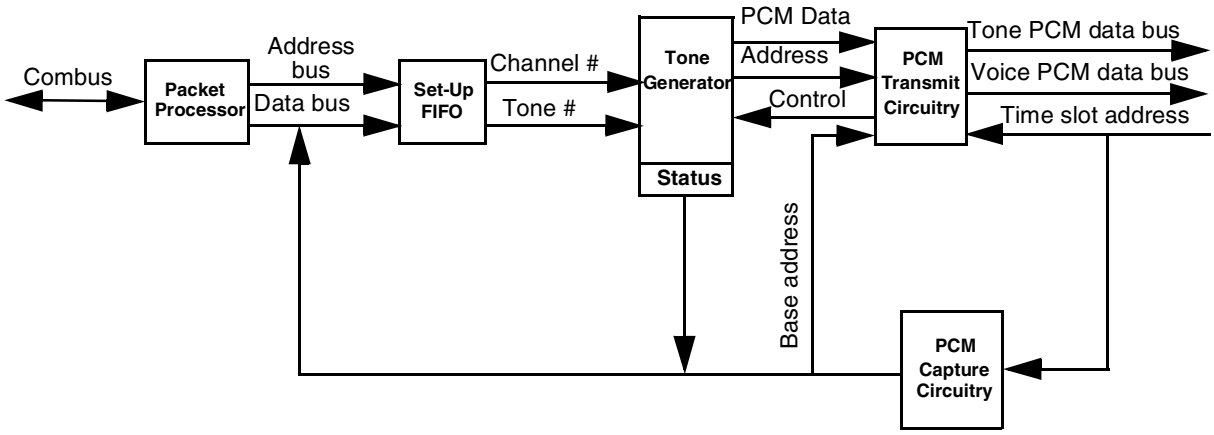


Figure 1: DTG-2 Block Diagram

3.1 TONE GENERATOR OPERATION

Any tone channel on the DTG-2 can output a constant tone or a constantly changing tone, such as a busy signal. Additionally, a tone can be used as an outpulse channel for outpulsing MF or DTMF digits. After power-up or card reset, the DTG-2 is initialized. However, the following limitations apply to tone setups:

- At least five microseconds must elapse between each tone setup.
- A channel must not be repeatedly programmed with the same tone number. The quiet tone is the only exception to this rule. Repeatedly setting up the same tone causes a clicking sound in the tone.

Table 1 lists the tones provided by the DTG-2 card with the North American PROM set. All tone levels are relative to transmission level point 0.

Table 1: DTG-2 Tones

Tone	Frequencies	Level
DTMF 0	941 Hz + 1336 Hz	-7 dBm/freq
DTMF 1	697 Hz + 1209 Hz	-7 dBm/freq
DTMF 2	697 Hz + 1336 Hz	-7 dBm/freq
DTMF 3	697 Hz + 1447 Hz	-7 dBm/freq
DTMF 4	770 Hz + 1209 Hz	-7 dBm/freq
DTMF 5	770 Hz + 1336 Hz	-7 dBm/freq
DTMF 6	770 Hz + 1447 Hz	-7 dBm/freq
DTMF 7	852 Hz + 1209 Hz	-7 dBm/freq
DTMF 8	852 Hz + 1336 Hz	-7 dBm/freq
DTMF 9	852 Hz + 1447 Hz	-7 dBm/freq
DTMF A	697 Hz + 1633 Hz	-7 dBm/freq
DTMF B	770 Hz + 1633 Hz	-7 dBm/freq
DTMF C	852 Hz + 1633 Hz	-7 dBm/freq
DTMF D	941 Hz + 1633 Hz	-7 dBm/freq
DTMF *	941 Hz + 1209 Hz	-7 dBm/freq
DTMF #	941 Hz + 1477 Hz	-7 dBm/freq
MF 0	1300 Hz + 1500 Hz	-7 dBM/freq
MF 1	700 Hz + 900 Hz	-7 dBM/freq
MF 2	700 Hz + 1100 Hz	-7 dBM/freq
MF 3	900 Hz + 1100 Hz	-7 dBM/freq
MF 4	700 Hz + 1300 Hz	-7 dBM/freq
MF 5	900 Hz + 1300 Hz	-7 dBM/freq
MF 6	1100 Hz + 1300 Hz	-7 dBM/freq
MF 7	700 Hz + 1500 Hz	-7 dBM/freq
MF 8	900 Hz + 1500 Hz	-7 dBM/freq
MF 9	1100 Hz + 1500 Hz	-7 dBM/freq
MF KP	1100 Hz + 1700 Hz	-7 dBM/freq
MF ST	1500 Hz + 1700 Hz	-7 dBM/freq
MFSTP3P	700 Hz + 1700 Hz	-7 dBM/freq
MFSTP	900 Hz + 1700 Hz	-7 dBM/freq
MFST2P	1300 Hz + 1700 Hz	-7 dBM/freq
Quiet	–	–

Table 1: DTG-2 Tones(Continued)

Tone	Frequencies	Level
Dial tone	350 Hz + 440 Hz	-13 dBm/freq
Ringback (steady)	440 Hz + 480 Hz	-19 dBm/freq
Busy tone	480 Hz + 620 Hz	-24 dBm/freq
Digit trip	380 Hz	-10 dBm
	440 Hz	-13 dBm
High tone	480 Hz	-17 dBm
	920 Hz	-13 dBm
	1400 Hz	-24 dBm
Pay phone trigger tone	1760 Hz	-10 dBm
CCITT tone	1000 Hz	0 dBm
Test tone	1000 Hz	Maximum output
Test tone	404 Hz	0 dBm
Test tone	1004 Hz	0 dBm
Test tone	2804 Hz	0 dBm
Ringback (2 sec ON/ 4 sec OFF)	440 Hz + 480 Hz	-19 dBm/freq
Busy (.5 sec ON/ .5 sec OFF)	480 Hz + 620 Hz	-24 dBm/freq
Reorder (.25 sec ON/ .25 sec OFF)	480 Hz + 620 Hz	-24 dBm/freq
NAK (1 sec ON/ 1 sec OFF)	380 Hz	
Cyclic bong tone (repeated every 3.25 sec)	–	-10 dBm/freq starting level
ISUP continuity test tone	1780 Hz	-12 dBm
ISUP continuity test tone	2010 Hz	-12 dBm

For information on the tones provided by the DTG-2 with other country PROM sets, refer to the appropriate Country Supplement. For information on accessing DTG-2 tones, refer to the *VCO/4K Standard or Extended Programming Reference.*

3.2 PACKET PROCESSOR

The DTG-2 contains an 8031-based packet processor that interfaces to the Combus. (A packet processor is part of all service circuit and port interface cards.) In addition to the 8031 microcomputer, the packet processor consists of program and data memory, Combus interface, an asynchronous serial port, and the LED register. The NBC-3 issues commands to the DTG-2 via the Combus in the form of data packets.

The packet processor supports a diagnostic serial port connected to the front panel of the NBC-3 card. The packet processor also controls three status LEDs (red, yellow, and green) which are visible through the NBC-3 card front panel.

3.3 REDUNDANCY

If a DTG-2 fails in a non-redundant system, calls cannot be completed, a major alarm is triggered, and a Phase 4 reboot occurs.

In redundant systems, the redundant DTG-2 is in standby status during normal operation. If the primary DTG-2 fails, the other is automatically placed in active service to process calls. A minor alarm is triggered to indicate the need to service the failed DTG-2.

Note the following:

- If the active NBC-3 card switches to standby, and the DTG-2 mounted on that NBC-3 is active, the DTG-2 also switches to standby.
- An active DTG-2 does not switch with its NBC-3 if the standby DTG-2 has failed, or if there is no standby DTG-2.
- If the active DTG-2 switches to standby, the corresponding NBC-3 does *not* switch with it.
- If you remove the NBC-3 card, the DTG-2 mounted on that NBC-3 is also removed.
- To remove the DTG-2 card, the NBC-3 on which it is mounted must be removed.
- Remove the corresponding Combined Controller before removing the NBC-3.

Note that in two cases listed above (bullets 2 and 3), the NBC-3 and DTG-2 could be active on different sides, even though they are located on the same card. In the event that you have to remove and replace a problem NBC-3 or DTG-2, make certain you know the current active configuration of your system.

3.4 DTG-2 STATUS LEDS

The DTG-2 LEDs are visible through the NBC-3 card front panel as shown in Figure 2.

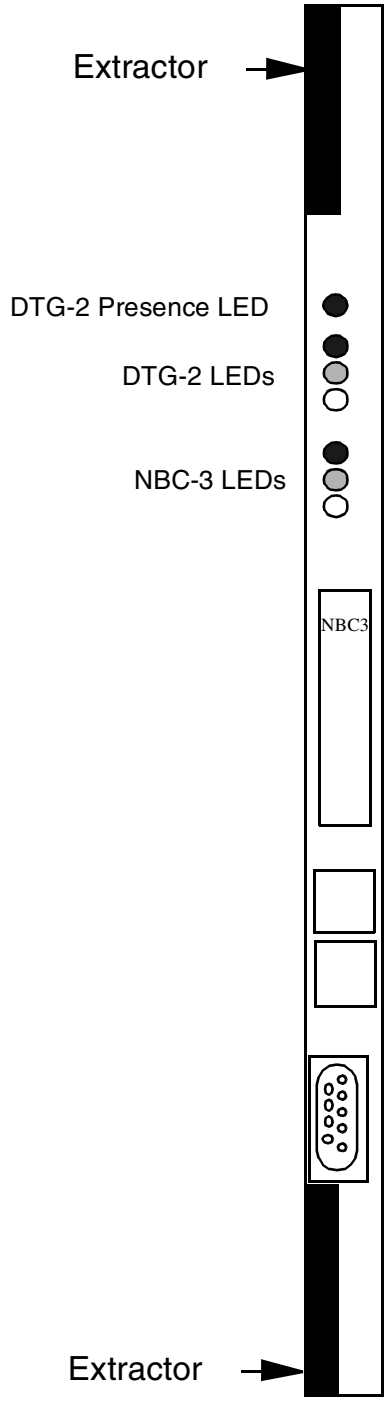


Figure 2: DTG-2 LEDs Visible From The NBC-3 Card Front Panel

The DTG-2 Presence LED is ON when a DTG-2 mezzanine card is installed on the NBC-3 card. The other DTG-2 LEDs generally indicate the following:

Red On—Major card failure

Yellow On—Minor card failure

Green On—Standby or diagnostic mode

4.0 CONFIGURATION NOTES

The DTG-2 is configured by Cisco Systems, Inc. Figure 3 shows the location of the PROM chips that control DTG-2 operation. Use this information to verify the correct positioning of the PROMs on the circuit board prior to installing it on an NBC-3.

There are no jumper options on the DTG-2 card that must be set to meet customer requirements.

PROM 1—The 2764 PROM in location **U2** contains firmware appropriate to DTG-2 polling and call processing requirements.

PROM 2—The 27128 PROM in location **U53** contains firmware labelled **Tone Even**.

PROM 3—The 27128 PROM in location **U54** contains firmware labelled **Tone Odd**.

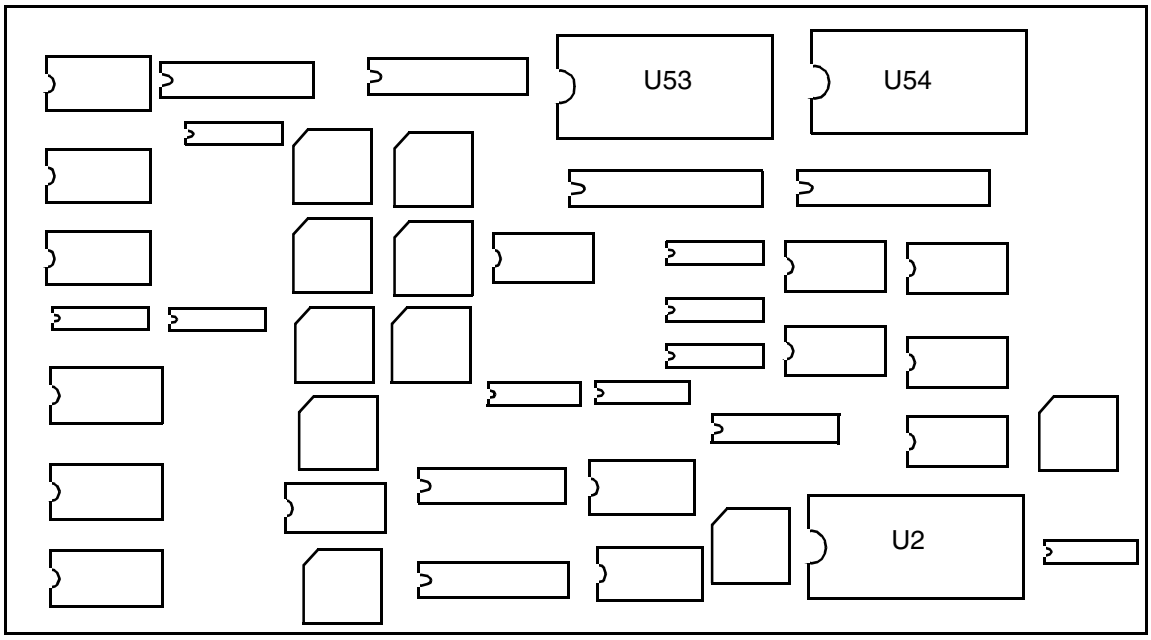


Figure 3: DTG-2 PROM Locations

5.0 DTG-2 REMOVAL AND REPLACEMENT PROCEDURES

You can remove and replace the NBC-3 with the DTG-2 mezzanine card with the system powered-up.

CAUTION: At least one NBC-3 and DTG or DTG-2 must be in-service for the system to process calls.

NOTE: The procedures for removing and replacing the DTG-2 card assume that the cards are being replaced with identical cards meeting the data base parameters.

CAUTION: Observe antistatic precautions when handling the NBC-3 and DTG-2 to avoid damaging sensitive CMOS devices. Wear a ground strap connected to the system equipment frame whenever removing or replacing circuit cards.

5.1 REMOVING A DTG-2 CARD

To remove the DTG-2 mezzanine card, complete the following steps:

1. From the Card Maintenance submenu, change the DTG-2 card status to Out-of-Service. (Refer to the *System Administrator's Guide* for more information.) Wait for the green DTG-2 LED on the front panel of the NBC-3 card to light.
2. If you have a redundant system, verify that the NBC-3 and DTG-2 mezzanine card you want to remove are on the Standby side. If the cards are not in the Standby side, run the Switch Active Side to Standby Utility as described in the *VCO/4K System Administrator's Guide*
3. If the utility does not switch the system over, flip the **SELECT** toggle on the AAC to force the system to switchover. (Refer to the *Alarm Arbiter Card (AAC) With Alarm Interface Card (AIC) Technical Description* for more information.)
4. If you have a non-redundant system, shut down the system. If you have a redundant system, shut down the Standby side.
5. Disable the external alarm system to which the AAC might be connected.
6. Disconnect all cables that are attached to the card (for example, BITS clock cable.)
7. Use your thumbs to pull the upper and lower extractors away from the card front panel. This action extracts the card from the backplane connectors.
8. Pull the NBC-3 free of the card slot.
9. After you have removed the NBC-3 card from the system, placed it component side up, on an antistatic mat or an antistatic envelope.
10. Firmly grasp the DTG-2 mezzanine card and pull the mezzanine card away from the NBC-3. Do not exert excessive force on the mezzanine card to remove it from the NBC-3.

    NOTE: Excessive force can seriously damage connectors and result in operating problems.
11. Place the removed DTG-2 mezzanine card on an antistatic mat or envelope.

5.2 REPLACING A DTG-2 CARD

To replace the DTG-2, complete the following steps:

1. Verify that all the proms on the new card correspond with those on the card you just removed. Refer to *Section 4.0* for details on PROM locations.

   NOTE: Refer to release notes to verify that the revision level of the PROMs match the requirements of the version of Generic software currently loaded in the system.

2. Align the mezzanine card with the mezzanine socket on the NBC-3 card and push the card downward until it makes contact with the NBC-3.
3. Grasp the replacement NBC-3 by the top handle and the bottom edge and align it with the top and bottom card guides of the subrack.
4. Be sure the extractor levers are perpendicular to the front panel. Push the NBC-3 in until it makes contact with the master port subrack backplane. The hooks on the extractors must be behind the front rail of the subrack. Use your thumbs to push the extractors toward the front panel.
5. If you are using the BITS clock option, reconnect the clock source to the DB-9 connector on the NBC-3 front panel.
6. If you have a have a nonredundant system, reboot the system. If you have a redundant system, reboot the Standby side. (Refer to the *VCO/4K System Maintenance Manual* for more information.)
7. Enable the external alarm system connected to the AAC terminals.
8. If you have a redundant system, flip the **SELECT** toggle switch on the ACC in the **A**, **B** or **AUTO** position, as desired.

   If you have a nonredundant system, reset the system as described in the *System Maintenance Manual.*
9. The DTG-2 is automatically brought into service when the NBC-3 is downloaded. If the DTG-2 card fails to automatically come into service, change the card status to Active from the master console Card Maintenance submenu. (Refer to the *VCO/4K System Administrator's Guide* for more information.)

6.0 TROUBLESHOOTING

The following sections discuss troubleshooting guidelines for the DTG-2 card.

6.1 DETECTING AND CORRECTING DTG-2 PROBLEMS

DTG-2 LEDs on the NBC-3 front panel and system error messages provide quick indications of the DTG-2 mezzanine card status. The DTG-2 status is indicated by the following LEDs:

DTG-2 Presence LED On—DTG-2 is installed on NBC-3

Red On—Self-test failure; out-of-service

Yellow On—Data overrun between the NBC-3 and the control circuit cards

Green On—Out-of-service or standby mode; can be removed from the NBC-3

6.2 RESETTING A DTG-2 CARD ON REDUNDANT SYSTEMS

A redundant system has two DTG-2 cards. One DTG-2 is active while the other remains in standby mode. The current DTG-2 status is displayed on the Card Maintenance Menu.

If the Yellow DTG-2 LED is on during normal system operation, reset the card from the Card Maintenance Menu of the master console. Select that DTG-2 card and change the card status to Out-of-Service. (Refer to the *System Administrator's Guide* for more information.) The system automatically activates a standby DTG-2 card, and switches the active DTG-2 to Out-of-Service. A minor alarm occurs; the alarm clears when the DTG-2 cards assume the new operating status.

To reset the Out-of-Service DTG-2 card, change the status to Active on the Card Maintenance menu. The DTG-2 is placed in Standby mode for approximately four minutes.

7.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation, and maintenance of the DTG-2, refer to the following documents:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference
- VCO/4K Hardware Planning Guide
- VCO/4K System Maintenance Manual
- Network Bus Controller 3 (NBC-3) Technical Description

DTMF Receiver Card (DRC-8)

1.0 GENERAL

The DTMF Receiver Card (DRC) is a standard service circuit card that resides in the Master or any Expansion Port Subrack. It includes eight Dual Tone MultiFrequency (DTMF) receiver circuits; that are available for assignment to calls as needed. DRC ports are allocated and released during a call as specified by the call processing application.

The number and type of receiver cards required by a system is based on anticipated traffic and the call scenario. DRCs are microprocessor-based, firmware controlled, and incorporate the standard internal control and digital network interface.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM 2K Bytes RAM
Power Requirements:	**Typical** +5 Volts:400 mA +15 Volts:100 mA –15 Volts:110 mA
DTMF Receiver:	þþ Detectable input level-29 dBm minimum 2 dBm maximum Acceptable twist 10 dB maximum Tone or quiet duration 50 mS minimum

Detected Digits:

DTMF Digit 1	697 Hz + 1209 Hz
DTMF Digit 2	697 Hz + 1336 Hz
DTMF Digit 3	697 Hz + 1447 Hz
DTMF Digit 4	770 Hz + 1209 Hz
DTMF Digit 5	770 Hz + 1336 Hz
DTMF Digit 6	770 Hz + 1447 Hz
DTMF Digit 7	852 Hz + 1209 Hz
DTMF Digit 8	852 Hz + 1336 Hz
DTMF Digit 9	852 Hz + 1447 Hz
DTMF Digit 0	941 Hz + 1336 Hz
DTMF Digit *	941 Hz + 1209 Hz
DTMF Digit #	941 Hz + 1447 Hz

3.0 CIRCUIT DESCRIPTION

The DRC provides systems with eight DTMF digit receivers. These receivers are typically used when DTMF digit signalling must be decoded on T1 and E+M type incoming trunks. UTC-2, SLIC-2 and DID-2 cards have a DTMF receiver per port and do not require DTMF receiver cards for DTMF digit collection.

Each DRC port can independently listen to any time slot on either PCM data bus. For a typical call setup, a DTMF receiver port is assigned by software to listen to the output of a T1 or E+M card and report any digits that are received. When the DTMF Receiver is no longer needed, the port is assigned to listen to quiet.

Figure 1 shows a simplified block diagram of the DRC.

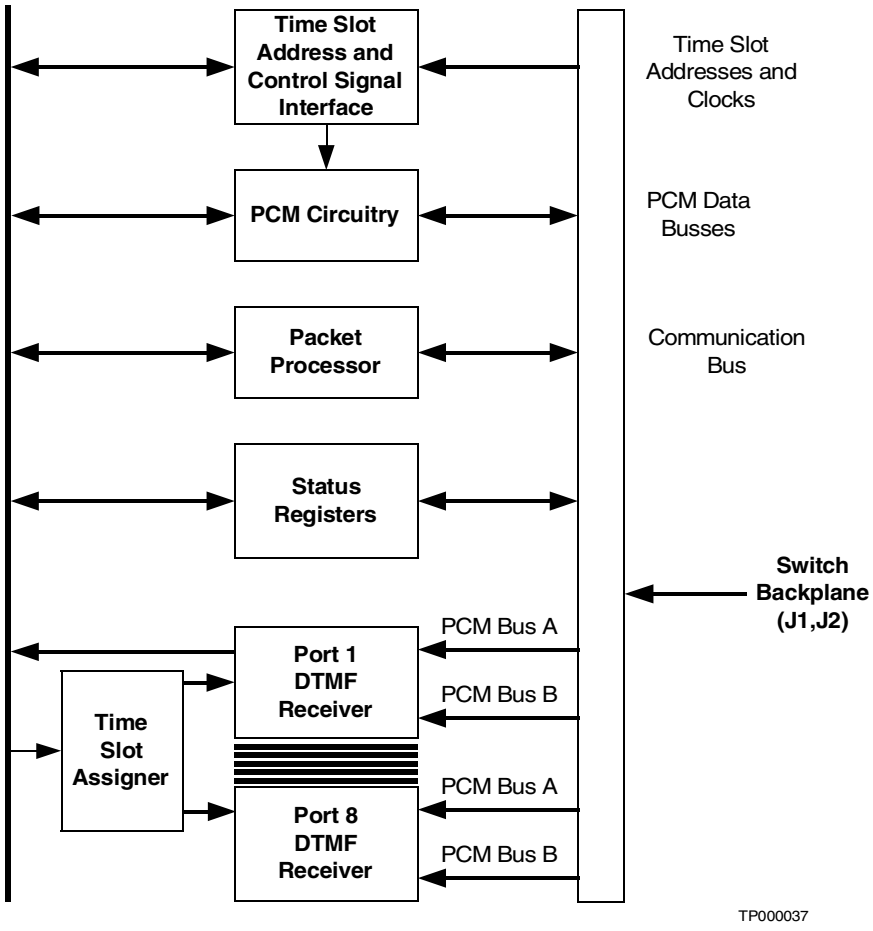


Figure 1: Block Diagram Of DRC

3.1 DTMF DIGIT RECEIVER

A DTMF digit receiver integrated circuit (I.C.) is provided for each DID port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within the system is encoded and transmitted as Pulse Code Modulated (PCM) data. Each DTMF receiver port contains a coder/decoder (codec) to translate PCM data into an analog signal. This signal is monitored by a DTMF receiver integrated circuit (I.C.). The DRC interfaces to the PCM time slot bus structure with bus interface circuitry which is common to system port cards.

When a DRC is plugged into a Port Subrack backplane it is automatically assigned a set of eight consecutive port addresses. The PCM data and time slot bus interfaces control the capture of the correct PCM data for reception by each DTMF receiver port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The DRC contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC).

The Packet Processor consists of the 8031 microcomputer, program and data memory, the Communication Bus Interface, an asynchronous serial port, and the LED register. It is via the Communication Bus that the NBC issues commands to the DRC in the form of data packets. The DRC reports the status of its DTMF digit receivers over the same bus and using the data packet protocol. When polled by the NBC, the Packet Processor reports any status change.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the DRC.

3.4 DRC STATUS LEDS

A red, a yellow, and a green LED are visible through the DRC's front panel to indicate the status of the card. Each LED is turned on when the software generic sets a bit low in an external memory register. Typically an illuminated red LED indicates a major card failure, an illuminated yellow LED indicates a minor card failure, and an illuminated green LED indicates the card is in standby or diagnostic mode (refer to *Section 6.01*).

3.5 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the DRC.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

Table 1: DRC J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V

Table 1: DRC J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

4.0 CONFIGURATION NOTES

The DRC is manufactured by Cisco Systems, Inc. Jumper plugs on the DRC are factory set for use in systems. Figure 3 indicates the location and correct installation of jumper plugs. Use this information to verify or reset jumpers on an interface card prior to installing it in a Port Subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

If a card is improperly configured, it may fail to operate. Therefore, great care must be taken to verify configuration settings before installing a replacement service circuit card in the system.

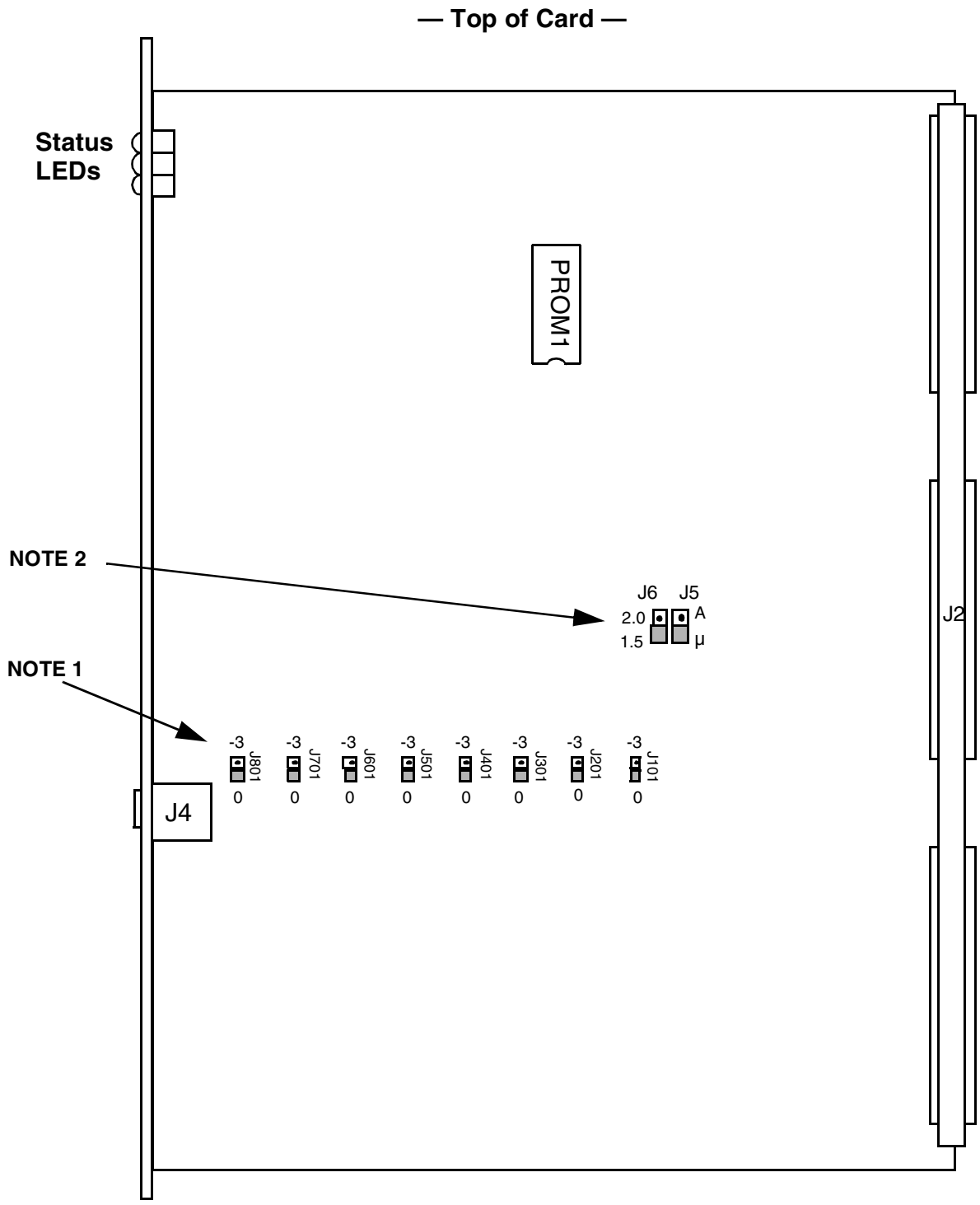


Figure 2: DRC Jumper & PROM Locations

4.0.1 JUMPER LOCATIONS

NOTE 1

Eight identical jumper locations (JX01) are provided; one for each circuit supported by the card. The locations are labelled J101 through J801.

- Install jumper plug in Position 0; Position -3 is not used.

NOTE 2

- Install jumper plug at J5 in the U position for codec µ-law operation (North American standard).
- Install jumper plug at J5 in the A position for codec A-law operation (European standard).
  Position U (µlaw) is the factory default setting for J5.
- Install the jumper plug at J6 in the 1.5 position for 1.544MHz codec clock (North American standard).
- Install the jumper plug at J6 in the 2.0 position for 2.048MHz codec clock (European standard).
  Position 1.5 (1.544MHz) is the factory default setting for J6.

PROM

The 2764 PROM in location U2 contains firmware appropriate to DRC polling and call processing requirements.

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the DRC, refer to the following system publications:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference
- VCO/4K Hardware Planning Guide
- VCO/4K System Maintenance Manual

INTEGRATED PROMPT/RECORD CARD (IPRC)

1.0 GENERAL

The Integrated Prompt/Record Card (IPRC) is a standard system service circuit card that resides in the Master or any Expansion Port Subrack. It is designed for the system switching product family to play and record digitized voice prompt information. The IPRC is available with the following port configurations:

- 8 playback/4 record ports
- 64 playback/32 record ports
- 128 playback/32 record ports

The IPRC can play voice information on up to 128 channels and record from up to 32 channels. All channels can operate simultaneously. The IPRC supports up to 16 prompt libraries of up to 256 prompts each.

The number and type of IPRCs required by a system is based on anticipated traffic and the call scenario. IPRCs are microprocessor-based and firmware controlled, and are incorporated with the standard system internal control and digital network interfaces.

2.0 SPECIFICATIONS

Microprocessor	MC68340 (16 MHz)	
SCSI Interface	NCR53C94 SCSI Controller	
Memory	128 KBytes EPROM	
	2-16 MBytes DRAM	
	7K Bytes Static RAM	
Power Requirements	**Typical**	
	+5 volts	**1.1 amps typical**
Operating Temperature	5 to 50 degrees C	
Relative Humidity	8-80% non-condensing	
Physical Dimensions	Height -	396mm (15.6 in)
	Depth -	305mm (12.1 in)
	Width -	20mm (0.79 in)
Voice Playback/Record Channels	8 playback/4 record port	
	64 playback/32 record port	
	128 playback/32 record	
Maximum Prompt Time	35 minutes	
Voice Encoding Method	64 Kbit Pulse Code Modulation (PCM)	

3.0 CIRCUIT DESCRIPTION

Voice data is stored in DRAM. Upon initialization, announcement data is uploaded and downloaded from the system controller hard disk to the IPRC via a SCSI bus. IPRC ports are allocated and released during a call as specified by the call processing application. The IPRC supports up to 16 prompt libraries, with up to 256 prompts per library and a total duration of 35 minutes. The IPRC plays prompts on up to 128 channels.

Each IPRC port can send prompt messages to any PCM time slot. For a typical call scenario, the application software assigns an IPRC channel to a voice path and then sends available voice prompts. When the IPRC channel is no longer needed, the port is removed from the voice path and the call is allowed to continue. Refer to Figure 1 for a functional block diagram.

> *NOTE: IPRCs are optional in systems, depending on whether the application call scenario requires voice prompting that is not provided by other peripheral equipment.*

IPRCs mount in any port card slot and include a microprocessor, speech processing circuitry and requisite firmware.

3.1 DRAM PROMPT STORAGE

Prompt data software consists of a series of phrases and scripts which have been converted to digital data. The software is stored on hard disk in the storage subsystem. Prompts are downloaded from the hard disk to an IPRC via the SCSI interface during card initialization.

Prompt data is stored in a 16 Mbyte DRAM controlled by the Packet Processor. The DRAM itself are 1 Mbit x 4 devices. Thirty five minutes of prompt storage require 32 devices. The IPRC application code and data are also stored in DRAM. The application software controls the output of the prompt data onto the appropriate PCM time slot via a message packet sent over the Communication Bus.

3.2 PCM TIME SLOT BUS INTERFACE

The IPRC PCM Bus Interface consists of dual port RAM to buffer, transmit, and receive PCM data, discrete logic (to control PCM bus access), and one of the internal 68340 timer modules.

The IPRC supports up to 128 channels for prompt playback using two dual port RAM buffers (U22 and U23). Each playback channel requires 32 bytes for PCM buffering, yielding 4Kbytes total dual port RAM for PCM transmission.

The IPRC supports up to 32 channels for prompt recording using additional dual port RAM buffers.

Each IPRC port interfaces to the PCM bus structure with bus interface circuitry which is common to system port cards. When an IPRC is plugged into the midplane it is automatically assigned a set of a maximum of 128 consecutive port addresses, depending on the IPRC's port configuration. The PCM interfaces control access to the correct PCM time slot on which to send the prompt data.

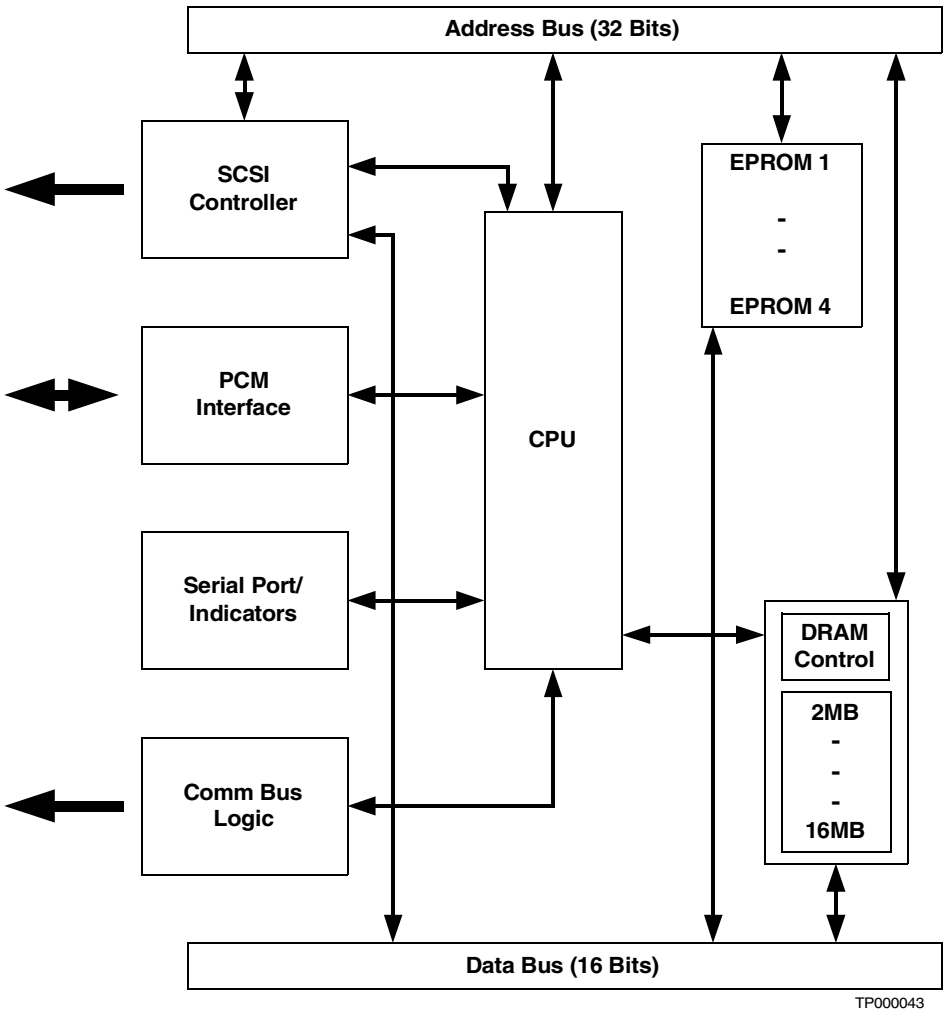


Figure 1: IPRC Functional Block Diagram

3.3 PACKET PROCESSOR

The IPRC contains a 68340-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards with the exception of the Network Bus Controller (NBC).

The Packet Processor consists of the 68340 microcomputer, program and data memory, associated RAM, EPROM, and address decode circuitry, the Communication Bus Interface, an asynchronous serial port, and the LED register. It is via the Communication Bus that the NBC issues commands to the IPRC in the form of data packets. The IPRC reports the status of its voice channels over the same bus using the data packet protocol. When polled by the NBC, the Packet Processor reports any status change. The 68340 provides the intelligence for the Packet Processor and, therefore, for the IPRC.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane and also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

3.4 IPRC STATUS LEDS

The IPRC has three LEDs that are visible through the front panel and two additional internal LEDs that are not visible from the front panel.

3.4.1 FRONT PANEL LEDS

A red, a yellow, and a green LED (DS1, DS2, and DS3, respectively) are visible through the IPRC's front panel to indicate the status of the card. Typically, an illuminated red LED indicates a major card failure, a yellow LED indicates a minor card failure, and a green LED indicates the card is in standby or diagnostic mode. Table 1 shows the card status information provided by the illuminated LEDs.

3.4.2 INTERNAL LEDS

The red LED inside the front panel (DS5) is tied to the HALT line on the 68340 CPU. DS5 is illuminated when the CPU stops processing.

The green LED inside the front panel (DS4) is the heartbeat indicator for the IPRC. During normal operation, DS4 flashes. Whenever the normal background operation is interrupted (for example during memory testing), DS4 stops flashing at its last known illumination state.

Table 1: Front Panel LEDs

Card Status	Green (DS3)	Yellow (DS2)	Red (DS1)
Card Plugged In (not initialized)	On	On	On
Self Test	On	Blinking	Off
Receiving Download	Blinking	Off	Off
Card Out Of Service (OOS)	On	Off	Off
Standby/Diagnostic Mode	On	On	Off
Major Alarm	Off	Off	On
Minor Alarm	Off	On	Off
Card Failure	On	Off	On

3.5 SCSI INTERFACE

The IPRC uses a SCSI interface to download prompt data to and from the system controller. The SCSI interface is maintained by an NCR 53C94 SCSI Controller, or equivalent, located at U3.

A 16-bit DMA interface is set up between the 68340 and the 53C94 to transfer data between the IPRC DRAM and the SCSI bus. This DMA interface physically exists on the data bus, but program control prevents other devices from using the data bus during DMA operations. The 68340 provides the DMA channel control through the on-chip DMA Module.

3.5.1 IPRC SCSI CABLES

The IPRC cards connect to the system controller cards (side A and B) with ribbon cables on the rear of the midplane. One ribbon cable connects from the A-side connector on the small daughter board located on the lower, right side of the midplane as viewed from the rear. Another ribbon cable connects from the B-side connector. These connectors are clearly marked on the daughter board.

The other end of each ribbon cable has connectors for up to four IPRC cards. These are connected to the lower set of pins (J3) on the rear of the midplane for each IPRC installed. Pin 1 on the connector is identified by the red stripe on the ribbon cable. The connectors are installed with Pin 1 facing up.

NOTE: Ensure that each cable connection on the rear of the midplane is aligned with a slot containing an IPRC card.

4.0 EXTERNAL INTERFACES

This section describes the connectors and jacks on the IPRC.

NOTE: J2 Pin Assignments are proprietary and are therefore not documented for customer use.

4.1 J1 PIN ASSIGNMENTS

Table 2 lists the pin assignments for J1 on the IPRC.

Table 2: IPRC J1 Pin Assignments

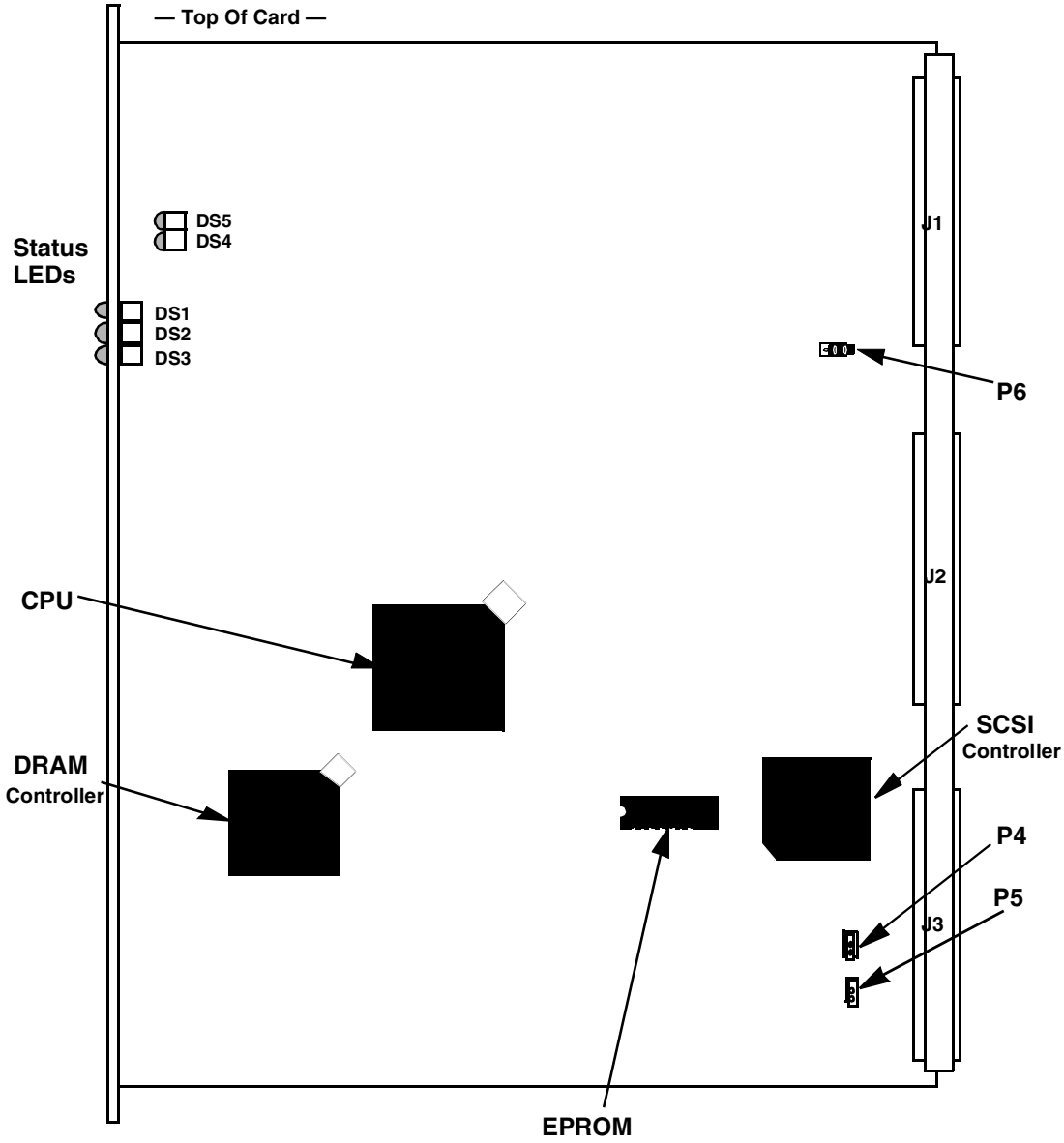
Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5 through 10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14 through 21	Unused	Unused	Unused
22	Card Address Bit 1	Unused	Card Address Bit 0
23	Card Address Bit 3	Unused	Card Address Bit 2
24	Card Address Bit 5	Unused	Card Address Bit 4
25	Card Address Bit 7	Unused	Card Address Bit 6
26	SRV	Unused	Unused
27	DID	Unused	Unused
28	RST	Unused	Unused
29 through 31	Unused	Unused	Unused
32	DGND	Unused	DGND

4.2 J3 PIN ASSIGNMENTS

The IPRC uses the first 25 pins on J3 rows A and C for SCSI bus signals. The following table specifies the pin connections.

Table 3: J3 Pin Assignments

Pin	Row A	Row B	Row C
1	SD0	Unused	DGND
2	SD1	Unused	DGND
3	SD2	Unused	DGND
4	SD3	Unused	DGND
5	SD4	Unused	DGND
6	SD5	Unused	DGND
7	SD6	Unused	DGND
8	SD7	Unused	DGND
9	SDP	Unused	DGND
10 through 12	DGND	Unused	DGND
13	TPWR	Unused	DGND
14	DGND	Unused	DGND
15	DGND	Unused	DGND
16	ATN	Unused	DGND
17	DGND	Unused	DGND
18	BSY	Unused	DGND
19	ACK	Unused	DGND
20	SRST	Unused	DGND
21	MSG	Unused	DGND
22	SEL	Unused	DGND
23	CD	Unused	DGND
24	REQ	Unused	DGND
25	1O	Unused	DGND
26 through 32	Unused	Unused	Unused



Note: Not all components / devices are shown.

Figure 2: IPRC Jumper and EPROM Locations

4.3 FRONT PANEL JACK (P2)

The IPRC has a front panel jack used to access internal diagnostics and internal debugger utilities, and to obtain run-time status/error messages. The front panel jack is an asynchronous serial port that is configured at 9600 baud, 8 bits, no parity. The front panel jack accepts the standard phone jack used on all system port cards.

5.0 CONFIGURATION NOTES

The IPRC is manufactured by Cisco Systems, Inc. Jumper plugs are factory set for use in systems. Figures 3 and 4 show the location of the factory set jumpers. Refer to the jumper settings to verify configuration jumper settings prior to installing the IPRC in a Port Subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

If a card is improperly configured, it may fail to operate. Therefore, be certain to verify configuration settings before installing a replacement service circuit card in the system.

5.1 EPROM SELECT JUMPERS

The IPRC is provided with an EPROM in socket U2. The default jumper configuration of P4 and P5 for 1 Mbit (128k x 8), is shown in Figure 3.

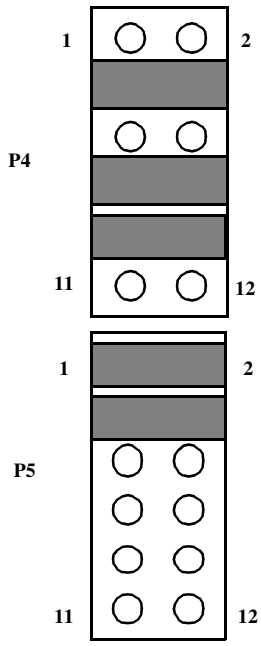


Figure 3: P4 and P5 Jumper Placement

5.2 RESET JUMPER

Jumper J6 is used to disconnect the Reset signal from the system backplane to the IPRC. Removal of this jumper prevents the NBC from resetting the IPRC. Remove this jumper only when using the background mode debugger on the IPRC on a system environment. During background mode debug operations, normal program execution on the 68340 is interrupted. Failure to remove this jumper during debugging results in the IPRC being reset as soon as the 68340 is placed in debug mode.

Figure 4 shows the jumper configuration for normal and background mode operation. The Normal Operation setting is the default.

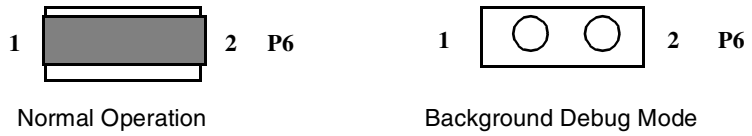


Figure 4: P6 Jumper Placement

5.3 SOFTWARE CONFIGURABLE PORT LIMITATION

When an IPRC is added to the system, it is defined with the physical number of ports. The 64 and 128 port IPRC configurations may also be configured to support less than the physical port capacity. This feature enables the user to configure the port density in 8-port increments through the IPRC Card Configuration screen. (Refer to the *VCO/4K System Administrator's Guide* for more information.) The screen processing frees up or re-allocates timeslots based on the defined port density.

6.0 RELATED DOCUMENTS

- *Integrated Prompt/Record Card User Supplement*
- *VFEdit User's Guide*
- *VCO/4K Standard or Extended Programming Reference*

MF Receiver Card (MRC)

1.0 GENERAL

The MF Receiver Card (MRC) card is a standard system service circuit card that resides in the master or any expansion port subrack. It includes eight multifrequency (MF) receiver circuits that are available for assignment to calls as needed. MRC ports are allocated and released during a call as specified by the call-processing application.

The number and type of receiver cards required by a system is based on anticipated traffic and the call scenario. MRCs are microprocessor-based, firmware controlled, and incorporate the standard system internal control and digital network interface.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM; 2K Bytes RAM
Power Requirements:	+5 Volts – 500 mA (typical) +15 Volts – 275 mA (typical) -15 Volts – 290 mA (typical)
Detectable input level:	-30 dBm minimum; 0 dBm maximum
Acceptable twist:	8 dB maximum
Tone or quiet duration	40 mS minimum
Detected Digits	
MF Digit 1	700 Hz + 900 Hz
MF Digit 2	700 Hz + 1100 Hz (Coin Collect)
MF Digit 3	900 Hz + 1100 Hz
MF Digit 4	700 Hz + 1300 Hz
MF Digit 5	900 Hz + 1300 Hz
MF Digit 6	1100 Hz + 1300 Hz
MF Digit 7	700 Hz + 1500 Hz
MF Digit 8	900 Hz + 1500 Hz (Operator Released)
MF Digit 9	1100 Hz + 1500 Hz
MF Digit 0	1300 Hz + 1500 Hz (Operator Attached)
MF Digit KP	1100 Hz + 1700 Hz (Coin Return, CCITT KP1)
MF Digit ST	1500 Hz + 1700 Hz (Coin Collect, Operator Released)
MF Digit STP	700 Hz + 1700 Hz (Ringback, CCITT Code 11, TSPS STP)
MF Digit STP2	900 Hz + 1700 Hz (CCITT Code 12, TSPS ST2P)
MF Digit STP3	1300 Hz + 1700 Hz (CCITT KP2, TSPS ST3P)

3.0 CIRCUIT DESCRIPTION

The MRC provides systems with eight MF digit receivers. These receivers are typically used when MF digit signalling must be decoded on incoming trunks. Each MRC port can independently listen to any time slot on either PCM data bus. For a typical call setup, an MF receiver port is assigned by software to listen to the output of a trunk and report any digits that are received. When the MF Receiver is no longer needed, the port is assigned to listen to quiet.

Figure 1 shows a simplified block diagram of the MRC.

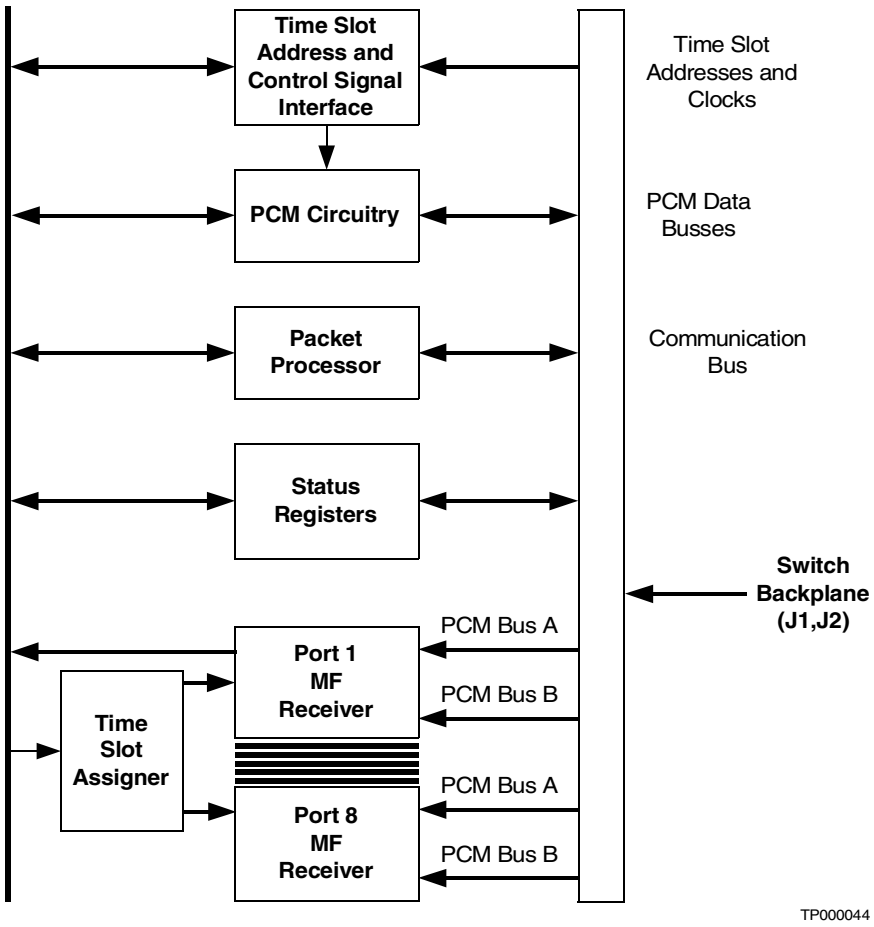


Figure 1: Block Diagram Of MRC

3.1 MF DIGIT RECEIVER

An MF digit receiver hybrid circuit is provided for each MRC port. The receiver is connected to the coder/decoder's (codec's) analog output signal and can identify MF digits 0 through 9, KP, ST, STP, STP2, and STP3 (refer to *Section 2.0*). The output of each MF receiver hybrid can be read by the packet processor.

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within the system is encoded and transmitted as Pulse Code Modulated (PCM) data. Each MF receiver port contains a codec to translate PCM data into an analog signal. This signal is monitored by a MF receiver hybrid circuit. The MRC interfaces to the PCM time slot bus structure with bus interface circuitry which is common to system port cards.

When an MRC is plugged into a port subrack backplane, it is automatically assigned a set of eight consecutive port addresses. The PCM data and time slot bus interfaces control the capture of the correct PCM data for reception by each MF receiver port.

The two PCM busses are functionally equivalent. Use the transmit time slot and PCM data bus for a particular port to select which time slot and bus a given port will listen to.

3.3 PACKET PROCESSOR

The MRC contains an 8031-based packet processor that interfaces to the communication bus. A packet processor is part of all cards in the master or expansion port subracks with the exception of the Network Bus Controller (NBC).

The packet processor consists of the 8031 microcomputer, program and data memory, the communication bus interface, an asynchronous serial port, and the LED register. It is via the communication bus that the NBC issues commands to the MRC in the form of data packets. The MRC reports the status of its MF digit receivers over the same bus and using the data packet protocol. When polled by the NBC, the packet processor reports any status change.

The packet processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The packet processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The packet processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry, the communication bus interface, an asynchronous serial port, and the LED register. The 8031 provides the intelligence for the packet processor and, therefore, for the MRC.

3.4 CONTROL STATUS REGISTERS

The MRC contains a number of control and status registers to interface the 8031 to the functions of the eight ports on the card. Eight address locations, 0000 to 0007, are read by the 8031 to determine the status of a port's MF receiver.

3.5 MRC STATUS LEDS

A red, a yellow, and a green LED are visible through the MRC's front panel to indicate the status of the card. Each LED is turned on when the software generic sets a bit low in an external memory register. Typically, an illuminated red LED indicates a major card failure, an illuminated yellow LED indicates a minor card failure, and an illuminated green LED indicates the card is in standby or diagnostic mode (refer to *Section 6.01*).

3.6 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the MRC.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

Table 1: MRC J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2

Table 1: MRC J1 Pin Assignments(Continued)

Pin	Row A	Row B	Row C
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

4.0 CONFIGURATION NOTES

The MRC is manufactured by Cisco Systems, Inc. Jumper plugs on the MRC are factory set for use in systems. Figure 3 indicates the location and correct installation of jumper plugs on an MRC based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it in a port subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

If a card is improperly configured, it may fail to operate. Therefore, make sure you verify configuration settings before installing a replacement service circuit card in the system.

Jumper Locations

NOTE 1

- Install jumper plug at J5 in the "U" position for codec µ-law operation (North American standard).
- Install jumper plug at J5 in the "A" position for codec A-law operation (European standard).
  Position "U" (µ-law) is the factory default setting for J5.
- Install the jumper plug at J6 in the "1544" position for 1.544 MHz codec clock (North American standard).
- Install the jumper plug at J6 in the "2048" position for 2.048 MHz codec clock (European standard).
  Position "1544" (1.544 MHz) is the factory default setting for J6.

PROM

The 2764 PROM in location U2 contains firmware appropriate to MRC polling and call processing requirements.

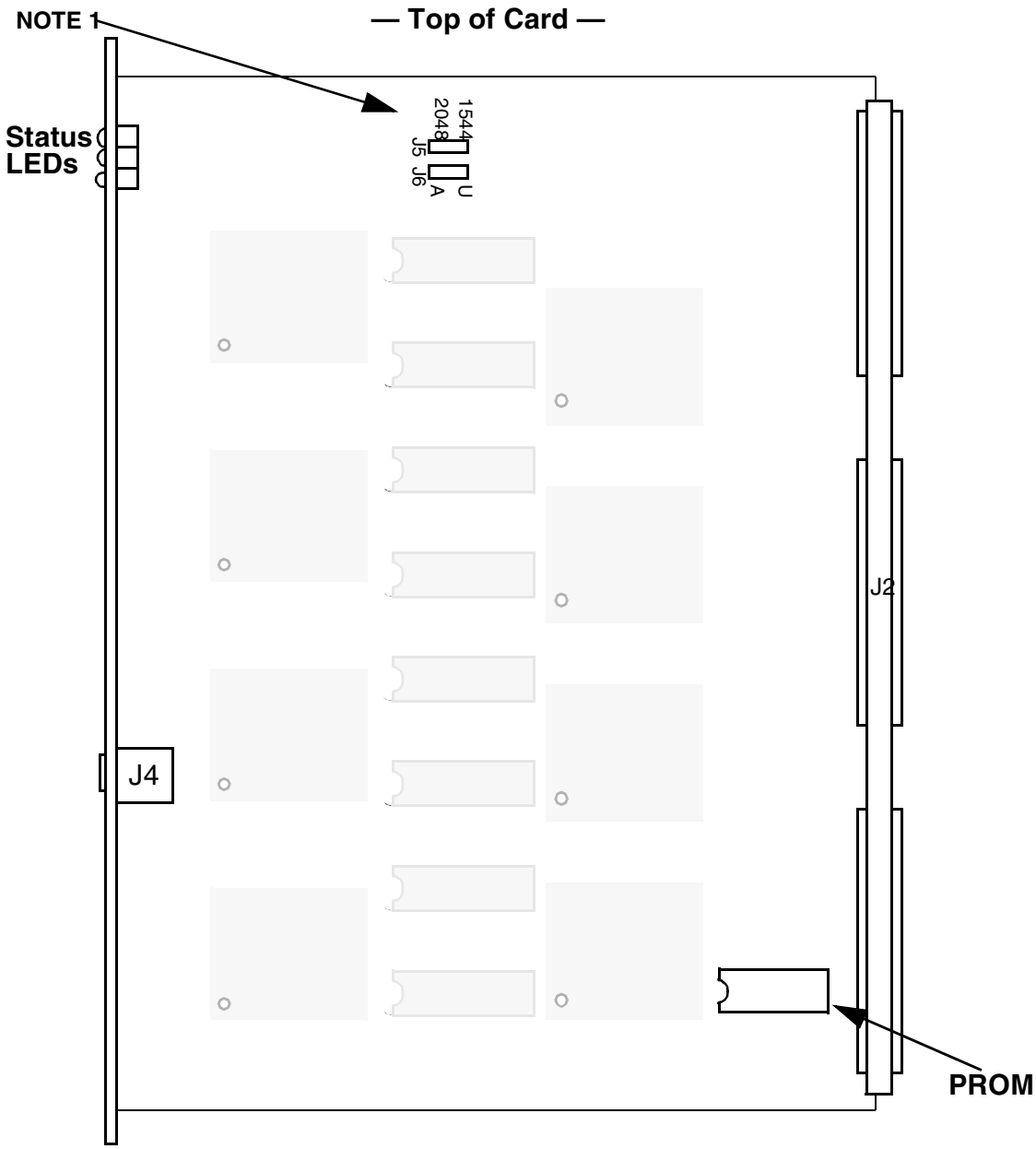


Figure 2: MRC Jumper & PROM Locations
Rev. A or B

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the MRC, refer to the following publications:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference
- VCO/4K Hardware Planning Guide
- VCO/4K System Maintenance Manual

DTMF Receiver Cards (DRC-24 and DRC-48)

1.0 GENERAL

The 24 and 48 port DTMF Receiver Cards (DRC-24 and DRC-48) are standard service circuit cards that may reside in the Master, or any Expansion Port, subrack.

When downloaded with signal processing software, the DRC-24 (or DRC-48) performs DTMF tone detection. The DRC-24/-48 is available as a resource for all trunk types.

The DRC-24 is equipped with one high-speed Digital Signal Processors (DSP); The DRC-48 is equipped with two. The DTMF Receiver Card signal processing software is automatically downloaded from the system's hard disk to the DRC-24/-48 card via the system communication bus upon boot-up.

This document describes the general hardware configuration of the DRC-24/-48. For additional information on the DRC-24/-48 implementation, refer to the *Generic Release Notes*.

2.0 SPECIFICATIONS

Digital Signal Processor		
Microprocessor	24 Port: One AT&T 32C (50MHz)	
	48 Port: Two AT&T 32C (50MHz)	
Packet Processor		
Microprocessor	(1) 8031 CPU (12MHz)	
Memory	2K Bytes RAM 8K Bytes EPROM	
Power Requirements		**Typical**
	+5 Volts:	24 Port: 800 mA
		48 Port: 1.5 A
Channels Per Card	24 or 48	
Tones Detected, DTMF Receiver		
Detectable Input Level	-29 dBm minimum, 2 dBm maximum	
Acceptable Twist	10 dB maximum	
Tone or Quiet Duration	40 ms minimum	

The DRC-24/-48 detects tones compliant with the specifications defined in the following Bellcore documents:

- BOC Notes on the LEC Networks-1990, Issue 1, March 1991
- SR-TSV-002275, Sections 6.13.1 - 6.13.3

Contact Cisco Systems, Inc. for additional information.

3.0 CIRCUIT DESCRIPTION

The DRC-24 and DRC-48 cards are high performance signal processing platforms with direct access to PCM busses. Two types of processors are employed on the DRC-24/-48.

- *Digital Signal Processor (DSP)* interfaces directly with the dual PCM busses and processes the PCM samples.
- *Packet Processor* manages the interface between the DRC-24/-48 and the Network Bus Controller (NBC). Its functions include the management of command and message packets passed between the DRC-24/-48 and NBC, and high level control over the DSP.

Figure 1 shows a simplified block diagram of the DRC-24/-48.

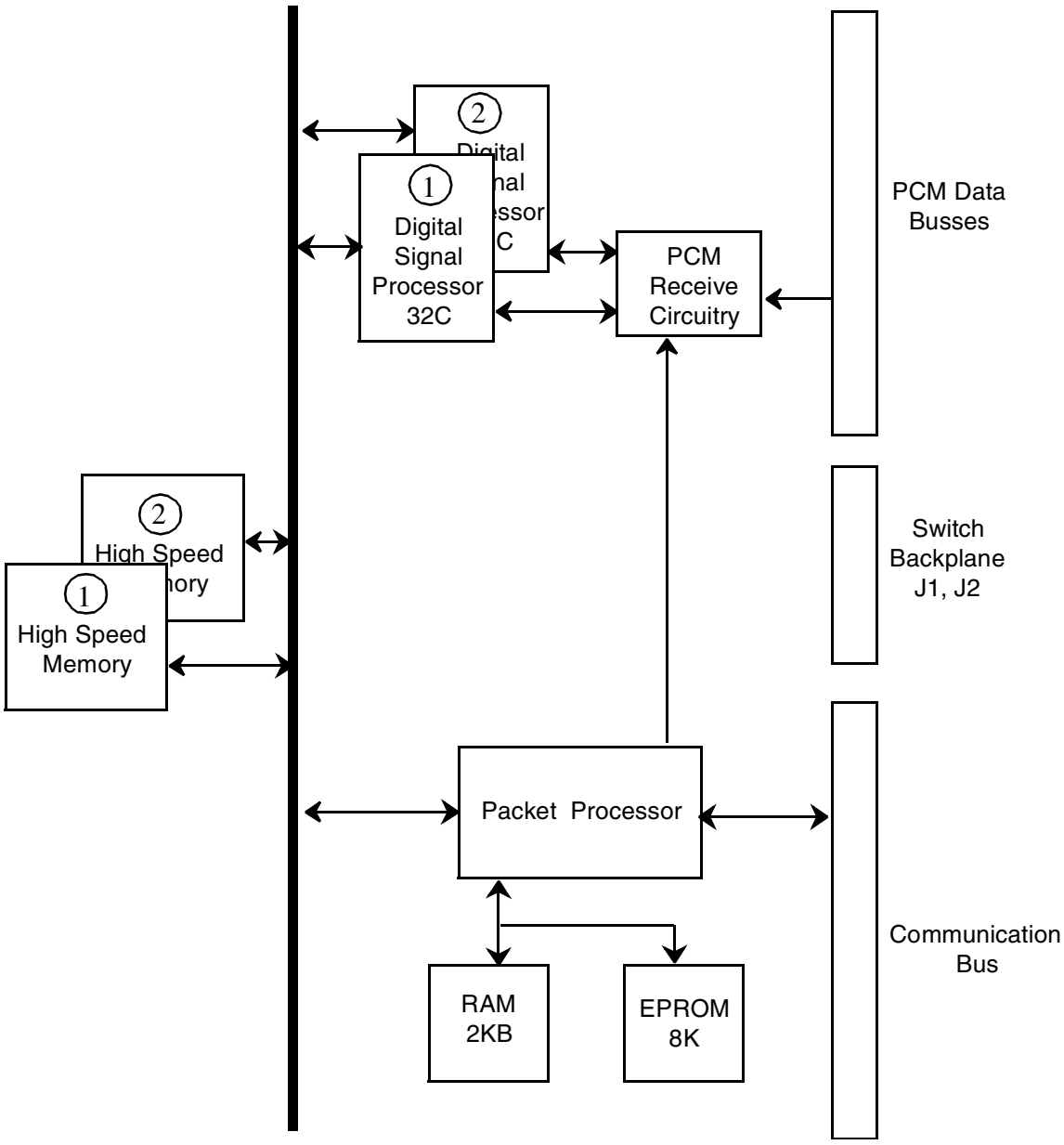


Figure 1: Block Diagram of DRC-24 and DRC-48

3.1 DIGITAL SIGNAL PROCESSOR

The DRC-24/-48 utilizes an AT&T 32C DSP running at 50MHz. The 32C incorporates the following features:

- 80ns cycle times
- 32-bit floating point arithmetic
- Single precision floating point IEEE compatibility
- 16 Mbps serial interface
- 32-bit external data bus

High speed, 128KB, 25ns SRAM memory is associated with the DSP.

3.2 PACKET PROCESSOR

The DRC-24/-48 contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC).

The Packet Processor consists of the 8031 microcomputer, program and data memory, the Communication Bus Interface, an asynchronous serial port, and the LED register. The NBC issues commands and downloads signal processing software to the DRC via the COMM Bus in the form of data packets.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The Packet Processor also controls the three status LEDs (red, yellow, and green), which are visible through the card's front panel.

3.3 COMMUNICATION BUS INTERFACE

The Communication Bus Interface on the Packet Processor interfaces to the Communication (COMM) Bus. There are two types of data transfer cycles over the COMM Bus – Individual Card Cycles and Broadcast Cycles. Individual Card Cycles are used when the NBC desires two-way communication with a single card. Broadcast Cycles are used when the NBC needs to send data (broadcast) to all cards or all cards of a particular type.

3.4 PCM RECEIVE CIRCUITRY

All PCM data are directly addressable by the DSP. The DRC-24/-48 uses Dual Port RAM (DPR) to interface with the PCM buses. Each of the DPRs holds two frames of PCM data. The frames switch on the system frame signal which occurs during the first time slot.

The DSP gets the PCM data for each of its 24 channels during a single 125 µs frame. The DSP is interrupted every 125µs by the system frame signal and enters a PCM acquisition subroutine. Each DSP has up to 24 ports for addressing PCM data. Under software command, the DSP reads the PCM data through an assigned port and stores it in memory.

The port address is converted into an actual time slot address. This time slot address directly addresses the stored PCM and enables the data onto the DSP data bus. Because the DSP setup RAM is shared by three resources – the DSP, the serial path setup circuitry, and the Packet Processor – access to the RAM is made on a request and grant basis.

The path setup RAM provides the gateway for access to the PCM data. Access is granted if none of the other resources are using or requesting it. Path setups originate from the Packet Processor.

A DIP switch on the DRC-24/48 card can be set to allow the card to process either µ-Law (US) or A-Law (Europe) PCM encoding.

3.5 DRC-24 AND DRC-48 STATUS LEDS

Red, yellow, and green LEDs are visible through the DRC-24/-48's front panel to indicate the status of the card.

> ***NOTE:*** *The DRC-48 uses the same front panels as the DRC-24 except for the "DRC 48" labels.*

Each LED is turned on when the software generic sets a bit low in an external memory register. Typically, an illuminated red LED indicates a major card failure, an illuminated yellow LED indicates a minor card failure, an illuminated green LED indicates the card is in the wrong slot, illuminated green and yellow LEDs indicate the card is out of service, and all LEDs off indicate the card is in active, standby, or diagnostic mode (refer to *Section 6.0*).

Table 1: Front Panel LEDs

Card Status	Green (DS3)	Yellow (DS2)	Red (DS1)
Card Plugged In (not initialized)	On	On	On
Self Test	On	Blinking	Off
Receiving Download	Blinking	Off	Off
Card Out Of Service (OOS)	On	On	Off
Active, Standby/Diagnostic Mode	Off	Off	Off
Major Alarm	Off	Off	On
Minor Alarm	Off	On	Off
Card Failure	On	Off	On
Card in Wrong Slot	On	On	Off

3.6 BACKPLANE CONNECTOR PIN ASSIGNMENTS

The DRC-24 and DRC-48 do not require connection to external devices. Pin assignments for backplane connectors J1 through J3 on the DRC-24/-48 are proprietary and are therefore not documented for customer use.

4.0 CONFIGURATION NOTES

The DRC-24 and DRC-48 are manufactured by Cisco Systems, Inc. Jumper plugs on the DRC-24/-48 are factory set for use in systems. Figure 3 indicates the location and correct installation of jumper plugs on a DRC-24/-48, based on the card's PCB revision level. Use this information to verify or reset jumpers on the DRC-24/-48 prior to installing it in a Port Subrack.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

If a card is improperly configured, it may fail to operate. Therefore, great care must be taken to verify configuration settings before installing a replacement service circuit card in the system.

> **CAUTION: A limitation in the DRC 24/48 exists which may cause several of the ports on a single card to be seized for DTMF collection simultaneously. This results in some ports losing digits.**
>
> **To alleviate this potential problem, alternate ports from different DRC 24/48 cards in the resource group. This causes consecutive collections to occur on separate cards.**

Figure 2 shows the location of the PROMs and jumpers for the DRC-24 and DRC-48 cards.

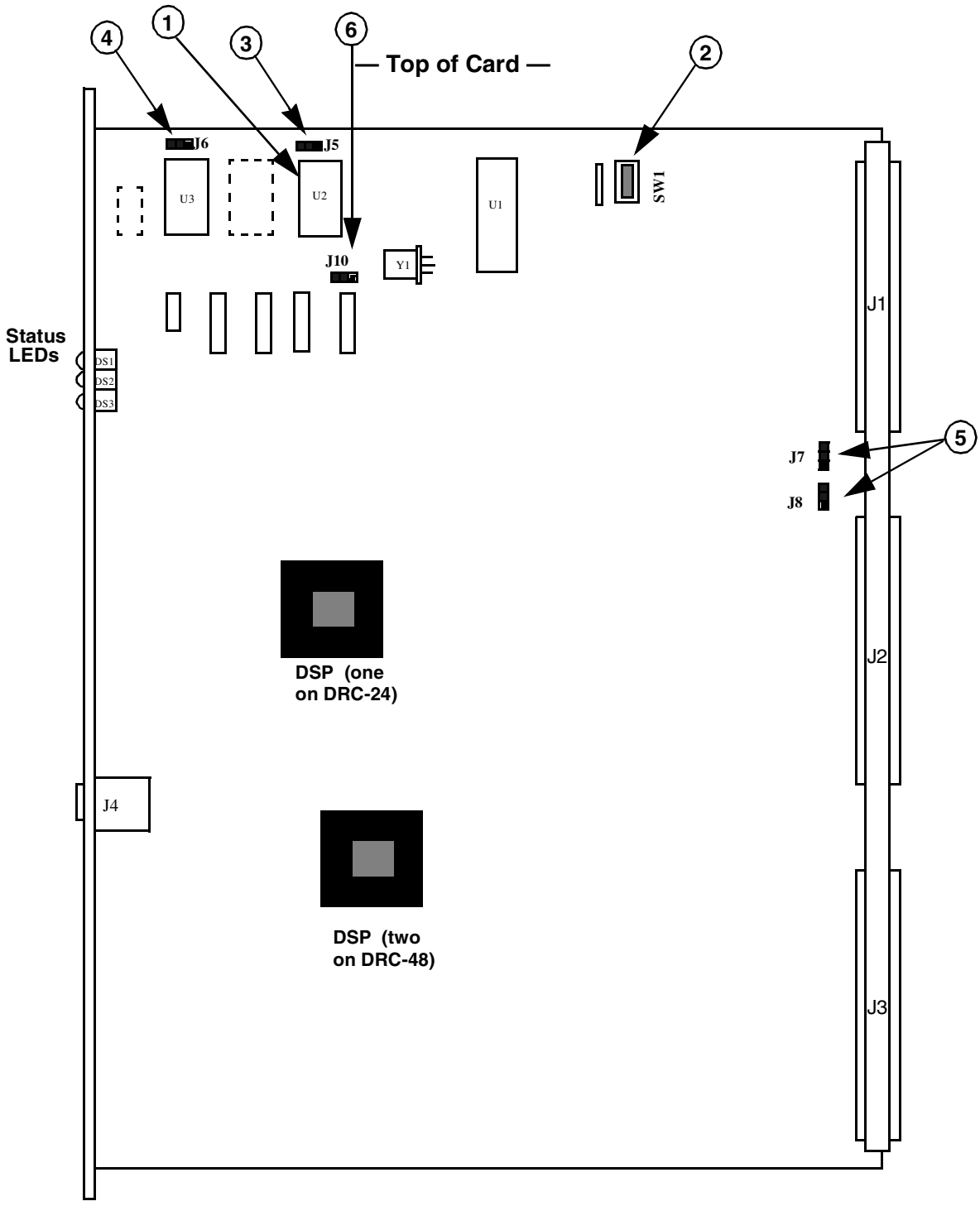


Figure 2: DRC-24 and DRC-48 Jumper and PROM Locations

4.0.1 NOTE 1

The PROM1 (2764 PROM) in location U2 contains firmware appropriate to DRC-24/48 processing requirements.

4.0.2 NOTE 2

The SW1 Dip switch has eight switches; SW1-1 through SW1-8:

- If the system is running Generic V3.2 and earlier, all switches must be set to the closed position.
- If the system is running Generic V3.3 or later, the switches must be set as follows:

  SW1-1 is used to enable either µ-Law (US) or A-Law (Europe) PCM encoding formats:

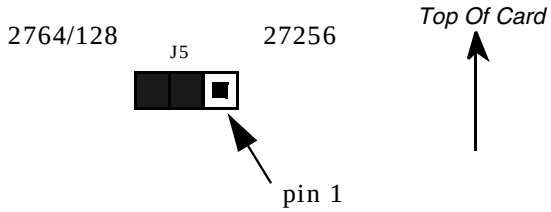
  – For µ-Law, SW1-1 must be closed.

  – For A-Law, SW1-1 must be open.

  The remaining switches, SW1-2 through SW1-8 must be closed.

4.0.3 NOTE 3

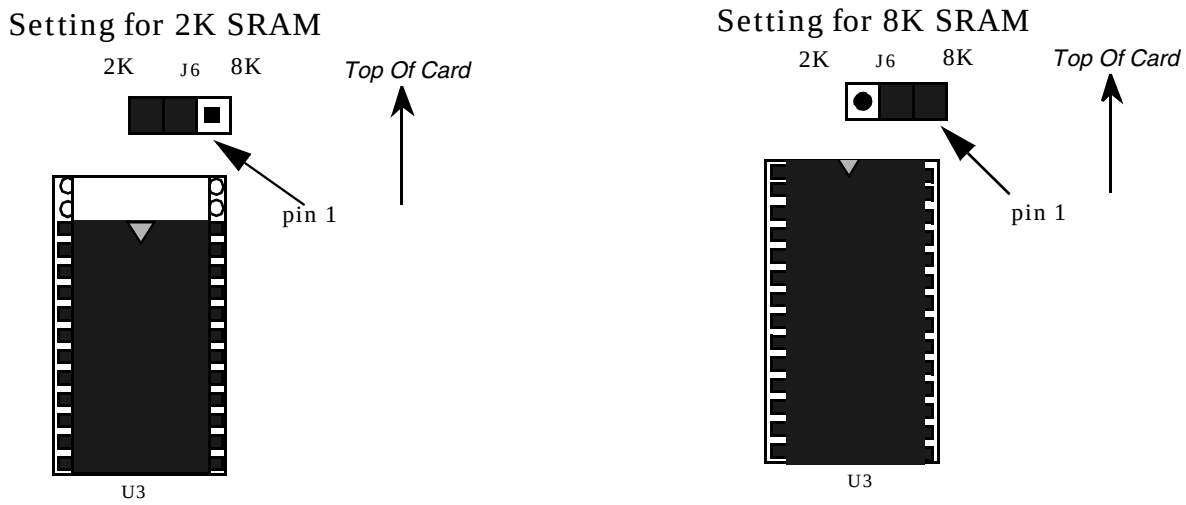
The J5 jumper must be set at pins 2 and 3 as shown in the following illustration:



NOTE: For readability, "2764/128," "J5," and "27256" are rotated 180° from the orientation of the printed text on the card.

4.0.4 NOTE 4

The setting of J6 jumper is dependent on the size of the card's SRAM. The SRAM is installed at location U3 and is either 2K or 8K. The J6 jumper settings are shown in the following illustration:



Set J6 to pins 2 and 3 for 2K SRAM

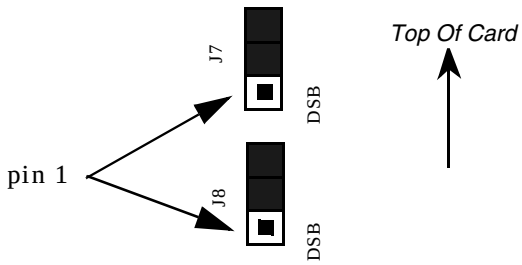
Set J6 to pins 1 and 2 for 8K of SRAM

NOTE: For readability, "2K," "J6," and "8K" are rotated 180° from the orientation of the printed text on the card.

To identify which SRAM device is installed on the card, observe how the SRAM chip sits in the U3 socket. The U3 socket can accommodate a 28 pin device. However, 2K SRAM is a 24 pin device. When 2K SRAM is installed at U3, the top two rows of the socket are left empty as shown in Figure 2. The 8K SRAM is a 28 pin device, therefore, when an 8K SRAM is installed, all rows in the socket are used.

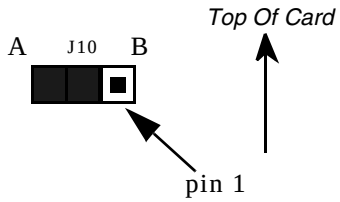
4.0.5 NOTE 5

J7 and J8 jumpers must be set at pins 2 and 3 as shown in the following illustration:



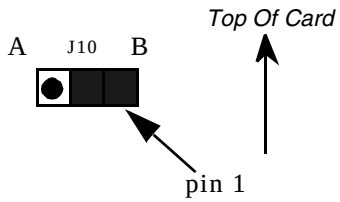
4.0.6 NOTE 6

For DRC-24 cards, J10 jumper must be set at pins 2 and 3 (position A) as shown in the following illustration:



NOTE: For readability, "A," "J10," and "B" are rotated 180° from the orientation of the printed text on the card.

For DRC-48 cards, J10 jumper must be set at pins 1 and 2 (position B) as shown in the following illustration:



NOTE: For readability, "A," "J10," and "B" are rotated 180° from the orientation of the printed text on the card.

5.0 TROUBLESHOOTING

5.1 FAILURE TO DOWNLOAD

Upon system reset, the DTMF Receiver Card signal processing software is broadcast to all DRC-24/-48s in the system. If an individual DRC-24/-48 fails to complete the download, it is taken out of service and a directed download is performed to the failed card after the broadcast download has been completed. Those DRC-24/-48s which complete the download come into service and become available to process DTMF tone detection requests.

A directed download to an individual DRC-24/-48 takes longer to complete. The affected DRC-24/-48 comes into service (if the card had previously been configured to be active) only after the directed download is successfully completed.

5.2 LOSS OF DRC-24 OR DRC-48: EFFECT ON SERVICE

A system can have DRC-24/-48s mounted in any Port Subrack. Depending on the application, loss of the only DRC-24/-48 in a system may block call originations through the switch. If one DRC-24/-48 fails in a system with multiple DRC-24/-48s, grade of service performance will suffer but calls can be processed. Call set-up time may increase as delays in mapping DTMF tone monitor ports occur.

NOTE: All DRC-24/-48s must be put into a single Resource Group.

Service Circuit Test Utility Fails

If the DRC-24/48 card fails the Service Circuit Test utility, verify that the S1 DIP switches are set properly. S1-1 must be closed for µ-Law or open for A-Law. Switches S1-2 through S1-8 must be closed.

6.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the DRC-24/-48, refer to the following publications:

- VCO/4K Product Overview
- VCO/4K Maintenance Manual
- VCO/4K Hardware Planning Guide
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference

Subrate Switching Card (SSC)

1.0 GENERAL DESCRIPTION

The Subrate Switching Card (SSC) is a service circuit card that occupies a single card slot in the VCO/4K platform.

The SSC allows the VCO/4K system to switch voice and data calls at N x 8 Kbit/s rates (where N equals the number of channels). With the SSC, service providers can improve trunk efficiency up to eight times by "packing" eight subrate channels within a traditional 64 Kbit/s channel.

The SSC enables the Cisco Systems switches to be used as Base Station Controllers (BSCs) in wireless telephone networks or other networks that carry compressed audio.

The following further describes the Subrate Switching Card.

- You can remove or replace the Subrate Switching Card without shutting off the system.
- The SSC supports a switching matrix of up to 2,000 64 Kbit/s timeslots, allowing up to 16,000 8 Kbit/s subrate connections.

2.0 SPECIFICATIONS

Microprocessor:	(1) MC68360
Memory:	1M DRAM 128K EPROM
Power Requirements:	30 Watts @ 5VDC max .5 Watts @ 15VDC .5 Watts @ -15VDC

3.0 REDUNDANCY

Redundant SSC operation requires that two SSC cards be present—an active card and a standby card. The standby card is responsible for verifying the operational status of the active card. When the standby card determines that the active card has failed, the standby card:

- Becomes active
- Informs the generic software of the failure
- Waits for the system to control the switchover to active status

Subrate switching requires that both the active and standby SSCs be located in the same rack and on the same level.

The presence of a Subrate Switching Card does not affect system level redundancy.

4.0 CIRCUIT DESCRIPTION

The SSC controls the subrate switching matrix with one Motorola MC68360 QUICC (QUad Integrated Communications Controller).

4.1 CIRCUITRY

The SSC includes the following circuitry:

- Clock drivers—provide clock synchronization for the subrate switching matrix.
- PCM interface—provides a common interface to the backplane for the subrate switching matrix; provides C-Bus access, which enhances the available timeslot count to 4,096 timeslots. The PCM interface is hyperchannel compatible (assuring constant delay through the SSC) for any combination of timeslots, which allows for subchannels.
- High-speed communications bus—provides automatic high-speed communications to the system controller when used in conjunction with the NBC3.

5.0 CONFIGURATION NOTES

5.1 HARDWARE CONFIGURATION

The following list provides hardware configuration information for the Subrate Switching Card.

- There are no configurable jumpers on the SSC.
- The SSC does not require an MDF Adapter.

5.2 SOFTWARE CONFIGURATION

All configuration parameters for the SSC are configured in software through the administration interfaces. There are no hardware options that you can select on the SSC.

The application software, downloaded to the SSC, enables control and configuration of the card, as well as each subrate channel. For more information about configuring subrate service, refer to the Subrate Configuration screen in the *System Administrator's Guide*.

Figure 1 shows the layout of the Subrate Switching Card.

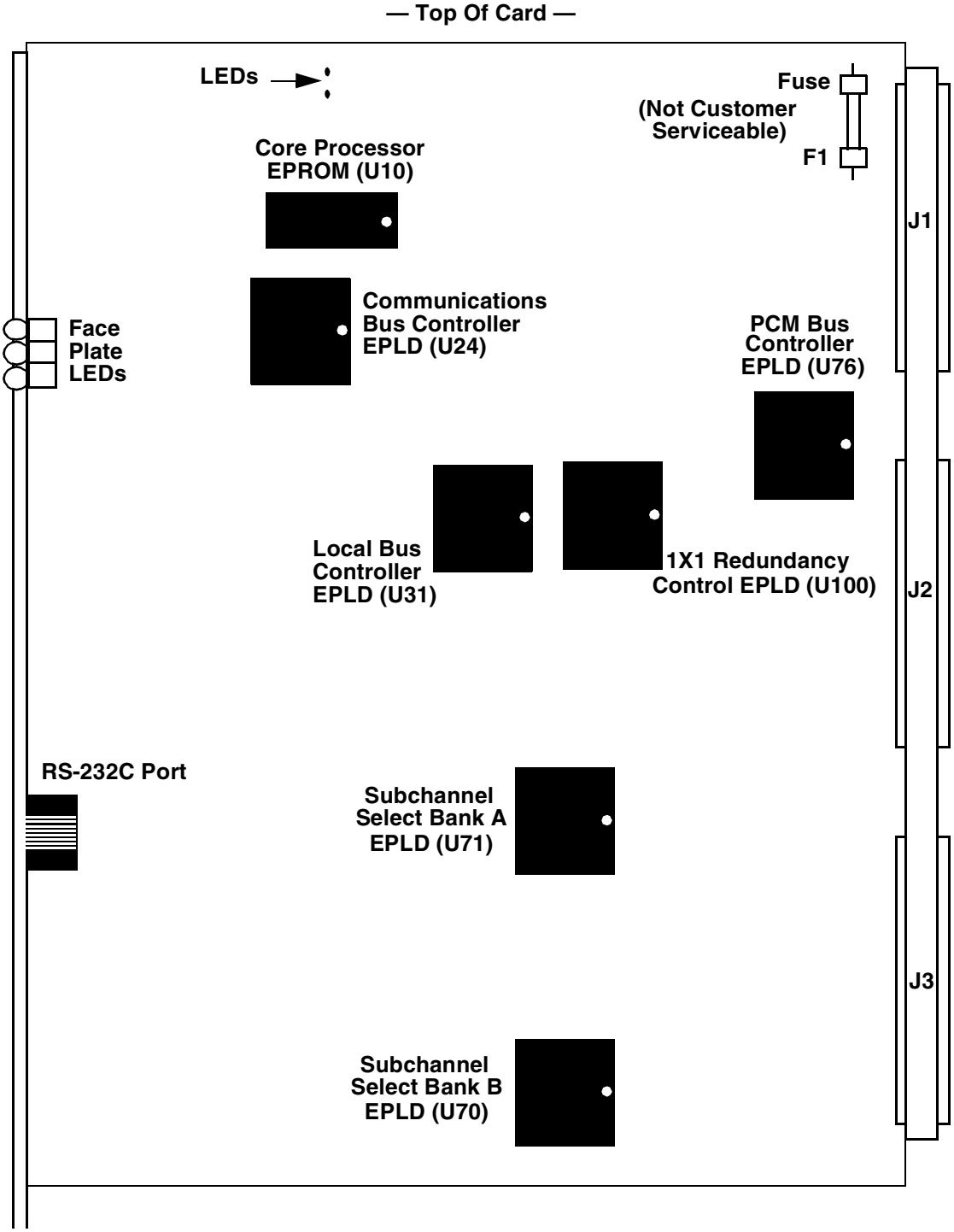


Figure 1: Subrate Switching Card Board Layout

NOTE: All components/devices are NOT shown.

Service Platform Card (SPC)

1.0 GENERAL

The Service Platform Card provides the service resources element of the three critical system elements of the VCO/4K product line — system control, port interfaces, and service resources. The SPC combines the capabilities of existing individual service resource cards in the VCO/4K product line into a single card, which contains all of the functions previously provided by the separate cards.

The hardware design of the SPC allows the software operating within the SPC and the SPC's mezzanine card (the Service Resource Module, or SRM) the ability to exceed the older service resource function's feature set, while providing a much higher level of integration both logically and physically.

The Service Platform Card architecture allows any service resource function of the VCO/4K product family to be performed with this card as a base platform, given a minimum of one SRM mezzanine card on the board to perform the service function(s). Mezzanine cards have the capability to perform more than one service function, and to perform these functions simultaneously.

Some other features of the SPC:

- Improved system reliability and error detection capabilities
- FLASH memory, which allows faster system boot time, and reduces the amount of communications bus traffic
- FPGA architecture, which supports a soft-configured system boot for easier hardware upgrades
- Ability for users to replaced the card with system power on
- Support for up to 2016 concurrently active service circuits per SPC
- Diagnostics support
- Compatiblity with 2K and 4K port systems
- Programmable service facility software support
- Support for up to 32 DSP engines with four SRM cards populated
- Ability for users to independently define each DSP service engine with a service resource function

2.0 SPECIFICATIONS

2.1 COMPLIANCE WITH STANDARDS

The SPC Card is in compliance with all applicable U.S. and international standards. Refer to Table 1.

Table 1: Standards Compliance

Category	Standard
Safety	UL1459 CSA C22.2 EN-60950 IEC-950
EMI/EMC	FCC Part 15 (US/Canada) EN55022 (Europe) EN50082-1 (Europe) VCCI (Japan)
PCB Manufacture	IPC

2.2 SPC CARD SPECIFICATIONS

Microprocessor	MPC860MHZP-50
Memory	8MB FLASH
	16MB DRAM 3.3V DO-DIMM EDO 60nS
Power Requirements	5 Volts – 1.5 A - board only, no SRMs (Max)
(5 V converted to	5 Volts – 1.0 A - each SRM (Max)
3.3 V on the board)	5 Volts – 5.5 A - board with four SRMs (Max)

3.0 SPC CARD ARCHITECTURE

The SPC card is a single-slot Cisco Systems *Type 2* card. Up to four separate SRMs, mounted as mezzanine cards, provide processing resources.

The SPC card is inserted in the VCO/4K switch from the front of the system.

The SPC card contains the following elements:

- Core Processor (HDLC-based multiprocessor architecture and command/response data routing)
- Communications Bus Interface
- Up to four SRMs (DSP-based service engine, mezzanine interface architecture, and serial mezzanine boot control), programmable for application requirements
- Memory subsystem (memory controller, DRAM, and flash memory)
- PCM Interface (bus support)
- Power Subsystem

The block diagram for the SPC card and SRM Modules is shown in Figure 1

The SPC card hardware layout is shown in Figure 2.

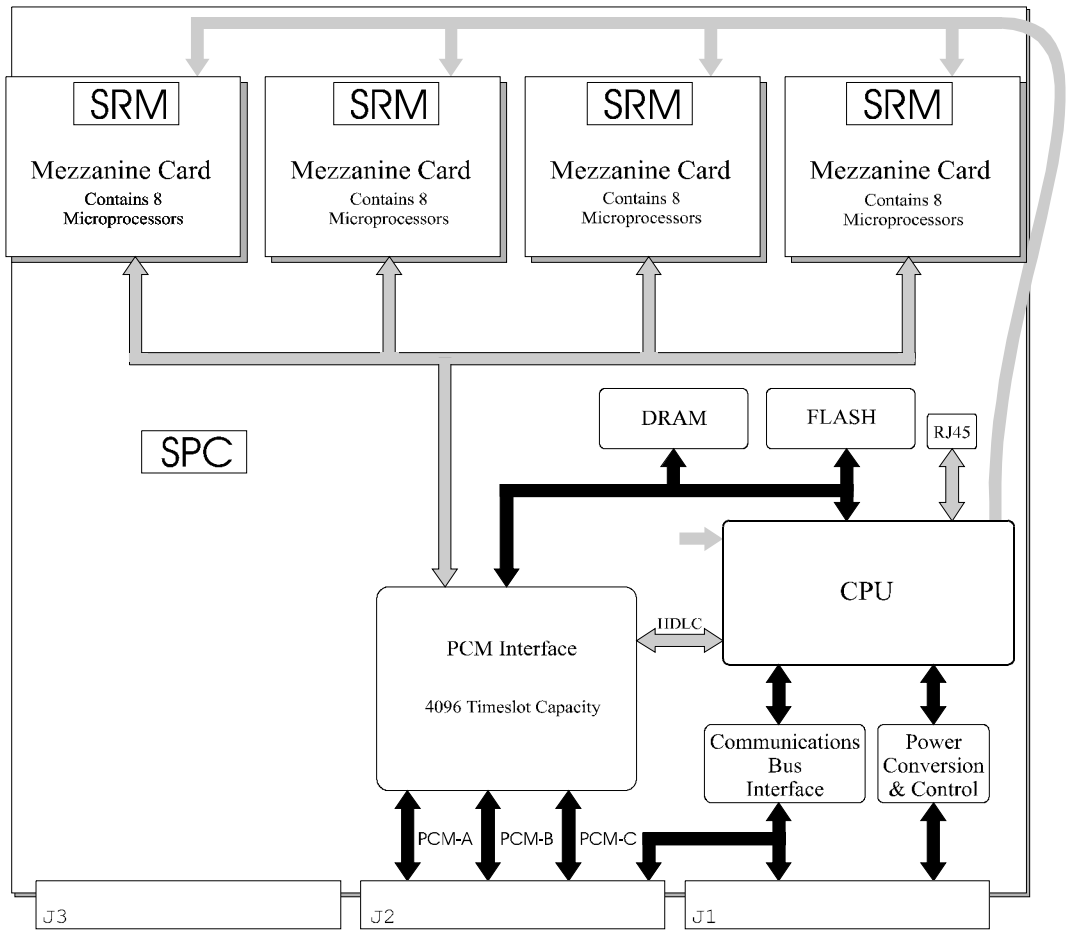


Figure 1: SPC Card and SRM Module Block Diagram

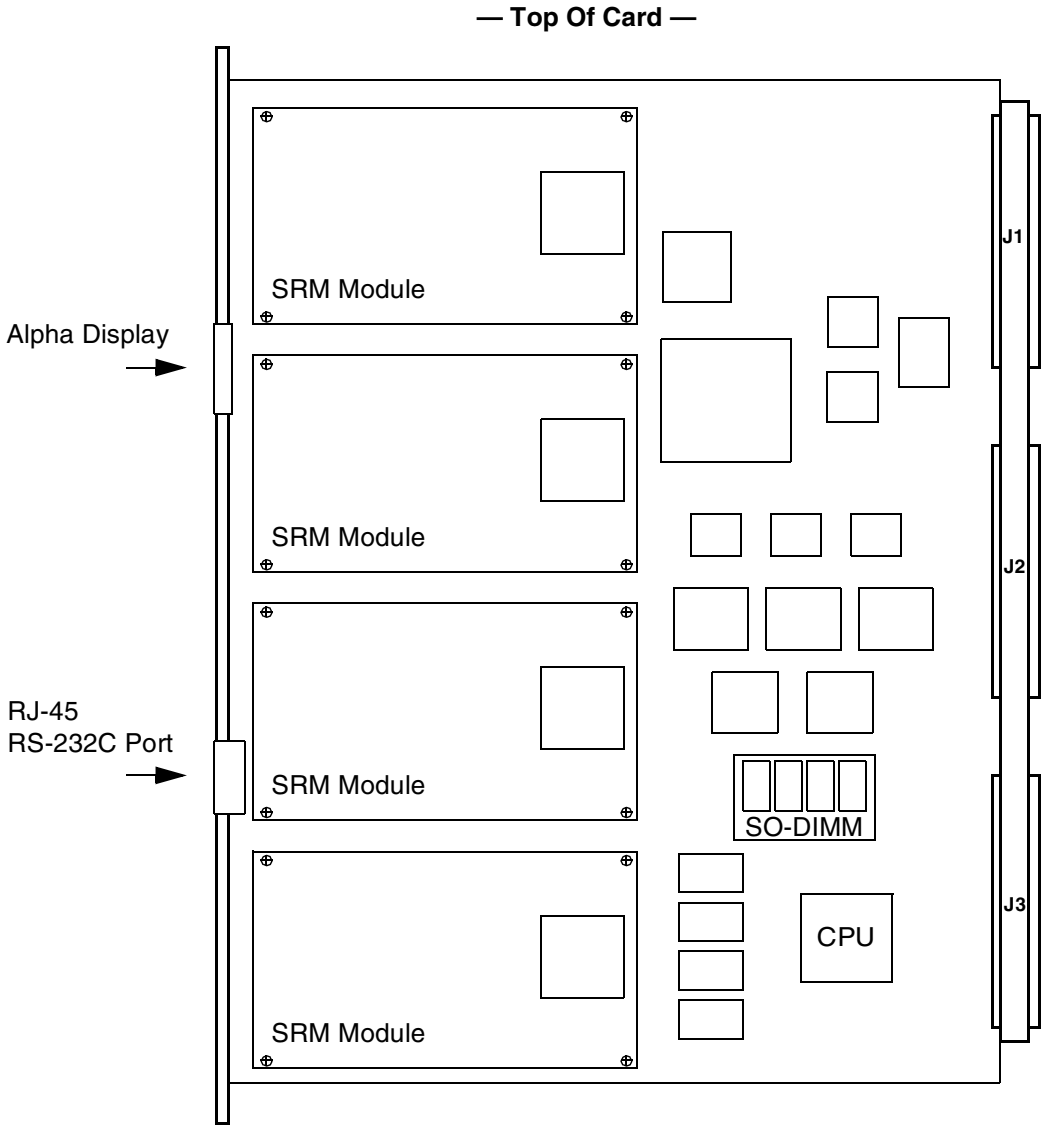


Figure 2: SPC Card Layout (Component Side)

NOTE: Not all components are shown.

4.0 CORE PROCESSOR

The processor and associated peripheral circuitry on the SPC is called the *Core Processor*. The Core Processor runs the card level application and diagnostics and is responsible for managing all SPC-based and mezzanine peripheral devices described in the sections that follow.

Features shown in Figure 1 are discussed in this section at a high level.

4.1 CORE PROCESSOR IMPLEMENTATION

The Core Processor comprises the Motorola MPC860MHZP-50 CPU and associated peripherals and support circuitry. The main timing reference for the Core Processor is supplied by an on-board 3.3V crystal oscillator.

4.2 HDLC-BASED MULTIPROCESSOR ARCHITECTURE

The Service Platform Card's architecture is dependent on a centralized (time division multiplexed and switched) HDLC controller connected to service engines (SEs) in a traditional multiprocessor star arrangement. In the SPC's particular implementation of this architecture, the HDLC controller is contained within the Core Processor. The PCM interface acts as the switching device, which spreads the communication time slots across the service engines. Refer to Figure 3:

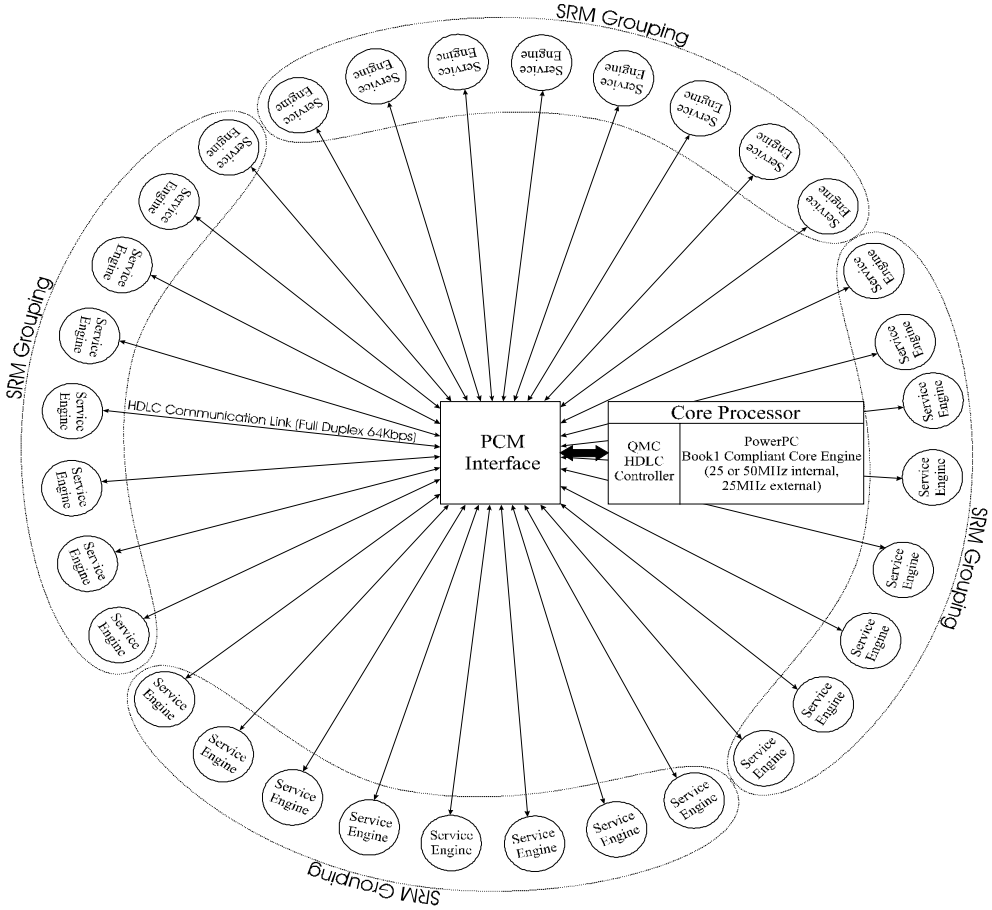


Figure 3: HDLC Command/Control Processor Arrangement

The central processor is responsible for command and response message control of any service engine, or any combination of service engines. The use of HDLC in this star manner has several benefits for the SPC:

- The Core Processor uses an on-board RISC engine, called the CPM (Communication Processor Module). The CPM manages all protocol specific actions.
- The CPM handles data in a multichannel mode. This allows up to 64 (32 used in the SPC architecture) separate DMA channels, each one dedicated to a single HDLC full-duplex pipe to a service engine.
- The physical arrangement and PCM interface facilitates the distribution of the 32-channel HDLC command pipes to the service engines on the Service Resource Modules.

4.3 COMMAND / RESPONSE DATA ROUTING

The Communications Processor Module within the MPC860MHZP-50 is internally routed to the time slot assigner. The transmit and receive data is routed through the TDMA interface to devices external to the MPC860MHZP-50. Once the data leaves the Core Processor, it has a time division multiplexed arrangement. This serial data is then routed to the PCM interface, where it is switched under the control of the Core Processor so the time slots are re-routed to the 32 service engine bound serial streams which contain regular PCM traffic. These 32 serial streams connect the service engines with the PCM interface.

The PCM interface routes 32 serial streams running at 4.096 Mbps each to the mezzanine card locations. Eight of the thirty-two streams are used by each mezzanine location. Each mezzanine card contains eight DSP Service Engines, each receiving one 4.096 Mbps, 64-timeslot, serial, full duplex stream. One 64Kbps timeslot from each stream is dedicated to the HDLC command/response data.

4.4 ALPHA DISPLAY/POWER FAILURE LED

The SPC card displays status on a 5x7 alpha display located on the SPC front panel. Table 2 defines the alpha display states.

NOTE: The SPC card has a card failure LED immediately above the Alpha display. This LED indicates a major SPC card circuit failure. If this is lighted, remove and reinsert the card. If the light illuminates again, replace the card.

Table 2: Alpha Display States

Display	Meaning
First Six Rows	
SPC	Card is SPC
Rotating line pattern	Download Progress Meter
Bottom Row	
1st LED (left) through the 4th LED (right)	Indicators for SRMs 1 through 4. A blinking LED indicates the associated SRM is configured. A constantly lighted LED indicates the SRM is populated but not configured. An unlighted LED indicates the SRM is not populated.
5th LED (right)	Heartbeat indicator. Normal operation is one on/off cycle per second. Erratic cycle may indicate a card overload. A stopped cycle may indicate a card failure (reboot or replace).

5.0 COMMUNICATIONS BUS INTERFACE

The communications bus is used by the Core Processor to communicate with the NBC. The Communications Bus Interface protocol is managed by hardware-based state machines assisted by an interrupt-based CPU support mechanism.

Supported features include high-speed parallel communications to the NBC3 and FLASH memory CPU-assisted download capability.

6.0 SERVICE RESOURCE MODULES

Each Service Resource Module (SRM) contains multiple Service Engines. Each engine consists of a single Digital Signal Processor (DSP) and associated RAM. The design of the SRM ensures that each Service Engine is a totally independent entity. Up to four SRMs may be populated per SPC, with eight engines per SRM.

Each Service Engine is connected to the PCM serial highways (and the PCM interface) through the Mezzanine Interface. These PCM serial highways contain both PCM data and command/response HDLC traffic from the Core Processor.

6.1 DSP-BASED SERVICE ENGINE

A Service Engine incorporates a sixteen-bit, fixed-point, digital signal processor (DSP) and SRAM memory. This signal processing engine contains several interface mechanisms:

- One TI TMS320LC548 (66MHz) DSP
- Two buffered serial ports
- One time division multiplexed interface serial port
- One host port interface
- 64K SRAM

6.2 MEZZANINE INTERFACE ARCHITECTURE

The Mezzanine interface is based upon a TDM traffic switched HDLC command/response architecture (refer to *Section 4.2*), with status and control registers for proper identification and reset control over the mezzanine locations. Additionally, the Mezzanine Interface uses a serial boot mechanism as its sole Core Processor master-to-slave boot device.

6.3 SERIAL MEZZANINE BOOT CONTROL

The SRM Core Processor provides serial boot control of the mezzanine SRMs. A continuous serial stream of boot code is targeted at a single DSP or to a group of DSP Service Engines. Any individual DSP or group of DSPs may be booted simultaneously.

7.0 PROGRAMMABILITY

The SPC supports a variety of service facilities implemented via software. This application software executes on the SRM's DSPs. This allows the SPC to support multiple tone plans and easily updated algorithm changes.

The following services are provided:

- DTMF detection
- Call progress analysis
- MF reception
- MFCR2 reception and transmission
- Tone generation
- DTMF and MF outpulsing
- Call conferencing

The individual SEs operate independently. This results in the ability to:

- download a service algorithm to one SE while the others are in service
- download different service algorithms to different SEs
- set or change the parameters of one SE while the others are in service
- configure the same service algorithm to multiple SEs

8.0 MEMORY SUBSYSTEM

The memory subsystem comprises components that interface to the Core Processor External Bus Interface. The Core Processor external bus consists of a 32-bit address bus, a 32-bit data bus, and several control signals to interface to a wide range of devices. This section discusses the configuration of the SPC's memory subsystem, which includes the FLASH and DRAM components.

8.1 MEMORY CONTROLLER

The interface between the Core Processor and external devices uses control signals and a configurable memory controller contained within the MPC860MHZP-50.

8.2 DRAM

DRAM is provided by 72-pin standard 32-bit wide Extended Data Out (EDO) 3.3V SO-DIMMs. SO-DIMM support is for multiple-bank 1 to 64 Mbyte modules with a maximum of two banks per module.

8.3 FLASH MEMORY

FLASH memory is the boot device. 8MB of FLASH are available for SPC and SE code to minimize boot-up time. The system controller can upgrade FLASH memory without users having to remove the card because the FLASH is hot-socketed.

9.0 PCM INTERFACE

The SPC PCM interface delivers up to 2016 time slots from the system backplane to service resources located on serial streams internal to the SPC. The PCM Interface is a full duplex mechanism, capable of time-space-time switching on both the transmit and receive paths. Per time slot loopback is provided for diagnostic mechanisms. Non-bandwidth-impacting loopback is provided to facilitate algorithms.

9.1 BUS SUPPORT

There are three PCM busses on the Cisco Systems backplane, known as the A, B, and C buses. The A and B buses are 8-bit parallel busses running at 8.192 MHz; the C-bus runs at 16.384 MHz. The C-bus is used with the ICC card to achieve 4K ports.

The PCM Interface performs the actual switching function. The interface routes 2016 full-duplex timeslots to the mezzanine interface and consists of functionally separate transmit, receive, and NBI switch matrixes.

The interface is of the non-blocking *time-space-time* type and is completely controlled by the local Core Processor.

10.0 POWER SUBSYSTEM

The power subsystem provides power to the on-board and mezzanine-based components on the SPC/SRM board pair, as well as protection from noise, over-current, and under/over voltage conditions. Alarming and voltage-monitored reset signals are provided to the Core Processor.

The power subsystem within the SPC mainboard is based upon two main functional components, the *hot swap controller* and the *switching regulator*. These components act together to protect the system from instantaneous current demands on any power rail that the SPC connects to, and additionally, to protect the SPC from dangerous events on the rails it depends upon.

11.0 CONFIGURATION NOTES

The SPC card is software configurable via downloads and FLASH only. There are no jumpers, sockets, or replaceable PROMs on the SPC card.

> *NOTE: An SRM that is configured in the database but is not physically installed will appear in the M (maintenance) state rather than the O (OOS) state.*

12.0 REMOVAL/REPLACEMENT PROCEDURES

Follow the directions in the VCO/4K Card Overview to remove or replace an SPC card.

12.1 REMOVING AN SRM MODULE

NOTE: Make sure you observe proper ESD procedures when handling this card. Have a wrist strap in place before replacing the card.

1. Remove the SPC card.
2. Using a screwdriver, remove the four screws holding the SRM in place (one at each corner). Ensure all hardware, including washers, is retained.
3. Gently remove the SRM, grasping it by the edges.
4. Replace the screws and washers on the SPC for future use.
5. Replace the SPC card in the system.

12.2 ADDING AN SRM MODULE

NOTE: Make sure you observe proper ESD procedures when handling this card. Have a wrist strap in place before replacing the card.

1. Remove the SPC card.
2. Using a screwdriver, remove the four screws and washers in the empty SRM location.
3. Gently insert the SRM on the two connectors. Be careful not to bend the board as you insert it. The large, square Altera component should face the back (connector side) of the SPC (refer to Figure 2). (The SRM is keyed to prevent improper insertion.)

   CAUTION: Do not press on semiconductor devices. Pressing above connectors, firmly snap in one and then the other connector. Hand tighten with screwdriver.

4. Secure the SRM (refer to Figure 4) with the four screws and washers removed in Step 2.

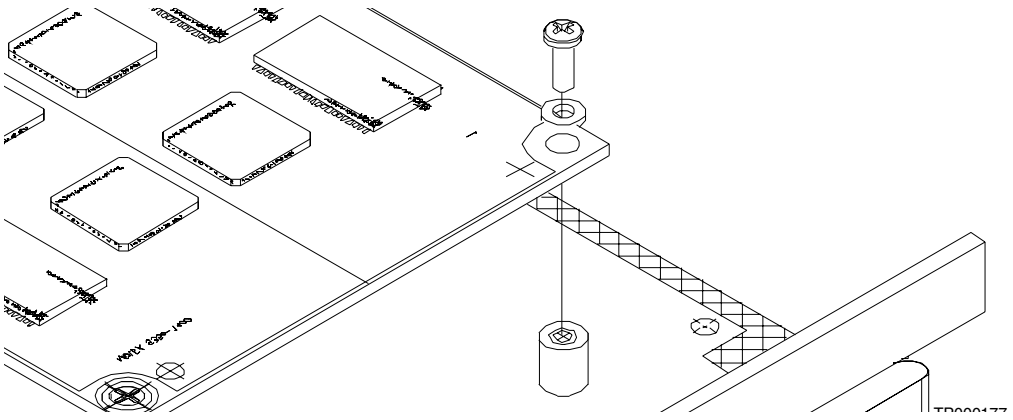


Figure 4: Securing the SRM

5. Replace the SPC card in the system.

13.0 RELATED DOCUMENTS

For additional information on the SPC card in VCO/4K Systems, refer to the following publications:

- *VCO/4K Hardware Planning Guide*
- *VCO/4K System Administrator's Guide*
- *VCO/4K System Maintenance Manual*

Direct Dial Inward Card (DDI)

1.0 GENERAL

The Direct Dial Inward (DDI) card is a standard port interface circuit card that resides in the Master or any Expansion Port Subrack. The DDI card provides interface to eight PBS-type (according to OFTEL standards) 2-wire terminating connections with a dedicated DTMF receiver and dial pulse detection. The DDI card supplies office battery. The A and B leads are surge protected.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM
	2K Bytes RAM
Power Requirements:	Typical Maximum
	+5 Volts:500 mA900mA
	+15 Volts:120 mA210mA
	–15 Volts:125 mA230mA
	+24 Volts:25 mA29mA*
	–48 Volts:38 mA nominal
	* per-port current requirements
Trunk Specifications:	
Input Level:	+3 dB ± 0.5 dBm
Output Level:	+3 dB ± 0.5 dBm
Crosstalk Attenuation:	68 dB minimum
Idle Circuit Noise:	23 dBrnc maximum
Line Impedance:	BS6305 Figure 4: 1982 (Complex Termination)
Echo Return Loss: (–2 dBm input)	18 dB minimum
Cable Loss:	0 dB minimum
	8 dB maximum
Singing Return Loss:	
Low (200 – 500Hz):	12 dB minimum
High (2500 – 3200Hz):	15 dB minimum

Frequency Response:
(Signal levels relative to 1004 Hz with C Message Filter)

60 Hz: –20 dB maximum
300 Hz:+3.0 +0.5 dB
600 to 2400 Hz:+3.0 +0.5 dB
3200 Hz:+3.0 +0.5 dB

Longitudinal Balance:

200–1000 Hz:60 dB minimum
1000–4000 Hz:50 dB minimum

Loop Current: 38 mA nominal (constant current source)

DTMF Receiver:

Detectable input level: –25 dBm minimum
1 dBm maximum

Acceptable twist: 10 dB maximum

Tone or quiet duration: 40 mS minimum

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the DDI. The five major elements of the DDI card are:

- Per Port Circuitry
- PCM Time Slot Bus Interface
- Packet Processor
- Control & Status Registers
- Protective Devices

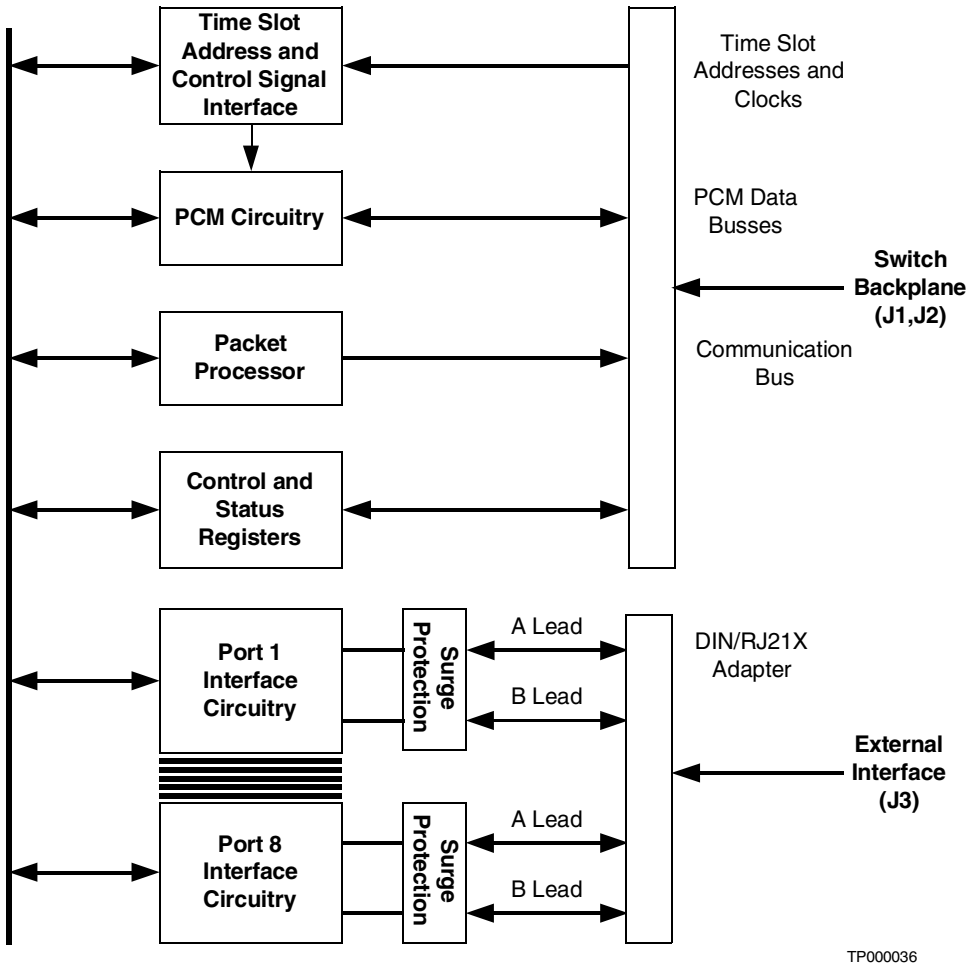


Figure 1: Block Diagram Of DDI Card

3.1 PER PORT CIRCUITRY

Each of the eight ports on a DDI card includes the following:

- DTMF Digit Receiver
- Analog to Digital Encoding and Decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On/Off hook detection
- Relay to reverse the A and B leads
- Surge protection across A and B leads.

3.1.1 DTMF DIGIT RECEIVER

A DTMF digit receiver integrated circuit (I.C.) is provided for each DDI port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

3.1.2 ANALOG TO DIGITAL ENCODING & DECODING

A 2913 codec provides digital-to-analog and analog-to-digital signal conversion. A codec semi-custom interface I.C. performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between itself and the codec.

Data received from both PCM busses is latched into parallel in/serial out shift registers internal to the codec interface I.C. The codec semi-custom interface I.C. supplies the data by selecting the output of one of the two internal parallel-to-serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode/decode A-law or µ-law PCM data. Two jumper areas on the DDI card allow selection of the clock frequency and PCM encoding rule for all eight codecs.

3.1.3 ANALOG INTERFACE

The analog interface consists of the circuitry from the A and B leads to the codec. An AMSþ2006 Subscriber Line Interface Circuit Hybrid performs the 2-wire to 4-wire conversion, provides internal lightning protection, and drives battery onto the A and B leads. The hybrid also monitors the current on the A and B leads to determine port on/off hook status, and outputs an on/off hook status bit. When a port is not terminated (on hook), the balance network is unbalanced. When this condition exists, an analog signal driven from the codec's receive amplifier into the hybrid is driven back to the input of the codec's transmit amplifier.

A DTMF digit receiver I.C. is connected to the analog signal output by the hybrid and input by the codec's transmit amplifier. A 3.5795 MHz crystal oscillator is provided to generate the clock signal required by the DTMF digit receivers.

3.1.4 CONTROL RELAY

A relay is provided for each DDI port. When energized by host command, the relay contacts reverse the A and B leads between the 2-wire/4-wire hybrid and the J3 connector. The relay is disabled when a line goes offhook.

3.1.5 A & B LEAD PROTECTIVE DEVICES

The A and B leads of the eight circuits on the DDI are protected from overvoltage and overload conditions as shown in Figure 2.

The SIDACtor™ on each port provides transient surge protection from lightning, line transients, and other damaging voltage spikes. This single package device protects against A Lead to B Lead, A Lead to Ground, and B Lead to Ground transients. When the monitored voltage exceeds 235Vac, the SIDACtor switches on through a negative resistance region to a low on-state voltage in nanoseconds. It continues to conduct until the current is interrupted or drops below the minimum holding current of the device.

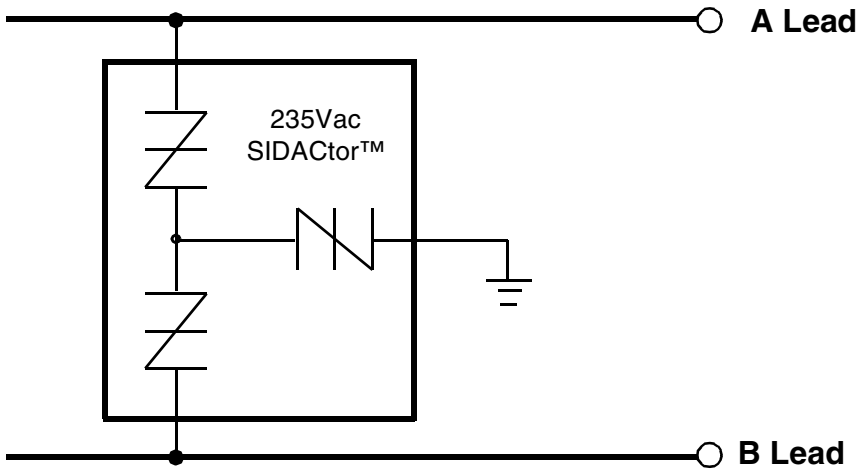


Figure 2: Schematic Diagram Of A & B Lead Protective Devices

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within a VCO/4K is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the DDI card translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The DDI card interfaces to the dual PCM time slot busses with bus interface circuitry common to several VCO/4K port-oriented circuit cards. Each of the eight port interfaces on the DDI card can “listen to” any time slot on either PCM data bus.

A DDI card is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular DDI card port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The DDI card contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the Master or Expansion Port Subracks with the exception of the Network Bus Controller (NBC). The Packet Processor polls each of the eight line/trunk connections looking for an event (i.e. off hook detection or valid DTMF digit reception). When polled by the NBC, the Packet Processor reports any status change. The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the DDI card.

The Communication Bus is the path by which the Packet Processor receives commands from and sends status to the Network Bus Controller.

3.4 PCM BUS INTERFACES — J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the DDI card.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.5 EXTERNAL INTERFACES

The connections to the A and B leads of the eight line/trunk interfaces on the DDI card are made via the J3 connector. A DIN to MDF adapter attaches to J3 and terminates the A/B lead connections of up to three DDIs to a standard RJ21X, 25-pair connector. It is expected that dry line/trunk connections be made via the RJ21X connector to the A and B leads of the individual lines/trunks (DDI card provides battery). The J3 pin assignments for each DDI card are provided as Table 2. J3 to RJ21X pinouts are shown in Table 3 and Figure 3.

Table 1: DDI Card J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (–48V)	Unused	Battery (–48V)
16	Battery (–48V)	Unused	Battery (–48V)
17	Battery (–48V)	Unused	Battery (–48V)
18	Analog –15V	Unused	Analog –15V
19	Analog –15V	Unused	Analog –15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DDI	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: DDI Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Unused
2	Trunk 1 – A Lead	Unused	Trunk 1 – B Lead
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – A Lead	Unused	Trunk 2 – B Lead
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – A Lead	Unused	Trunk 3 – B Lead
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Trunk 4 – A Lead	Unused	Trunk 4 – B Lead
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – A Lead	Unused	Trunk 5 – B Lead
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – A Lead	Unused	Trunk 6 – B Lead
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Trunk 7 – A Lead	Unused	Trunk 7 – B Lead
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – A Lead	Unused	Trunk 8 – B Lead
31	Unused	Unused	Unused
32	Unused	Unused	Unused

Table 3: J3 To RJ21X Pinouts

Card	Trunk	A Lead			B Lead		
1	1	J3-2A	to	RJ21X-26	J3-2C	to	RJ21X-1
1	2	J3-6A	to	RJ21X-27	J3-6C	to	RJ21X-2
1	3	J3-10A	to	RJ21X-28	J3-10C	to	RJ21X-3
1	4	J3-14A	to	RJ21X-29	J3-14C	to	RJ21X-4
1	5	J3-18A	to	RJ21X-30	J3-18C	to	RJ21X-5
1	6	J3-22A	to	RJ21X-31	J3-22C	to	RJ21X-6
1	7	J3-26A	to	RJ21X-32	J3-26C	to	RJ21X-7
1	8	J3-30A	to	RJ21X-33	J3-30C	to	RJ21X-8
2	1	J3-2A	to	RJ21X-34	J3-2C	to	RJ21X-9
2	2	J3-6A	to	RJ21X-35	J3-6C	to	RJ21X-10
2	3	J3-10A	to	RJ21X-36	J3-10C	to	RJ21X-11
2	4	J3-14A	to	RJ21X-37	J3-14C	to	RJ21X-12
2	5	J3-18A	to	RJ21X-38	J3-18C	to	RJ21X-13
2	6	J3-22A	to	RJ21X-39	J3-22C	to	RJ21X-14
2	7	J3-26A	to	RJ21X-40	J3-26C	to	RJ21X-15
2	8	J3-30A	to	RJ21X-41	J3-30C	to	RJ21X-16
3	1	J3-2A	to	RJ21X-42	J3-2C	to	RJ21X-17
3	2	J3-6A	to	RJ21X-43	J3-6C	to	RJ21X-18
3	3	J3-10A	to	RJ21X-44	J3-10C	to	RJ21X-19
3	4	J3-14A	to	RJ21X-45	J3-14C	to	RJ21X-20
3	5	J3-18A	to	RJ21X-46	J3-18C	to	RJ21X-21
3	6	J3-22A	to	RJ21X-47	J3-22C	to	RJ21X-22
3	7	J3-26A	to	RJ21X-48	J3-26C	to	RJ21X-23
3	8	J3-30A	to	RJ21X-49	J3-30C	to	RJ21X-24

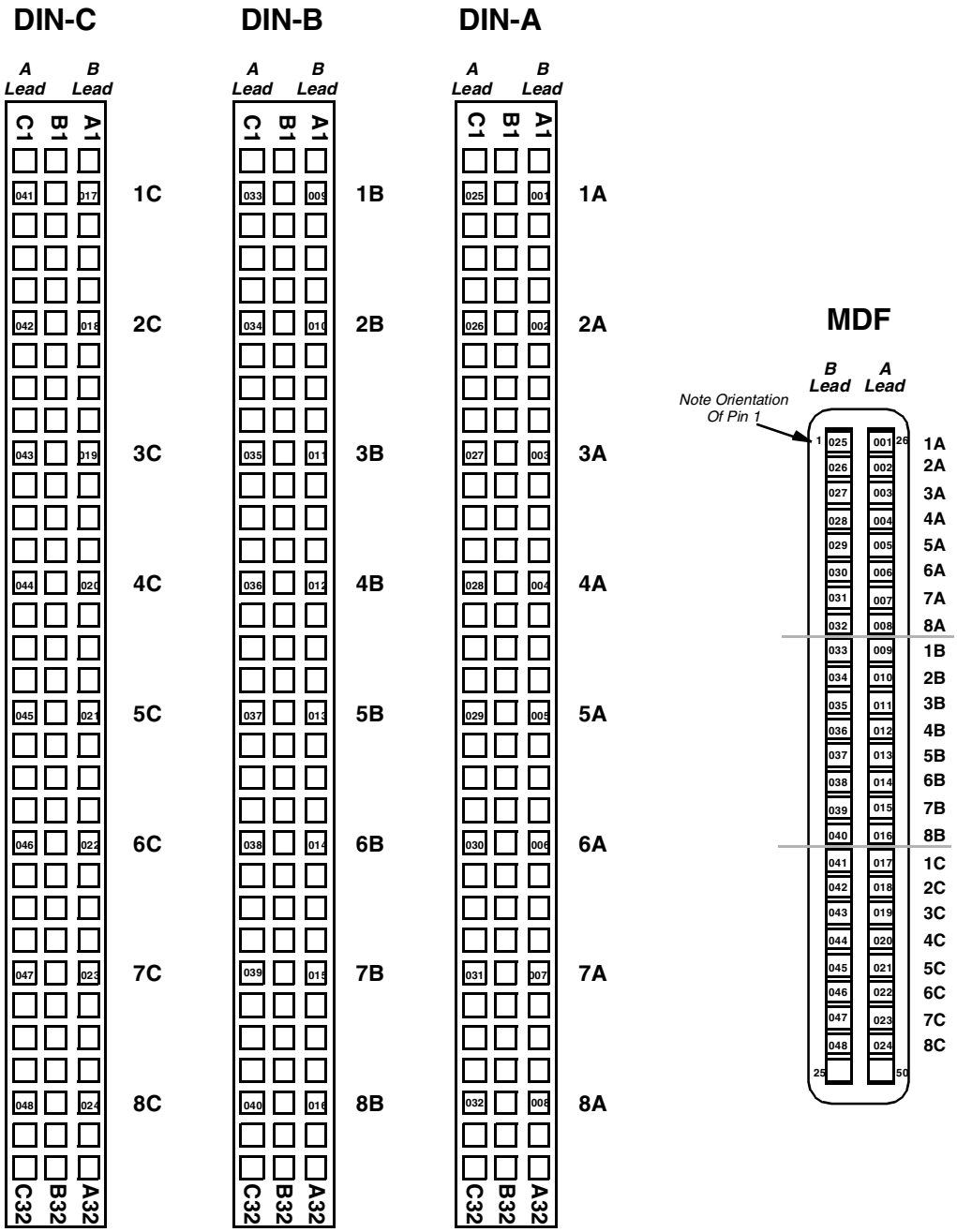


Figure 3: Pin-Out Diagram Of DIN–RJ21X MDF Adapter

4.0 CONFIGURATION NOTES

The DDI card is manufactured by Cisco Systems, Inc. Jumper plugs on the DDI card are factory set for use in VCO/4K systems. Figure 4 indicates the location and correct installation of jumper plugs on a DDI card based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it in a Port Subrack.

> *NOTE: The artwork revision level for the PCB itself (unpopulated) is etched on the solder side of the board near the front panel. The circuit card assembly part number, revision level and serial number appear on the component side of the PCB near the card front panel. The assembly part number includes four characters indicating the revision level. The first three characters are the actual revision level. The final letter "R" indicates that the PCB is at Release level. For example, a revision level A0L card is marked as Rev. "A0LR".*

If a card is improperly configured, it may fail to perform its interface function between external lines/trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a DDI card in the VCO/4K database, refer to the *VCO/4K System Administrator's Guide*.

Class of Service (COS) also greatly affects operation of the card. A COS of "T" or "2" sees inward seizures as call originations If calls are not being properly processed, check the COS.

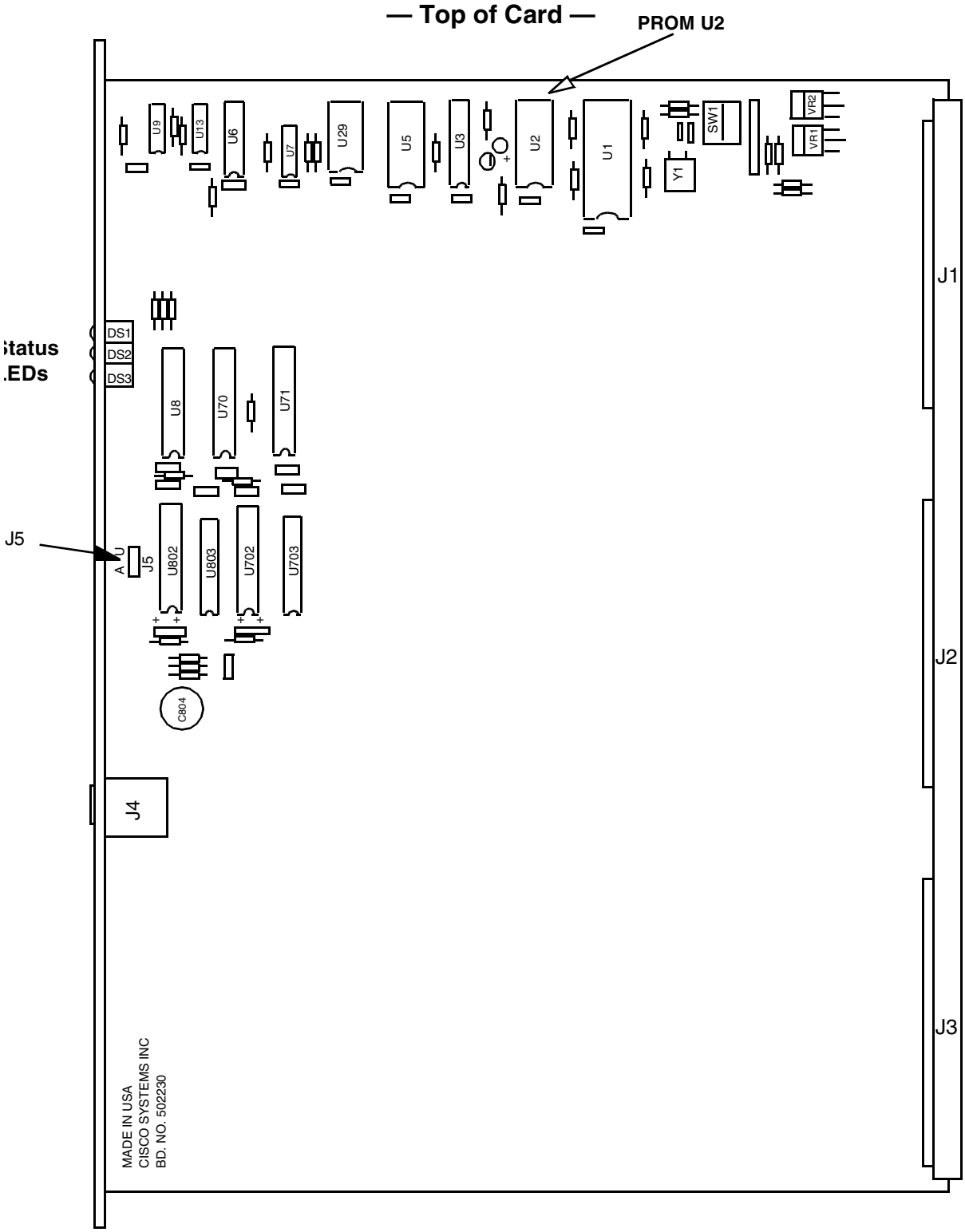


Figure 4: DDI Card J5 Jumper & U2 PROM Locations — P/N 50223080224

4.1 DIRECT DIAL INWARD CARD

J5 Jumper Locations

NOTE 1

- Install jumper plug at J5 in the “U” position for codec µlaw operation (North American standard).
- Install jumper plug at J5 in the “A” position for codec A-law operation (European standard).
  Position “A” (A-law) is the factory default setting for J5.

U2 PROM Location

The 2764 PROM in location U2 contains firmware appropriate to DDI card signaling interface requirements.

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation, and maintenance of the DDI card, refer to the following VCO/4K publications:

- United Kingdom Supplement
- VCO/4K System Administrator’s Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual

E1-Channel Associated Signalling Card (E1-CAS)

1.0 GENERAL

The E1-CAS is a standard port interface circuit card that resides in the master or any expansion port subrack. It operates at 2.048Mbps (32 X 64KHz channels), supports A-law/µ-law PCM coding or clear channel data, and uses channel associated signalling (CAS) with all bit positions of timeslot 16 in every frame reserved for bit-oriented signalling data transmission.

Electrical interface to the E1-CAS complies with CCITT G.703 standards using the E1 interface adapter. The 2.048Mbps data rate and channel signalling comply with CEPT (Conference of European Postal and Telecommunications administrators) recommendations for PCM switching interfaces.

System timing can be synchronized to an internal reference, a selected digital trunk, or an external reference. System software allows administrators to designate primary and secondary master timing links to which the system is synchronized. If both links fail or the external reference signal is lost, the system defaults to its internal reference clock (refer to the *System Administrator's Guide* for further information).

2.0 SPECIFICATIONS

CAS Processor

Microprocessor:Intel 8032 (12 MHz)

Memory: 64K Bytes EPROM
256K Bytes SRAM

Power Requirements: Typical

+5 Volts: 1500 mA

E1 Stream Specifications

Format: G.703 & G.732 with CRC framing

Ones Density:HDB3 coding

Frequency: 2.048 MHz ± 200 Hz

Impedance:75 ohms ± 10 ohms unbalanced-*or-*
120 ohms ± 10 ohms balanced

Jitter & Wander:Complies with CCITT G.823

3.0 CIRCUIT DESCRIPTION

The E1-CAS acts as an interface between a VCO/4K system with a digital data carrier stream. It receives and transmits a CEPT format, 2.048 Mbps, 32-channel (30 PCM telephone channels + 2 reserved framing & signalling channels), bipolar digital data stream synchronized with the system clocks. The E1-CAS receives a data stream of frequency 2.048 MHz $\pm$200 Hz and can drive a reference clock onto the system backplane which the communication bus (NBC) uses as an input to its system synchronization circuitry. The E1-CAS employs a clock adapter circuit which makes it compatible with all NBCs currently in the field.

The E1-CAS detects loss-of-carrier errors, framing errors, and remote alarms, on its incoming data stream. It also detects *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus. The E1-CAS contains an elastic PCM data buffer to minimize slips caused by incoming data stream frequency jitter.Figure 1 is a simplified block diagram of the E1-CAS card.

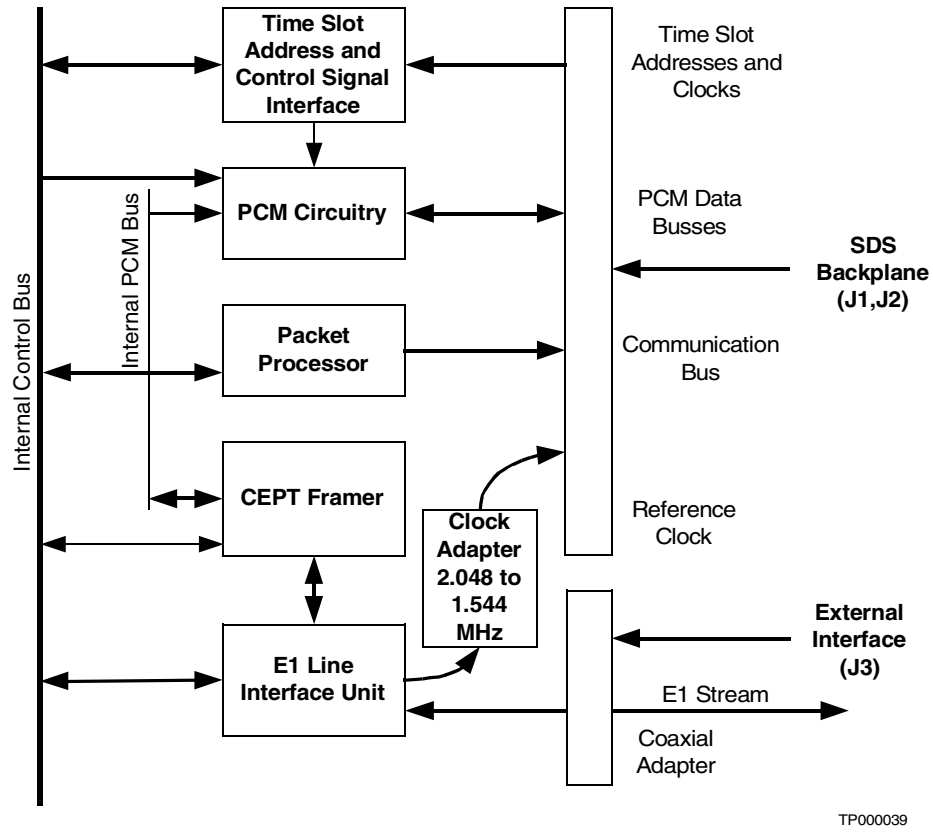


Figure 1: Block Diagram of E1-CAS Card

3.1 OVERVIEW OF CIRCUIT OPERATION

The E1-CAS frames incoming and outgoing PCM data in accordance with CEPT requirements. All internal operations are controlled by processor firmware in ROM. All framing is synchronized to internal or external clock sources as selected in the system data base.

The physical interface to the PCM stream is through a VCO/4K I/O module. The adapter supports UG-1094 A/U type 75Ω unbalanced, or 120Ω balanced coaxial connections.

4.0 PHYSICAL INTERFACE

Physical interface with the PCM stream is through a Line Interface Unit (LIU) and a CEPT framer. Together these devices support direct connection to the Packet Task through J3. A Layer 1 device driver based on CCITT Recommendation I.431 controls the LIU and CEPT framer.

The LIU performs the following functions:

- Lightening and short circuit protection
- Clock recovery
- Jitter attenuation
- Bipolar to TTL conversion
- Wave shaping
- Line buildout control
- Loopback and maintenance functions
- Data transparency selection

Associated channel signalling uses timeslot 16 of each frame in a 16-frame multiframe. This timeslot contains network and signalling information about the other channels in the frame.

Framing functions are implemented under packet task control via the framer. The framer performs the following functions

- Alarm detection
- Alarm mode selection
- Channel separation
- Drop and insert control

Data Transparency is provided by the HDB3 (high density bipolar 3) method as specified in CCITT, G.703, Annex A for 2048Kbps operation.

4.1 PACKET PROCESSOR

The packet processor consists of the 8032 microcomputer and associated RAM, EPROM, and address decode circuitry; communication bus interface; an asynchronous serial port; and the LED register. The 8032 provides the intelligence for the packet processor, and therefore for the E1-CAS interface card.

The communication bus is the path by which the packet processor receives commands from and sends status to the NBC.

A packet processor is part of all cards in the master or expansion port subracks with the exception of the NBC. The packet processor polls the E1 LIU looking for an event (i.e., error condition or signalling bit transition). When polled by the NBC, the packet processor reports any status change and controls three status LEDs (red, yellow, and green) that are visible through the card's front panel. The packet processor supports a diagnostic serial port connected to a signal line on the backplane.

4.2 CEPT FRAMER

The framer interfaces to a CEPT, 2.048Mbps digital trunk through the LIU. It provides clear channel capability through appropriate zero suppression and signalling modes. System ones density is maintained through HDB3 (High Density Bipolar 3) coding. HDB3 coding is pseudo-ternary with three states noted as B+, B– and 0. Spaces in the binary signal are coded as spaces in the HDB3 signal. Violations of the rule for alternate mark inversion (AMI) are introduced when coding strings of four spaces occur.

The transmit framer/formatter circuits generate appropriate framing bits, supervise zero suppression, generate alarms, and provide output clocks for data conditioning and decoding. The receiver/synchronizer circuits establish frame and multiframe boundaries, extract signalling data and report alarms and signalling formats.

Channel Associated Signalling (CAS) is a bit-oriented technique which uses a 16-frame multiframe. The multiframe alignment signal, extra and alarm bits occupy timeslot 16 of frame 0. Timeslot 16 of the remaining 15 frames is reserved for channel signalling data.

The CEPT framer recognizes the PCM signalling codes defined in the following tables.

Table 1 lists the E1 alarm conditions and their meanings.

Table 1: E1 Signaling Alarm Conditions

Local Condition[1]	Declare In	Clear In	LED	Transmit
Loss of Carrier	2 seconds	10 seconds	Red	RAI
Loss of Frame	2 seconds	10 seconds	Red	RAI
Received AIS[2]	2 seconds	10 seconds	Red	RAI
Received RAI	500 ms	500 ms	Yellow	In-frame
Received DMA[3]	500 ms	500 ms	Yellow	In-frame
E1 Out of Service	—	—	Green	AIS
E1 Maintenance	—	—	—	—
Slip Threshold	255 slips	—	—	—
OOF Threshold	17 occurrences	—	—	—

1 *Prompt indications of these events are made to the system controller.*

2 *Alarm Indication Signal (AIS) is a steady all-ones signal, and can be detected in the presence of an error rate of 0.001.*

3 *Received DMA is indicated as a Signaling Bit Alarm and Received AIS is indicated as Loss of Frame.*

CAS multiframe sync is declared when the multiframe alignment pattern is properly detected and timeslot 16 of the previous frame contains code other than zeros. If no valid pattern can be found in 12 to 14 milliseconds, frame search is restarted.

Figure 2 shows how four signalling bits (A, B, C and D) are transmitted once per multiframe.

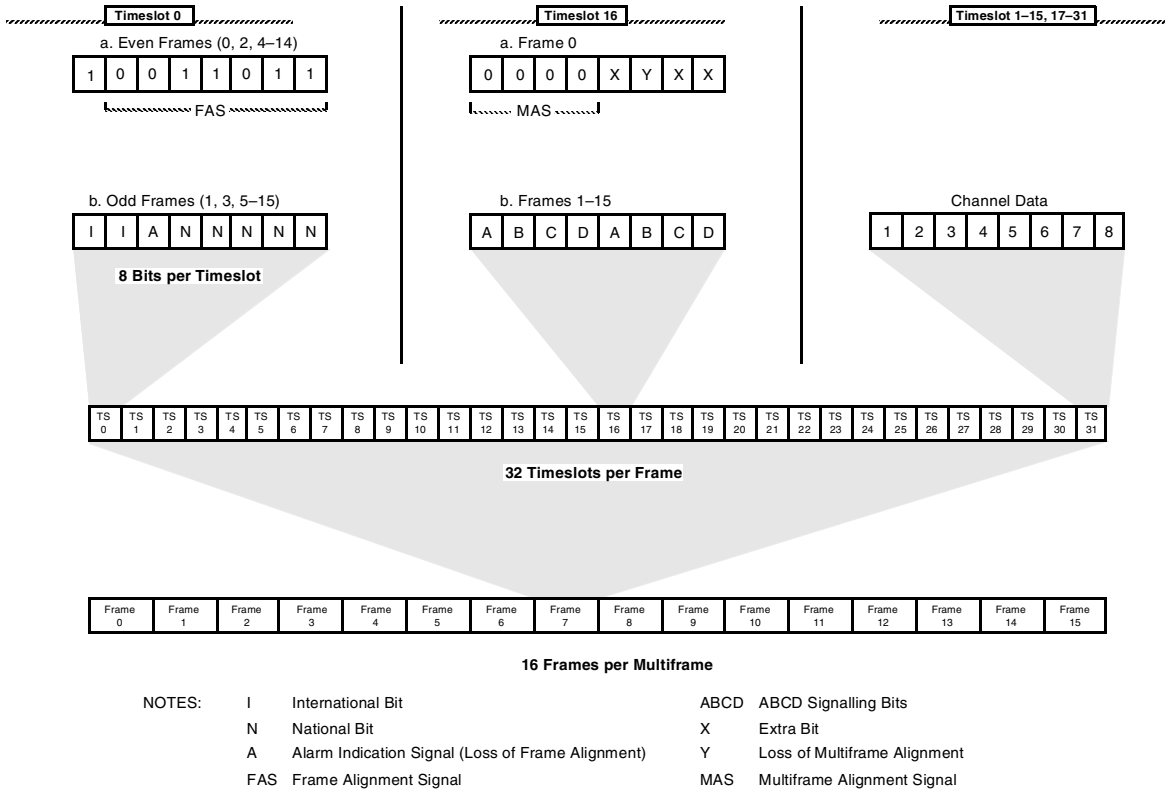


Figure 2: CAS Multiframe Format

4.3 LINE INTERFACE UNIT

The LIU employed on the E1-CAS is a fully integrated transceiver designed for CEPT operation. It performs line driver, data recovery and clock recovery functions. The LIU supports full-duplex transmission of digital data over 75Ω unbalanced for 120Ω balanced installations in accordance with CCITT, G.703 interface specifications.

4.4 E1 LED STATES

The LED status appears on the front of the E1 card. The following signalling conditions apply to each LED.

- Red (top) LED: Signals a problem with an inward E1 stream (carrier loss, OOF or AIS).
- Yellow (center) LED: Signals a Remote E1 Alarm on the E1 stream (refer to Table 2, Table 3, and Table 4).
- Green (bottom) LED: Illuminates until the card is placed into service.

Table 2: CCITT, Q.421 "R2" PCM Signalling Codes – Normal Conditions

State of the Circuit	Signalling Code			
	Forward		Backward	
	A*f*	B*f*	A*b*	B*b*
Idle/Released	1	0	1	0
Seized	0	0	1	0
Seizure Acknowledged	0	0	1	1
Answered	0	0	0	1
Clear Back	0	0	1	1
Clear Forward	1	0	0	1
			– or –	
			1	1
Blocked	1	0	1	1

NOTE: C and D bits are always set to "01" for Q.421 Digital Signalling

Table 3: CCITT, Q.422 PCM Signalling Codes – Outgoing End

Normal State at the Outgoing End	Transmitted Code	Received Code			
		A*b* = 0 B*b* = 0	**A*b* = 0, B*b* = 1**	**A*b* = 1, B*b* = 0**	**A*b* = 1, B*b* = 1**
Idle/Released	A*f* = 1, B*f* = 0	Abnormal Minor Alarm	Abnormal Minor Alarm	Idle	Blocked
Seized	A*f* = 0, B*f* = 0	Abnormal Minor Alarm	Abnormal Minor Alarm	Seized	Seizure Acknowledged
Seizure Acknowledged	A*f* = 0, B*f* = 0	Abnormal Minor Alarm	Answered	Abnormal Minor Alarm	Seizure Acknowledged
Answered	A*f* = 0, B*f* = 0	Abnormal Minor Alarm	Answered	Abnormal Minor Alarm	Clear Back
Clear Back	A*f* = 0, B*f* = 0	Abnormal Minor Alarm	Answered	Abnormal Minor Alarm	Clear Back
Clear Forward	A*f* = 1, B*f* = 0	Abnormal Minor Alarm	Clear Forward	Released = Idle	Clear Forward
Blocked	A*f* = 1, B*f* = 0	Abnormal Minor Alarm	Abnormal Minor Alarm	Idle	Blocked

Table 4: CCITT, Q.422 PCM Signalling Codes – Incoming End

Normal State at the Outgoing End	Transmitted Code	Received Code			
		A*f* = 0 B*f* = 0	**A*f* = 0, B*f* = 1**	**A*f* = 1, B*f* = 0**	**A*f* = 1, B*f* = 1**
Idle/Released	A*b* = 1, B*b* = 0	Seized	Abnormal Minor Alarm	Idle	Abnormal Minor Alarm
Seizure Acknowledged	A*b* = 0, B*b* = 0	Seizure Acknowledged	Abnormal Minor Alarm	Clear Forward	Abnormal Minor Alarm
Answered	A*b* = 0, B*b* = 0	Answered	Abnormal Minor Alarm	Clear Forward	Abnormal Minor Alarm
Clear Back	A*b* = 0, B*b* = 0	Clear Back	Abnormal Minor Alarm	Clear Forward	Abnormal Minor Alarm
Clear Forward	A*b* = 1, B*b* = 0	Abnormal Minor Alarm	Abnormal Minor Alarm	Clear Forward	Abnormal Minor Alarm
Blocked	A*b* = 1, B*b* = 0	Abnormal Minor Alarm	Abnormal Minor Alarm	Blocked	Abnormal Minor Alarm

4.5 PCM BUS INTERFACES – J1 PIN ASSIGNMENTS

Table 5 lists the J1 pin assignments on the E1-CAS card.

Table 5: E1-CAS Card J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	–24V	Unused	+24V
15	Battery (–48V)	Unused	Battery (–48V)
16	Battery (–48V)	Unused	Battery (–48V)
17	Battery (–48V)	Unused	Battery (–48V)
18	Analog –15V	Unused	Analog –15V
19	Analog –15V	Unused	Analog –15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	Unused	Unused	Unused
30	AGND	Unused	AGND

Table 5: E1-CAS Card J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
31	AGND	Unused	AGND
32	DGND	Unused	DGND

NOTE: J2 Pin Assignments are proprietary and not documented for customer use.

5.0 EXTERNAL INTERFACES

Connections to the incoming and outgoing E1 digital data streams are made via the J3 connector. A DIN to MDF adapter attaches to the J3 connector and allows external connection to the E1-CAS card via UG-1094 A/U type female coaxial connectors (one transmit + one receive connection per span). Table 6 lists the J3 connector pinouts for the E1-CAS card.

Table 6: E1-CAS Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Digital Ground
2	Unused	Unused	Reserved
3	Unused	Unused	Rcv Line Tip[1]
4	Unused	Unused	Rcv Line Ring[1]
5	Unused	Unused	Xmt Line Tip[2]
6	Unused	Unused	Xmt Line Ring2
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Unused	Unused	Unused
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Unused	Unused	Unused
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Unused	Unused	Unused
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused

Table 6: E1-CAS Card J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
22	Unused	Unused	Unused
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Unused	Unused	Unused
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	GND
30	Unused	Unused	RS-232 DX (Out)
31	Unused	Unused	RS-232 DX (In)
32	Unused	Unused	Unused

1. Signal to E1-CAS

2. Signal from E1-CAS

Figure 3 shows the J3 to coaxial connector pinouts.

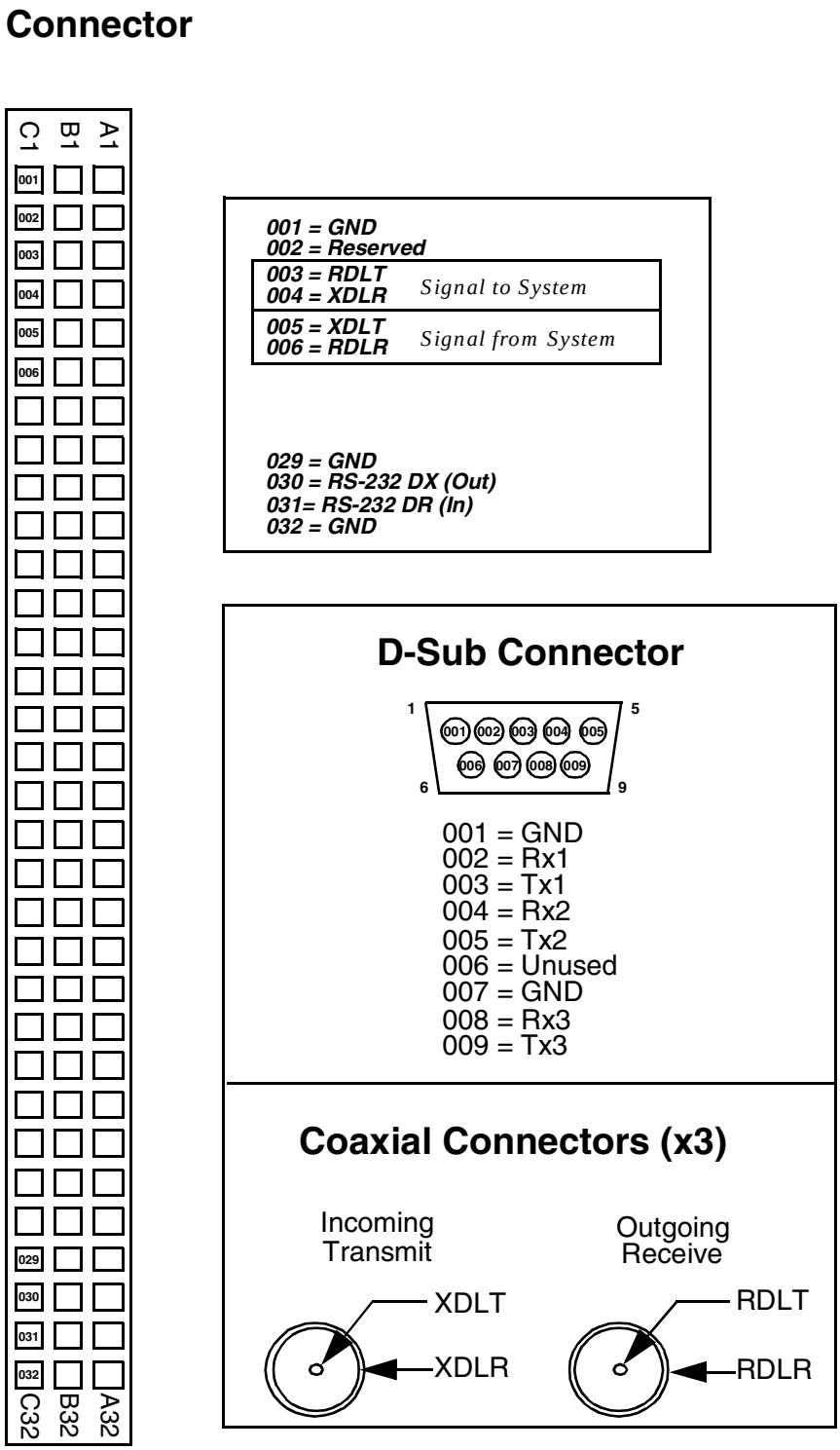


Figure 3: Pinout Diagram of E1/E1-PRI Adapters

6.0 CONFIGURATION NOTES

The E1-CAS is manufactured by Cisco Systems, Inc. Figure 4 shows the E1-CAS jumper settings and locations.

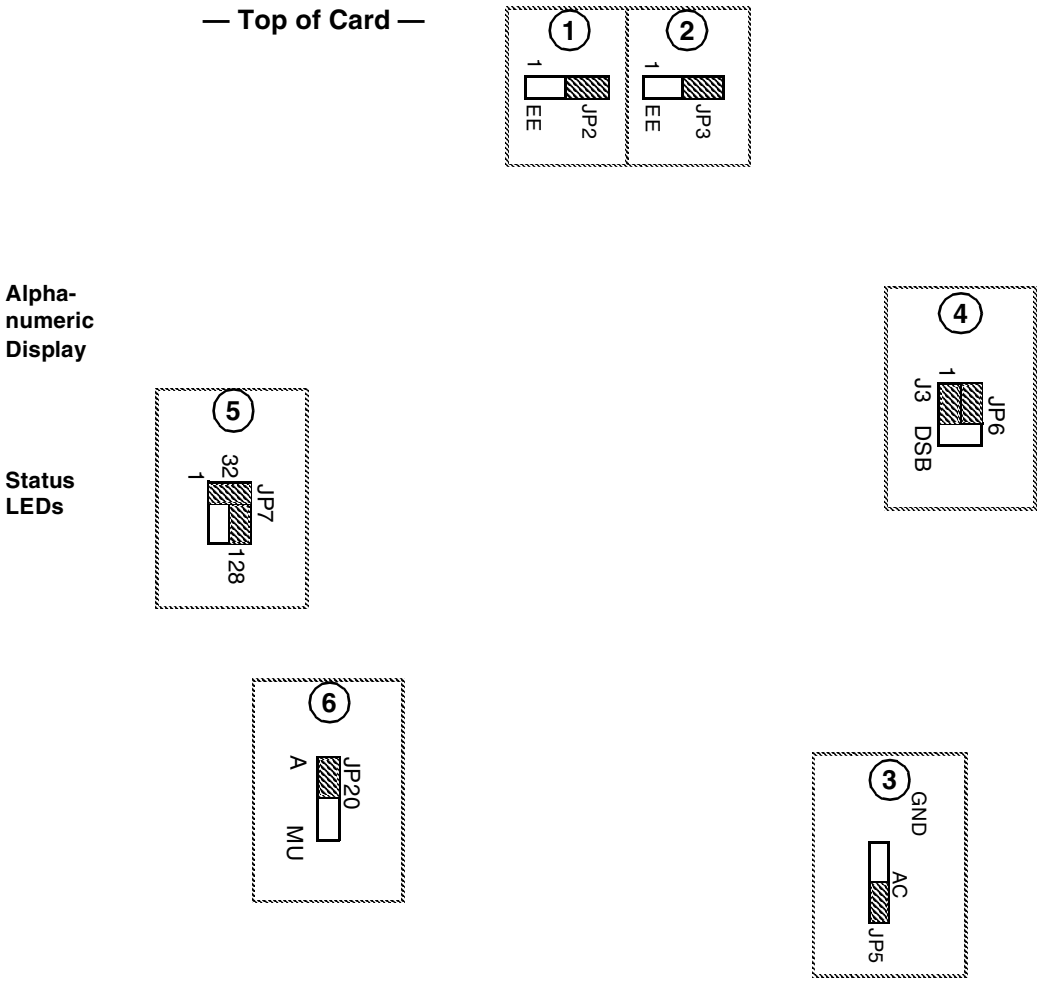


Figure 4: E1-CAS Card Jumper Locations

Use Figure 4 to verify configuration jumper settings before installing the E1-CAS. If a card is improperly configured, it will not perform its interface function between external spans and the system.

Port Configuration refers to specifying appropriate data for each port in the system data base, including line equalization. If the port is improperly configured, the system may improperly interpret the incoming E1 stream. For additional information about configuring an E1-CAS in the system data base, refer to the applicable country supplement.

6.1 DIP SWITCH

DIP switch 1 controls both the static settings of the outbound C- and D-channel associated signalling bits, and the PCM gain injection and companding law conversion.

> *Note: DIP switch 1 is factory set and should not be changed. The default settings are all closed.*

Jumper JP20 on each E1 card indicates the PCM companding law switched over the system backplane. JP20 and DIP switch 1 should both indicate an A-Law trunk conversion. If the settings are different, companding law conversion is performed. Law conversion occurs in both directions and on all timeslots with the exception of the CAS signalling channel (TS-16).

> *NOTE: Be sure that JP20 and the DIP switch are set correctly for your application before powering up the system. It is important that JP20 corresponds to the companding law used by your DTG card. For more information, contact Cisco Systems, Inc. Technical Support.*

7.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the E1, refer to the following documentation:

- VCO/4K Product Overview
- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- Technical Description: Port Subrack

Earth/Loop Connect Trunk Card (ECT/LCT)

1.0 GENERAL

The Earth and Loop Connect Trunk (ECT/LCT) card is a standard VCO/4K port interface circuit card that can reside in any slot other than those reserved for the control system cards. This card supports eight PAS-type, 2-wire, originating and terminating trunk connections; the CO must supply office battery. Terminating characteristics include:

- 2-wire interface with ringdown detect
- ring trip capability
- A dedicated DTMF receiver

Originating characteristics include:

- 2-wire, loop calling (LCT) or earth calling (ECT)
- Battery reversal detection and wink detect

2.0 SPECIFICATIONS

Microprocessor	8031 (12 MHz)
Memory	8K Bytes EPROM 2K Bytes RAM
Power Requirements	+5 Volts: 700mA (typical) +15 Volts: 150mA (typical) –15 Volts: 160mA (typical)
Trunk Specifications:	
Input Level	+3 dB ± 0.5 dBm
Output Level	+3 dB ± 0.5 dBm
Line Impedance	BS6305, Figure 5 (Complex Termination)
Crosstalk Attenuation	75 dB minimum
Idle Circuit Noise	23 dBrnc maximum
Echo Return Loss (Line to Trunk)	20 dB minimum
Cable Return Loss	0 dB minimum 8 dB maximum
Singing Return Loss (Line to Trunk)	12 dB minimum (low) to 15 dB minimum (high)
Single Freq. Return Loss (Line to Trunk)	16 dB minimum, 200 to 4000 Hz
Frequency Response (Signal levels relative to 1004 Hz with C Message Filter)	60 Hz: -20 dB maximum 200 Hz: -3 to 0.0 dB 300 to 3000 Hz: -1 to 0.5 dB 3400 Hz: -3 to 0.0 dB

Longitudinal Balance	200 – 4000 Hz: 60 dB minimum
Operating Loop Current	16 mA to 100 mA
DTMF Receiver	
Detectable input level	-25 dBm minimum 1 dBm maximum
Acceptable twist	10 dB maximum
Tone or quiet duration	40 mS minimum

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the ECT/LCT. The five major elements of the ECT/LCT are:

- Per Port Circuitry
- PCM Time Slot Bus Interface
- Packet Processor
- Control & Status Registers
- Protective Devices

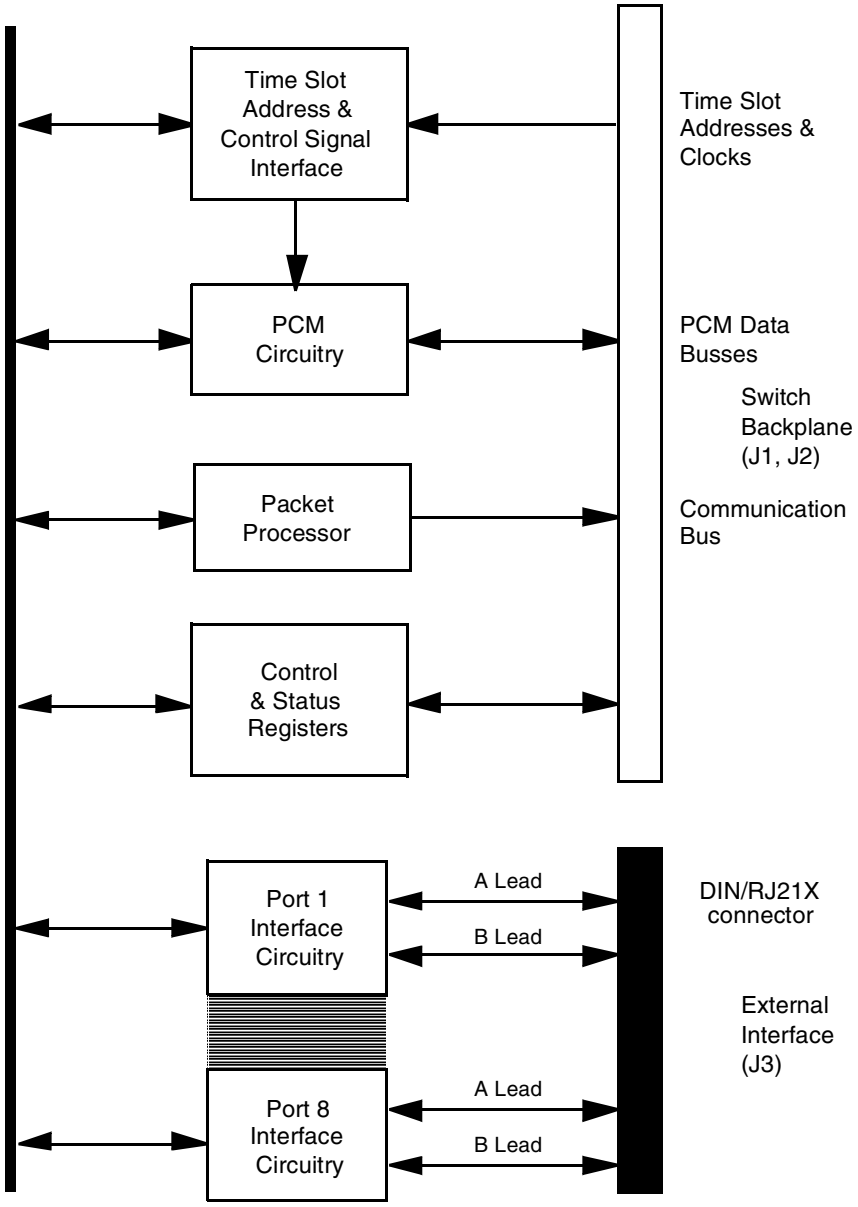


Figure 1: Block Diagram Of ECT/LCT

3.1 PER PORT CIRCUITRY

Each of the eight ports on the ECT/LCT include the following:

- DTMF digit receiver
- Analog to digital encoding and decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On/Off hook detection
- Earth start relay (grounds B lead)
- Incoming ring voltage detection
- Battery reversal and current detection

3.2 DTMF DIGIT RECEIVER

A DTMF digit receiver integrated circuit (I.C.) is provided for each ECT/LCT card port. The receiver is connected to the incoming analog signal and can identify DTMF digits zero through nine, A, B, C, D, #, and *.

3.3 ANALOG INTERFACE

The analog interface consists of circuitry from the A and B leads to the input of the code device. A high-impedance op-amp circuit detects battery reversal conditions. The ring voltage detector is connected across the A and B leads; the normally open relay contacts are connected to the B lead and to battery ground. When the relay is energized, battery ground is applied to the B lead for ground start trunk seizing.

Voiceband energy presented to the A and B leads is coupled to the negative input of the codec's transmit amplifier via the transformer and the hybrid circuit. Voice and energy driven by the codec's receive amplifier is coupled to the A and B leads via the hybrid circuit and transformer.

The DTMF digit receiver I.C. is connected to the output of the codec transmit amplifier. A single 3.5795 MHz crystal oscillator package provides the clock input required by the DTMF receivers.

3.4 ON/OFF HOOK & EARTH START RELAYS

Before a call can be initiated or answered on a trunk connected to an ECT/LCT port, the trunk must first be set off-hook. On-board relays control the off-hook process. Call processing software causes the appropriate port to go off-hook allowing current to flow. The current (if battery is being provided by an external source such as a Central Office trunk) is detected by one of the two current detectors. The earth start relay seizes a ground start trunk by grounding the B lead of the trunk.

3.5 RING VOLTAGE AND CURRENT FLOW DETECTORS

Ring voltage, battery reversal and current detectors are provided for each ECT/LCT port. The ring voltage detector alerts the packet processor to answer an incoming call.

Current flow detectors allow the packet processor to determine winks and other port activity. When a port is set off hook, a control register bit goes low to indicate that current is flowing in the normal direction. If an open circuit or reverse battery wink occurs, this bit goes high for the duration of the wink. The on/off hook relay must be set off hook to detect current, but need not be off hook to detect ring voltage.

3.6 PCM TIME SLOT BUS INTERFACE

All voice data within the system is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the ECT/LCT translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The ECT/LCT interfaces to the dual PCM time slot busses with bus interface circuitry common to several port-oriented circuit cards. Each of the eight port interfaces on the ECT/LCT can “listen to” any time slot on either PCM data bus.

An ECT/LCT is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular ECT/LCT port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.7 PACKET PROCESSOR

The ECT/LCT contains an 8031-based Packet Processor that interfaces to the communication bus. All port interface cards and service circuit cards have a packet processor. The Packet Processor polls each of the eight trunk connections looking for an event (i.e., ring detection or valid DTMF digit reception). When polled by the NBC/NBC-3, the packet processor reports any status change.

The packet processor supports a diagnostic serial port connected to a signal line on the backplane. The packet processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The packet processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the communication bus interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the packet processor and, therefore, for the ECT/LCT. The communication bus is the path by which the packet processor receives commands from and sends status to the Network Bus Controller.

3.8 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the ECT/LCT.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.9 EXTERNAL INTERFACES

The connections to the A and B leads of the eight line/trunk interfaces on the ECT/LCT are made via the J3 connector. A DIN to the I/O module attaches to J3 and terminates the A/B connections of up to three ECT/LCTs to a standard RJ21X, 25-pair connector. It is expected that wet trunk connections be made via the RJ21X connector to the A and B leads of the individual trunks. The J3 pin assignments for are provided as Table 2. J3 to RJ21X pinouts are shown in Table 3 and Figure 2.

Table 1: ECT/LCT J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V

Table 1: ECT/LCT J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: ECT/LCT J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Unused
2	Trunk 1 – A Lead	Unused	Trunk 1 – B Lead
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – A Lead	Unused	Trunk 2 – B Lead
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – A Lead	Unused	Trunk 3 – B Lead
11	Unused	Unused	Unused
12	Unused	Unused	Unused

Table 2: ECT/LCT J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
13	Unused	Unused	Unused
14	Trunk 4 – A Lead	Unused	Trunk 4 – B Lead
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – A Lead	Unused	Trunk 5 – B Lead
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – A Lead	Unused	Trunk 6 – B Lead
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Trunk 7 – A Lead	Unused	Trunk 7 – B Lead
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – A Lead	Unused	Trunk 8 – B Lead
31	Unused	Unused	Unused
32	Unused	Unused	Unused

Table 3: J3 to RJ21X Pinouts

Card	Trunk	A Lead	B Lead
1	1	J3-2A to RJ21X-26	J3-2C to RJ21X-1
1	2	J3-6A to RJ21X-27	J3-6C to RJ21X-2
1	3	J3-10A to RJ21X-28	J3-10C to RJ21X-3
1	4	J3-14A to RJ21X-29	J3-14C to RJ21X-4
1	5	J3-18A to RJ21X-30	J3-18C to RJ21X-5

Table 3: J3 to RJ21X Pinouts (Continued)

Card	Trunk	A Lead	B Lead
1	6	J3-22A to RJ21X-31	J3-22C to RJ21X-6
1	7	J3-26A to RJ21X-32	J3-26C to RJ21X-7
1	8	J3-30A to RJ21X-33	J3-30C to RJ21X-8
2	1	J3-2A to RJ21X-34	J3-2C to RJ21X-9
2	2	J3-6A to RJ21X-35	J3-6C to RJ21X-10
2	3	J3-10A to RJ21X-36	J3-10C to RJ21X-11
2	4	J3-14A to RJ21X-37	J3-14C to RJ21X-12
2	5	J3-18A TO RJ21X-38	J3-18C to RJ21X-13
2	6	J3-22A to RJ21X-39	J3-22C to RJ21X-14
2	7	J3-26A to RJ21X-40	J3-26C to RJ21X-15
2	8	J3-30A to RJ21X-41	J3-30C to RJ21X-16
3	1	J3-2A to RJ21X-42	J3-2C to RJ21X-17
3	2	J3-6A to RJ21X-43	J3-6C to RJ21X-18
3	3	J3-10A to RJ21X-44	J3-10C to RJ21X-19
3	4	J3-14A to RJ21X-45	J3-14C to RJ21X-20
3	5	J3-18A to RJ21X-46	J3-18C to RJ21X-21
3	6	J3-22A to RJ21X-47	J3-22C to RJ21X-22
3	7	J3-26A to RJ21X-48	J3-26C to RJ21X-23
3	8	J3-30A to RJ21X-49	J3-30C to RJ21X-24

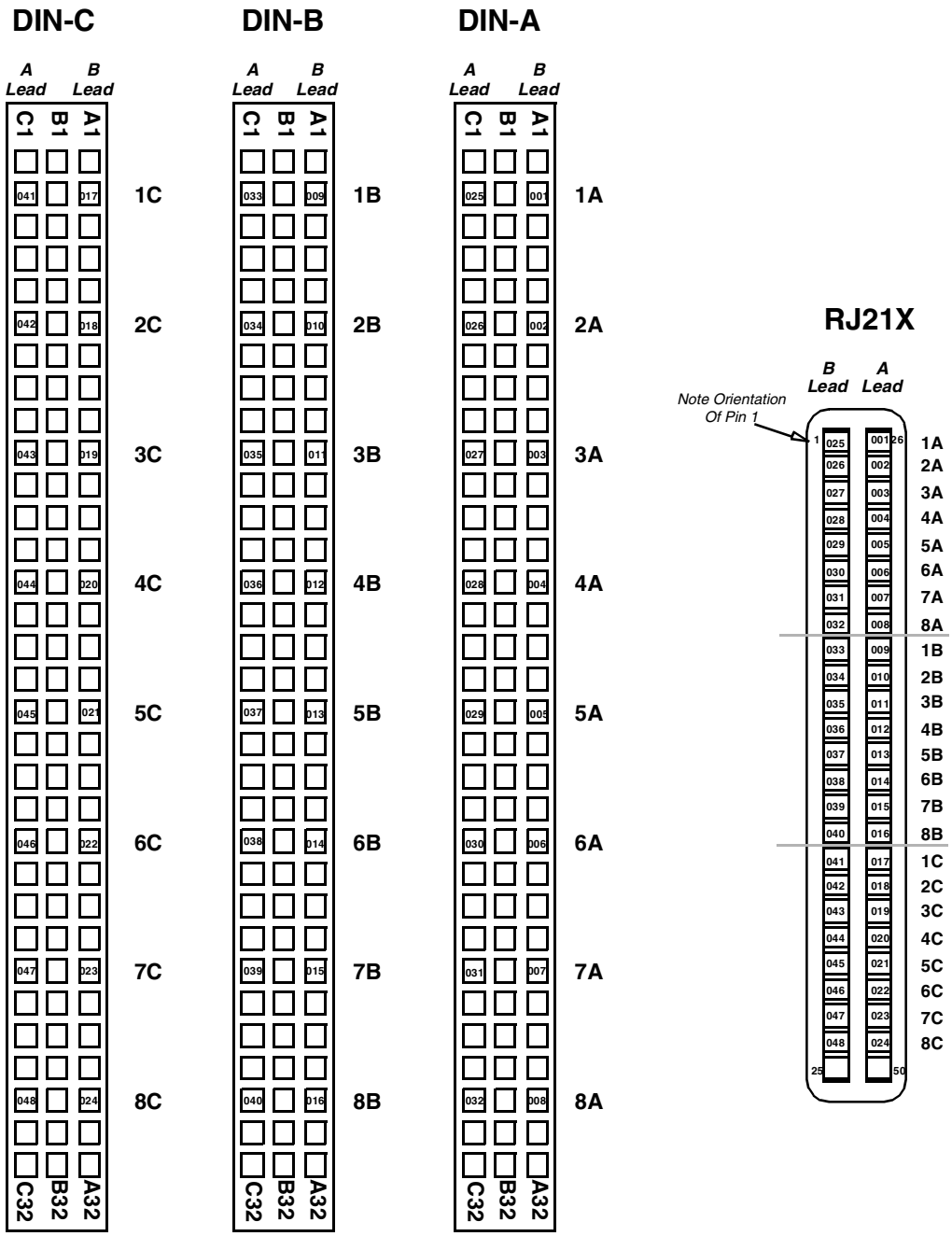


Figure 2: Pin-Out Diagram Of DIN–RJ21X Connector

4.0 CONFIGURATION NOTES

The ECT/LCT is manufactured by Cisco Systems, Inc. Jumper plugs on the ECT/LCT are factory set for use in the systems. Figure 3 indicates the location and correct installation of jumper plugs and wires on ECT/LCT based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the component side of the PCB near the card front panel. The PCB is etched with four characters indicating the revision level. The first three characters are the actual revision level. The final letter "R" indicates that the PCB is at Release level. For example, a revision level A0L card is marked as Rev. "A0LR".*

If a card is improperly configured, it may fail to perform its interface function between external trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring an ECT/LCT in the data base, refer to the *System Administrator's Guide*.

Class of Service (COS) also greatly affects operation of the card. A COS of "T", "2" or "A2" sees inward seizures as call originations. A COS of "O" interprets inward seizures as the port being busied out by the far end. If calls are not being properly processed, check the COS.

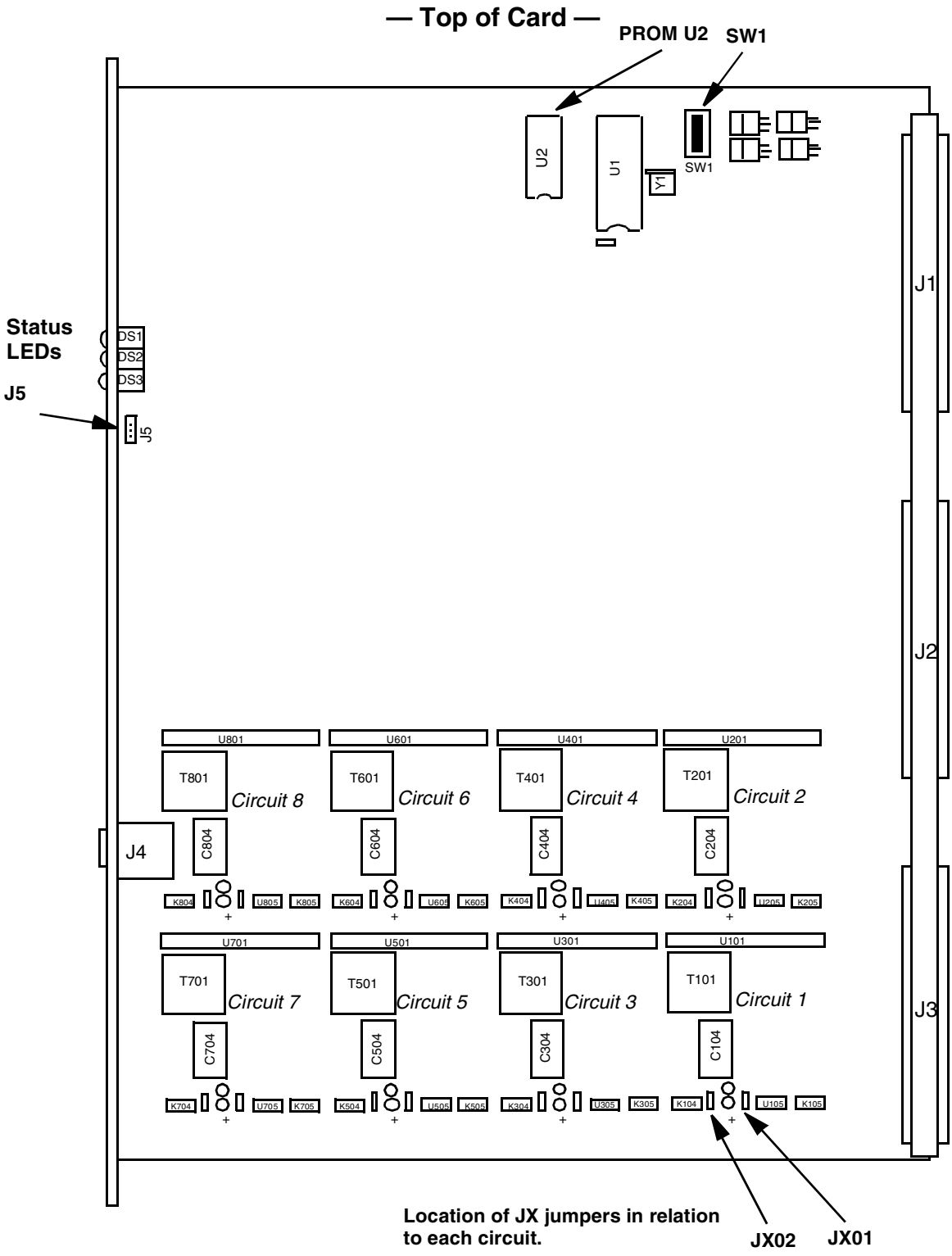


Figure 3: ECT/LCT Jumper & PROM Locations

4.1 EARTH CALLING

Jumper and Switch Locations

NOTE 1

When jumpers are installed at locations JX01 and JX02 (X = circuits 1 through 8), the card signals in earth calling format.

NOTE 2

The SW1 dip switch settings at this location have no effect on earth calling processing.

NOTE 3

- Install jumper plug at J5 in the “U” position for codec µlaw operation (North American standard).
- Install jumper plug at J5 in the “A” position for codec A-law operation (European standard).
  Position “A” (A law) is the factory default setting for J5.

U2 PROM

The 2764 PROM in location U2 contains firmware appropriate to earth calling signal interface requirements.

4.2 LOOP CALLING

Jumper and Switch Locations

NOTE 1

No jumpers are installed at locations JX01 and JX02 (X = circuits 1 through 8) on ECT/LCT configured for loop calling.

NOTE 2

The Position 1 dip switch setting at SW1 determines whether the card uses disconnect clearing signal method or standard guarded clearing.

- Set the Position 1 dip switch at SW1 in the “OPEN” position for guarded clearing.
- Set the Position 1 dip switch at SW1 in the “CLSD” position for disconnect clearing.
  Position 1 “OPEN” (guarded clearing) is the factory default setting for SW1.

NOTE 3

- Install jumper plug at J5 in the “U” position for codec µlaw operation (North American standard).
- Install jumper plug at J5 in the “A” position for codec A-law operation (European standard).
  Position “A” (A law) is the factory default setting for J5.

U2 PROM

The 2764 PROM in location U2 contains firmware appropriate to loop calling signal interface requirements.

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the ECT/LCT, refer to the following publications:

- United Kingdom Supplement
- VCO/4K System Administrator's Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual

International E+M Trunk Card (E+M/DC5)

1.0 GENERAL

The E+M Trunk Card (E+M) is a standard VCO/4K port interface circuit card that can reside in any slot other than those reserved for the control system cards. It supports eight E+M trunk connections. Both 2-wire (2BS, 3BS OFTEL port type) and 4-wire (2CS, 3CS OFTEL port type) versions are available. Jumper options are provided for Type 1, 2, 4, and 5, trunk-side or signaling-side operation. For United Kingdom installations, only Type 5 configurations are permitted.

2.0 SPECIFICATIONS

Microprocessor: 8031 (12 MHz)

Memory: 8K Bytes EPROM
2K Bytes RAM

Power Requirements:	Typical
+5 Volts:	750 mA
+15 Volts:	130 mA
–15 Volts:	135 mA
+24 Volts:	96 mA

2-Wire Trunk Specifications

Input Level: –3 dB ± 0.5 dB
Output Level: –3 dB ± 0.5 dB

Crosstalk Attenuation: 68 dB minimum
Idle Circuit Noise: 23 dBrnc maximum
Echo Return Loss: 18 dB minimum
Line Impedance: BS6305: 1982 (Complex Termination)
Frequency Response:
(Signal levels relative to 1004 Hz with C Message Filter)

60 Hz:	–20 dB maximum
200 Hz:	–10 to 0.0 dB
300 Hz:	–6 to 0.0 dB
500 to 3000 Hz:	–2.5 to 1.5 dB
3200 Hz:	–1.5 to 1.5 dB
3400 Hz:	–3.0 to 0.0 dB

Longitudinal Balance: 200–4000 Hz 60 dB minimum

4-Wire Trunk Specifications

Input Level:	0 dB nominal	
Output Level:	0 dB nominal	
Crosstalk Attenuation:	Inter-channel	60 dB minimum
	Intra-channel	50 dB minimum

Idle Circuit Noise: 23 dBrnc maximum

Echo Return Loss: 18 dB minimum

Line Impedance: 600 ohms

Frequency Response:

(Signal levels relative to 1004 Hz with C Message Filter)

60 Hz:	–20 dB maximum
200 Hz:	–5.0 to 0.0 dB
300 to 3000 Hz:	–1.5 to 0.5 dB
3200 Hz:	–1.5 to 0.5 dB
3400 Hz:	–3.0 to 0.0 dB

Longitudinal Balance: 200–4000 Hz 60 dB minimum

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the E+M card. The four major elements of the E+M card are:

- Per port circuitry
- PCM timeslot bus interface
- Packet processor
- Control & status registers

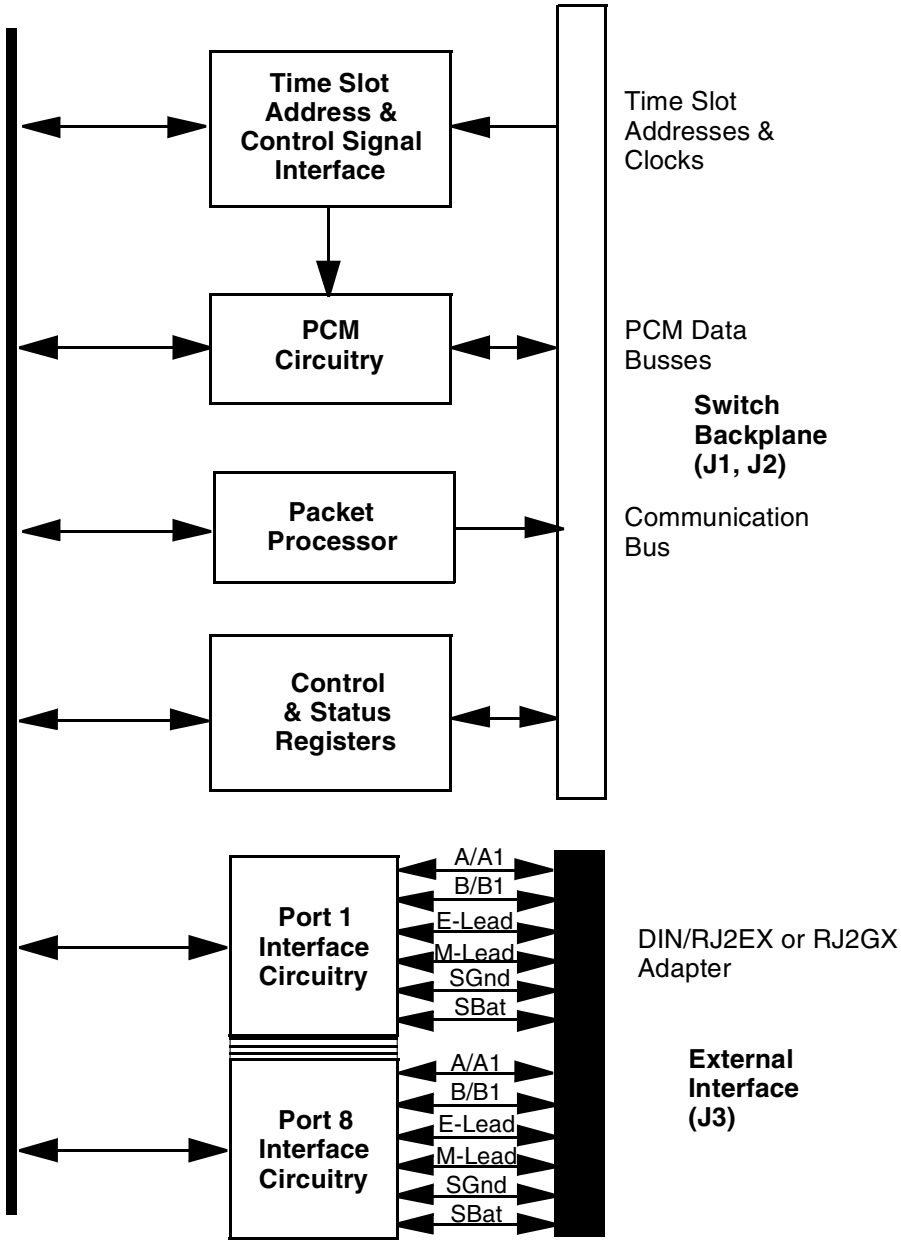


Figure 1: Block Diagram Of E+M Card

3.1 PER PORT CIRCUITRY

Each of the eight ports on a E+M card includes the following:

- Analog to digital encoding and decoding
- Jumper options for trunk or signaling side operation
- 2-wire or 4-wire voice trunks

Analog to Digital Encoding and Decoding

A 2913 codec provides digital-to-analog and analog-to-digital conversion. A dual-ported RAM interface performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between the PCM bus and the codec.

The codec operates at clock frequencies of 2.048 MHz and encodes and decodes A-law or µ-law PCM data.

Analog Interface

The analog interface consists of circuitry from the A and B leads to the codec. Protection diodes are connected across the secondary of transformers Tx01 and Tx02. Jumper areas Jx01, and Jx04 through Jx08 are provided for this configuration. E+M cards are factory configured for two-wire or four-wire operation with the appropriate resistor values and jumper settings. Configuration settings are given in *Section 4.0*.

E+M Signaling Interface

No signaling is performed on the voice path of the E+M trunks. Separate signaling leads, called the E and M leads, are provided for signaling purposes. Each E+M port has a signaling relay and a signaling detector. Types 1, 2, 4, and 5 electrical signaling is supported on the E+M card with either trunk or signaling side hardware configuration (see Figure 3 through Figure 5). Protection diodes are connected between the E lead and battery ground, and M lead and battery ground for lightning protection. Two 10 ohm, half-watt resistors are connected in series with the E and M leads to limit current.

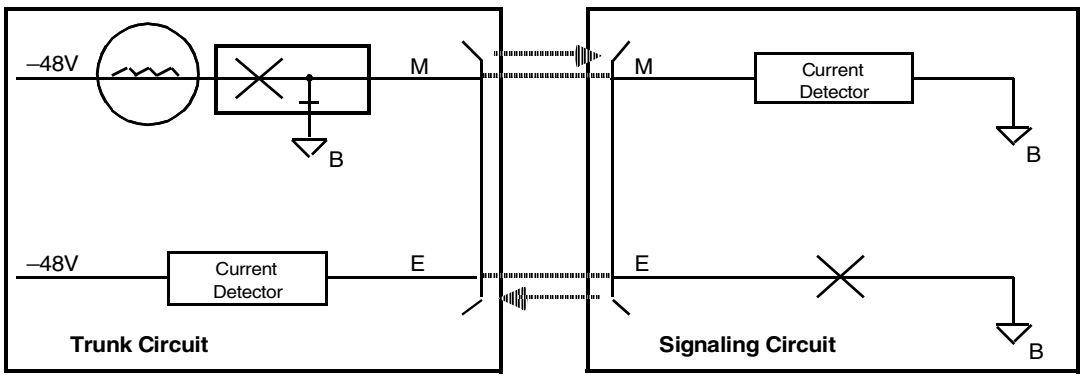


Figure 2: E+M Type I Interface

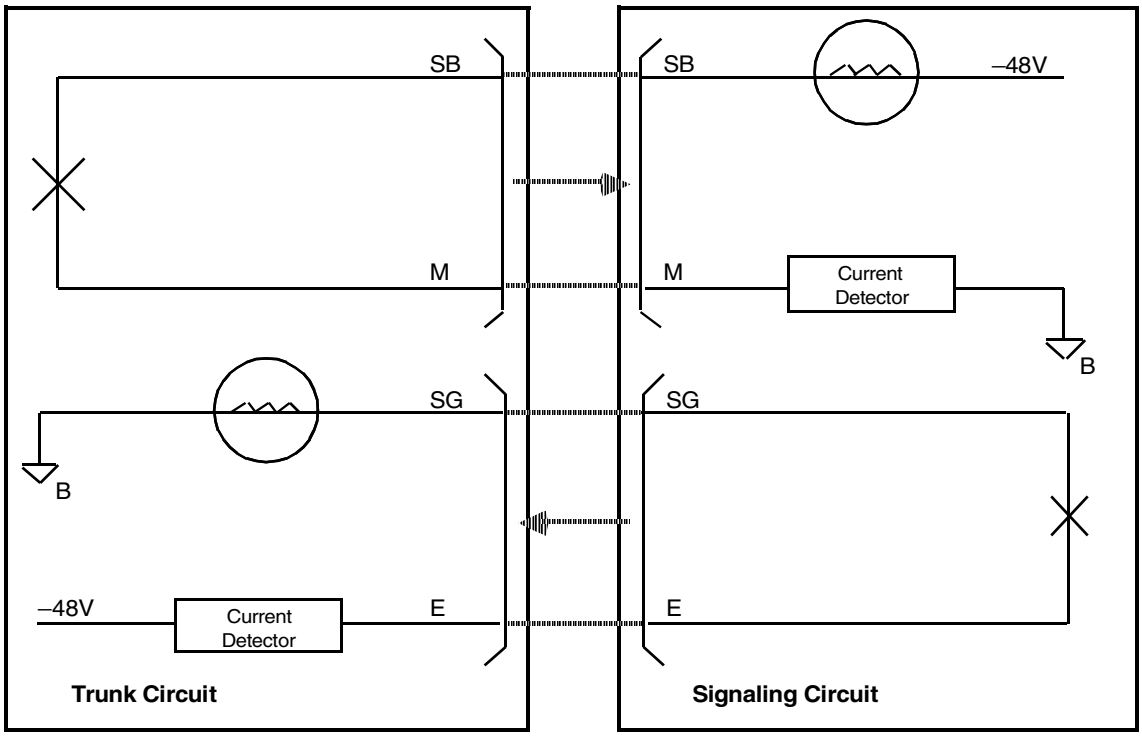


Figure 3: E+M Type II Interface

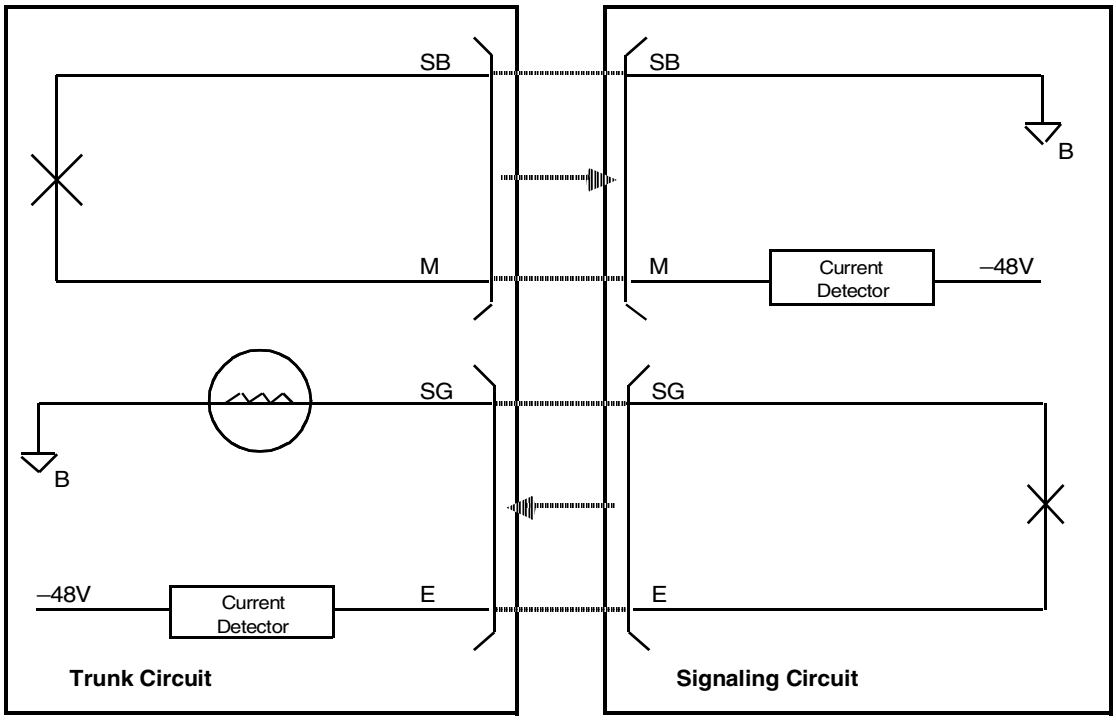


Figure 4: E+M Type IV Interface

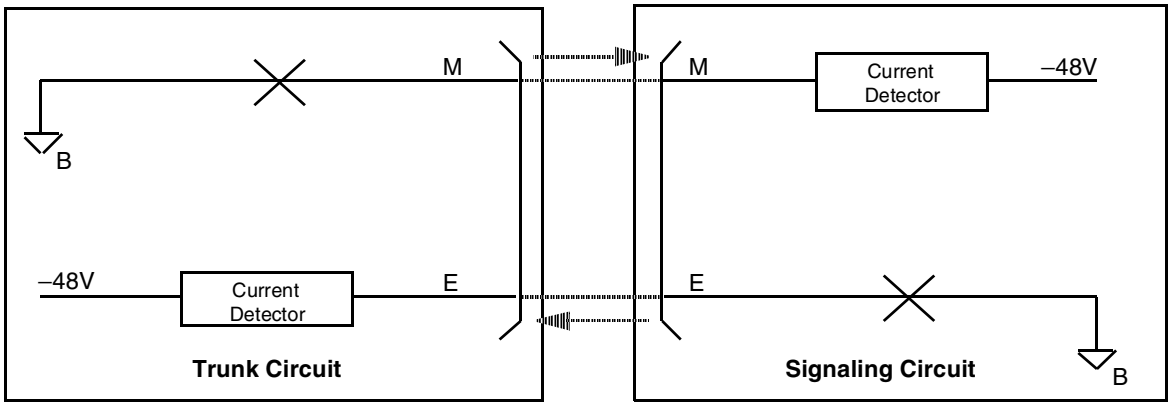


Figure 5: E+M Type V Interface

The trunk circuit asserts the M lead and the signaling circuit asserts the E lead using relay Kx01 (refer to *Section 4*). A thermistor is connected in series with the asserted signal lead to protect the interface if a signaling lead is improperly shorted.

A signaling lead detector is attached to the E lead in the trunk circuit and the M lead in the signaling circuit to detect when the far end of the trunk circuit asserts its signaling lead. The detector consists of an opto-isolator whose output goes low when detecting a signaling lead assertion.

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within the system is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the E+M card translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The E+M card interfaces to the PCM time slot busses with bus interface circuitry common to several VCO/4K port-oriented circuit cards. Each of the eight port interfaces on the E+M card can listen to any time slot on either PCM data bus.

An E+M card is automatically assigned a set of eight consecutive port addresses when it is entered into the database. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular E+M port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The E+M card contains an 8031-based packet processor that interfaces to the communication bus. All port interface cards and service circuit cards have a packet processor. The packet processor polls each of the eight trunk connections looking for an event (i.e. E+M signaling lead activity). When polled by the NBC/NBC-3, the packet processor reports any status change. The packet processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The packet processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The packet processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the communication bus interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the packet processor and, therefore, for the E+M card.

The communication bus is the path by which the packet processor receives commands from and sends status to the Network Bus Controller.

3.4 EXTERNAL INTERFACES

The connections to the Tip and Ring leads [2-wire (T, R) and 4-wire (T, R, T1, R1)] and the E+M signaling leads (E, M, SG, SB) of the eight trunk interfaces on the E+M card are made with the J3 connector.

An MDF I/O adapter terminates all voice and signaling leads to two 50-pin modular connectors (J1, J2), as shown in Figure 6.

CAUTION: Wiring must agree with your configuration requirements—Voice (2W-T, R or 4W-T, R, T1, R1) and Signaling (Type I, II, IV, V - trunk or signaling side)—as described in *Section 4.0*, *Configuration Notes*. Refer to *Table 1* for per port connections wired to connectors J1 and J2.

NOTE: Refer to the System Configuration Guide *for additional information on I/O module and the* Host Application Development Series: Supervision and Call Progress Tone Detection *module for an explanation of E+M signaling.*

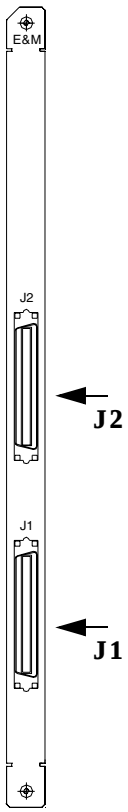


Figure 6: MDF I/O Adapter

Table 1: MDF I/O Adapter Pinouts

Port	2-wire/4-wire Voice Lead Connections	MDF-J1	MDF-J2	Type II, V/ I, IV Signaling Leads	MDF-J1	MDF-J2
	Pinout			Pinout		
1	T	N/A	16	E	N/A	14
	R		15	M		39
	T1		41	SG		13
	R1		40	SB		38
2	T	N/A	12	E	N/A	10
	R		11	M		35
	T1		37	SG		9
	R1		36	SB		34
3	T	N/A	8	E	N/A	6
	R		7	M		31
	T1		33	SG		5
	R1		32	SB		30
4	T	N/A	4	E	N/A	2
	R		3	M		27
	T1		29	SG		1
	R1		28	SB		26
5	T	16	N/A	E	14	N/A
	R	15		M	39	
	T1	41		SG	13	
	R1	40		SB	38	
6	T	12	N/A	E	10	N/A
	R	11		M	35	
	T1	37		SG	9	
	R1	36		SB	34	

Table 1: MDF I/O Adapter Pinouts (Continued)

Port	2-wire/4-wire Voice Lead Connections	MDF-J1	MDF-J2	Type II, V/ I, IV Signaling Leads	MDF-J1	MDF-J2
	Pinout			Pinout		
7	T	8	N/A	E	6	N/A
	R	7		M	31	
	T1	33		SG	5	
	R1	32		SB	30	
8	T	4	N/A	E	2	N/A
	R	3		M	27	
	T1	29		SG	1	
	R1	28		SB	26	

4.0 CONFIGURATION NOTES

The E+M is manufactured by Cisco Systems, Inc. Jumper plugs on the E+M are factory set for use in VCO/4K systems as Type 1 signaling side. Figure 7 shows the location of jumper plug areas on E+Ms based on the card's PCB revision level. Figure 8 shows the jumper plug settings specific to the type of E+M signaling employed on the card. Use this information to verify or reset jumpers on an interface card prior to installing it.

CAUTION: Jumpers associated with interface characteristics (2- or 4-wire) must be identically set for all eight circuits on the E+M card. Settings must correspond to the I/O module. Failure to set each circuit for identical operation results in cross-wiring problems at the I/O module.

NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card. The PCB may be etched with two to four characters indicating the revision level. Only the first two or three characters are important. In four-character revision level markings, the final letter is an R, which indicates that the PCB is at Release level. For example, a revision level C0Q card may be marked as Rev. CQ, C0Q or C0QR.

If a card is improperly configured, it may fail to perform its interface function between external trunks and the system. Great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port configuration refers to the process of specifying appropriate data for each port in the system database. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a E+M in the system's database, refer to the *System Administrator's Guide*.

JX01 and JX02 Jumper Locations

JX01 (14 pin head) and JX02 (15 pin head) jumpers are used to configure the ports for types 1, 2, 4, and 5 signaling protocols, as either Trunk or Signaling circuit types. Figure 8 illustrates the jumper configurations for each protocol and type.

> **CAUTION: Carefully examine and configure the JX01 and JX02 jumpers before you insert the E+M card into your system and apply power. The card circuitry could be damaged if the jumpers are not configured for the correct protocol and circuit type.**
>
> *NOTE: In the United Kingdom, JX01 and JX02 must be configured for Type 5 signaling.*

J5 Jumper Location

The J5 Jumper enables either µ-law (US) or A-law (Europe) PCM encoding formats.

- Place the jumper on pins 1 and 2 for codec µ-law operation (North American standard). Pins 1 and 2 are the closest pins to the LEDs.
- Place the jumper on pins 2 and 3 for codec A-law operation (European standard).

  NOTE: The factory default setting for J5 is pins 2 and 3 on and pin 3 off (A-law).

U2 PROM

The 2764 PROM in location U2 contains firmware appropriate to E+M signaling interface requirements.

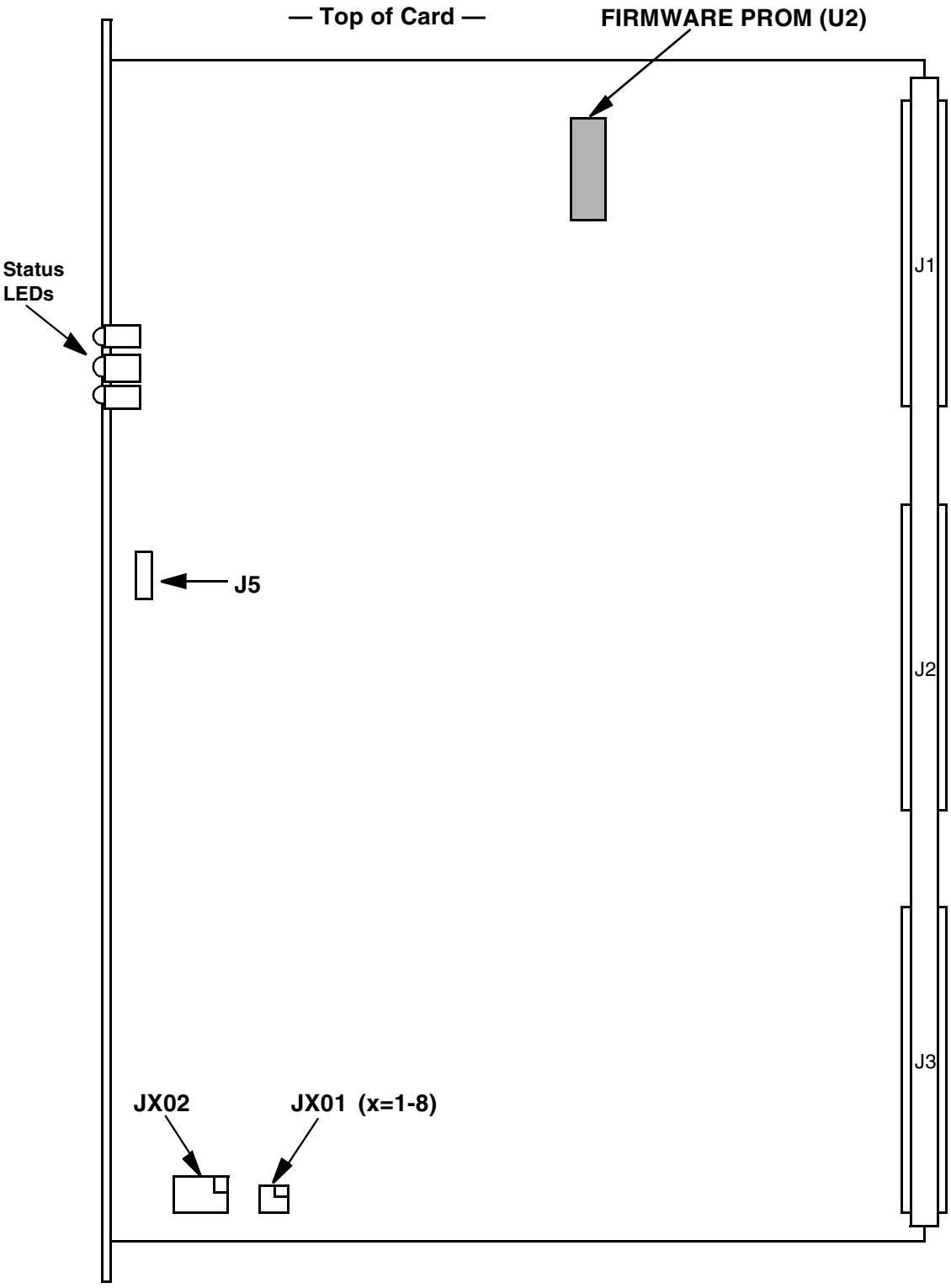


Figure 7: E+M JUMPER & PROM LOCATIONS

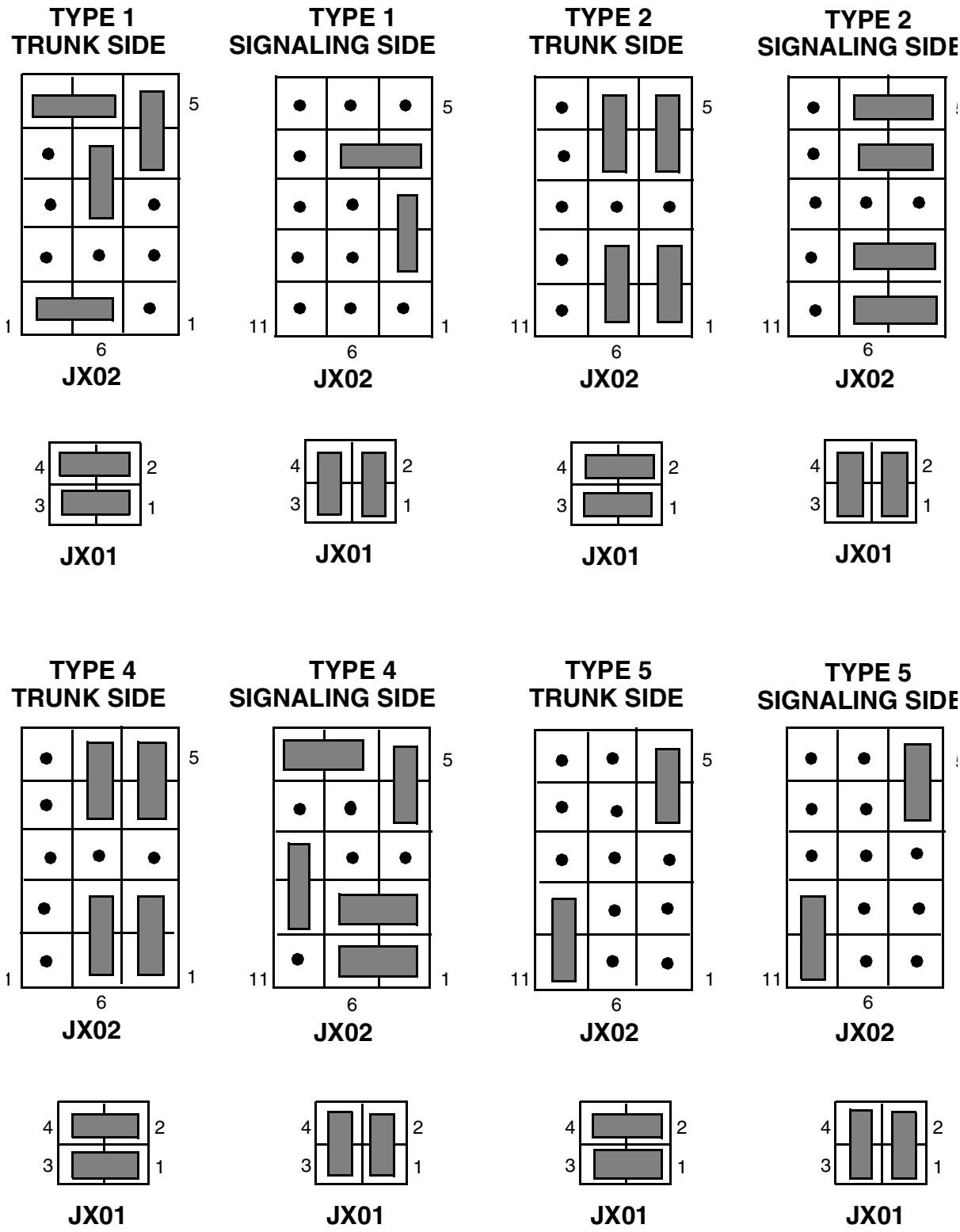


Figure 8: E+M Jumper Settings

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation, and maintenance of the E+M card, refer to the following publications:

- United Kingdom Supplement
- VCO/4K System Reference Guide
- VCO/4K System Administrator's Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual
- Technical Description: I/O Module

E1-Primary Rate Interface Card (E1-PRI)

1.0 GENERAL

The E1-Primary Rate Interface (E1-PRI) card is a standard port interface circuit card that can reside in any slot other than those reserved for the control system cards. The E1-PRI card supports 2.048 Mbps digital line transmission system connections between the system and an E-1 PRI. These connections provide:

- 30 x 64 kbs switchable *traffic channels* for both voice and data
- 1 x 64 kbs *synchronization channel* (time slot 0) for frame alignment
- 1 x 64 kbs *signaling channel* (time slot 16) for all signaling/maintenance information

This capability is the functional equivalent of North American ISDN Primary Rate Interface (PRI).

Electrical interface to the E1-PRI card complies with CCITT G.703 standards using the E1 I interface adapter. The 2.048Mbps data rate and common channel signaling comply with CCITT G.732 recommendations for PCM switching interfaces.

The E1-PRI is a platform for interfacing with DPNSS, DASS2-Network Termination, DASS2-Exchange Termination, and DSS1. Switches on the card can be set for the desired card type. There are separate download software packages available for each interface. These include: DPNSS, NT-DASS2, and ET-DASS2 download.

To use the E1-PRI interface, the system must be equipped with one of the optional software packages. Refer to the *DASS 2 , DPNSS, or ISDN Supplement* for more information about these software packages.

The E1-PRI card relies on system timing; timing can be synchronized to an internal reference clock, a selected E1 or E1-PRI span, or an external reference. The VCO/4K software allows administrators to designate primary and secondary master timing links to which the system is synchronized. If both links fail or the external reference signal is lost, the system defaults to its internal reference clock.

2.0 SPECIFICATIONS

Integrated Multi-Protocol (IMP) Processor:	
Microprocessor:	MC68302 (16 MHz)
Memory:	64K Bytes EPROM 256K Bytes SRAM
Power Requirements:	Typical
	+5 Volts: 1500mA
Input E1-PRI Stream Specifications:	
Format:	Common Channel Signaling (CCS) on Time Slot 16
	Frame Alignment Signaling on Time Slot 0
	Time Slots 1 – 15 and 17 – 31 switchable
Data Transparency:	HDB3
Frequency:	2.048 MHz ± 200 Hz
Impedance:	75 ohms ± 10 ohms 120 ohms ± 10 ohms
Output E1-PRI Stream Specifications:	
Format:	Common Channel Signaling (CCS) on Time Slot 16
	Frame Alignment Signaling on Time Slot 16
	Time Slots 1 – 15 and 17 – 31 switchable
Data Transparency:	HDB3
Frequency:	2.048 MHz ± 200 Hz
Impedance:	75 ohms ± 10 ohms 120 ohms ± 10 ohms

3.0 CIRCUIT DESCRIPTION

The E1-PRI card interfaces a VCO/4K system with a E1-PRI digital data carrier stream. The E1-PRI card transmits a 2.048 MHz, 32-channel (30 traffic channels, 1 synchronization channel and 1 signaling channel), bipolar digital data stream. The stream can be synchronized with the system clocks or loop timed. The E1-PRI card receives a data stream of frequency 2.048 MHz $\pm$200 Hz and can drive a reference clock onto the switch backplane which the NBC-3 uses as an input to its system synchronization circuitry.

The E1-PRI card detects loss of carrier errors, framing errors, and remote alarms on its incoming E1-PRI stream. It detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different, such as in loop timed configurations. The E1-PRI card contains elastic PCM data buffers to minimize slips caused by E1-PRI stream frequency jitter.

3.1 OVERVIEW OF CIRCUIT OPERATION

The E1-PRI card interfaces with a E1-PRI data stream. All internal operations are controlled by a intelligent processor downloaded with application software upon card power-up. All framing is synchronized to internal or external clock sources as selected in the system data base via the master timing link selection screen (refer to the *VCO/4K System Administrator's Guide* for more information.

Physical interface to the PCM stream is accomplished via an I/O module that mounts on the rear of the system. The module supports UG-1094 A/U type 75¾ unbalanced or 120¾ balanced coaxial connections.

Figure 1 is a simplified block diagram of the E1-PRI card.

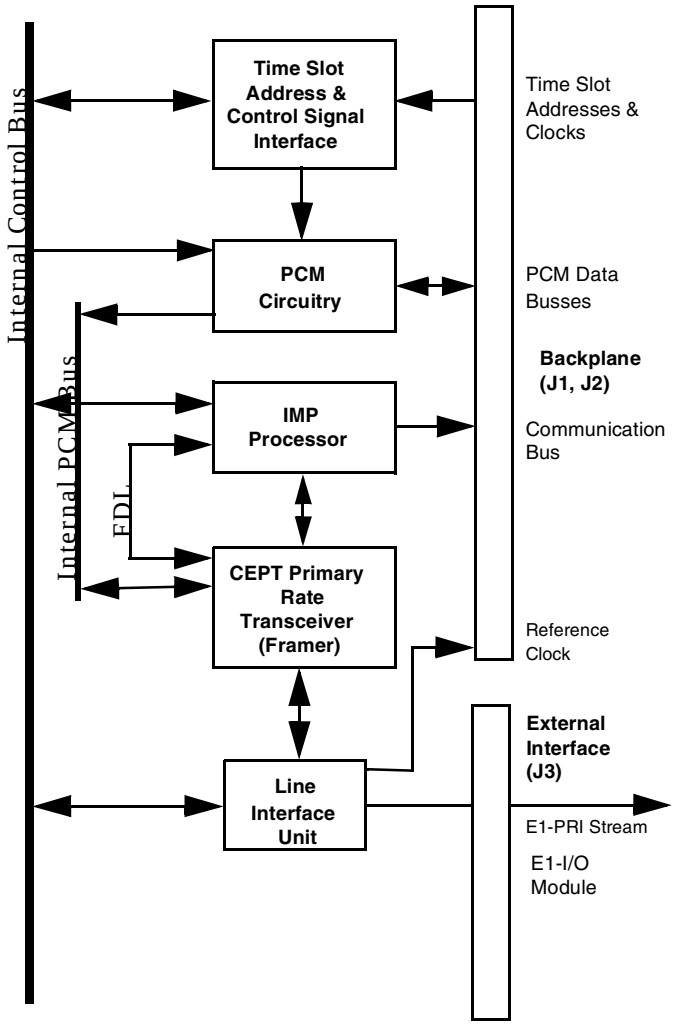


Figure 1: Block Diagram of E1-PRI Card

3.2 PHYSICAL INTERFACE

Physical interface with the E1-PRI stream is accomplished through a line interface unit (LIU) and a CEPT Primary Rate framer (transceiver). The link layer task controls and maintains the operation of the LIU and CEPT framer.

The LIU performs the following functions:

- Lightening and short circuit protection
- Clock recovery
- Jitter attenuation
- Bipolar to TTL conversion
- Wave shaping
- Line buildout selection
- Loopback and maintenance functions
- All ones (1s) generation

Common channel signaling is accomplished by using timeslot 16 as a dedicated signaling channel (D-Channel). This timeslot contains network and signaling informations about the other 30 traffic channels in the span.

CEPT Primary Rate transceiver functions are implemented under IMP control via the framer. The framer performs the following functions

- Alarm detection
- Alarm mode selection
- Channel separation
- FDL maintenance
- Microprocessor interface to Link Layer statistics
- Serial outputs of signaling channels and FDL
- Data transparency

Data Transparency is provided by the HDB3 (high density bipolar 3) method as specified in CCITT, G.703, Annex A for 2048Kbps operation.

3.3 IMP PROCESSOR

The IMP processor consists of an MC68302 Integrated Multi-Protocol (IMP) processor, memory and communication bus circuitry. The IMP controls Link Layer and framer tasks, and coordinates communications along the internal communication bus.

3.3.1 MC68302 PROCESSOR

The MC68302 integrates a closely coupled MC68000 microprocessor core with a flexible communications architecture. This processor supports concurrent operation of different protocols through a combination of architectural and programmable features.

A serial Communication Port (SCP) controls the operation of external Line Interface Unit and CEPT framer devices. Its three Serial Communications Controllers (SCCs) are used for signaling channel (HDLC, SCC1), Facility Data Link (HDLC, SCC2) and card front panel port (UART, SCC3) connections.

Configuration of OSI Layer 1 (Physical Layer), Layer 2 (Link Layer) and portions of Layer 3 (Network Layer) tasks are executed on the IMP Processor. Figure 2 shows the function/task assignments on E1-PRI cards.

3.3.2 MEMORY

The E1-PRI card includes 64 Kbytes of PROM. This nonvolatile memory holds boot firmware including card initialization and self-diagnostics.

The card also includes 256 Kbytes of 100 ns Static RAM (SRAM). Following power up, application software controlling OSI Layer 2 and Layer 3 is downloaded over the communication bus to SRAM. The IMP executes these programs from static memory.

3.3.3 SERIAL COMMUNICATION CONTROLLERS

SCC1 is configured as a full duplex HDLC (High Level Data Link Control) port for handling the common channel signaling data. Data is synchronously transmitted and clocked at an effective data rate of 64Kbps. The SCC1 transmitter is always enabled so as to keep the outbound data buffer loaded with signaling channel data or flag sequences. The receiver is always enabled and synchronized with a receive clock at 2.048Mbps. The receive clock is also gated to receive 8 bits of data from the signaling channel every 125µS for an effective data rate of 64Kbps.

SCC2 is configured as a full duplex HDLC port for handling the 4Kbps Facility Data Link (FDL) used for framing maintenance information.

SCC3 is configured as a half-duplex, 9600bps UART port connected to the front panel (J4) jack. It serves as an RS-232C diagnostic port.

NOTE: The front panel jack (J4) is not intended for customer use.

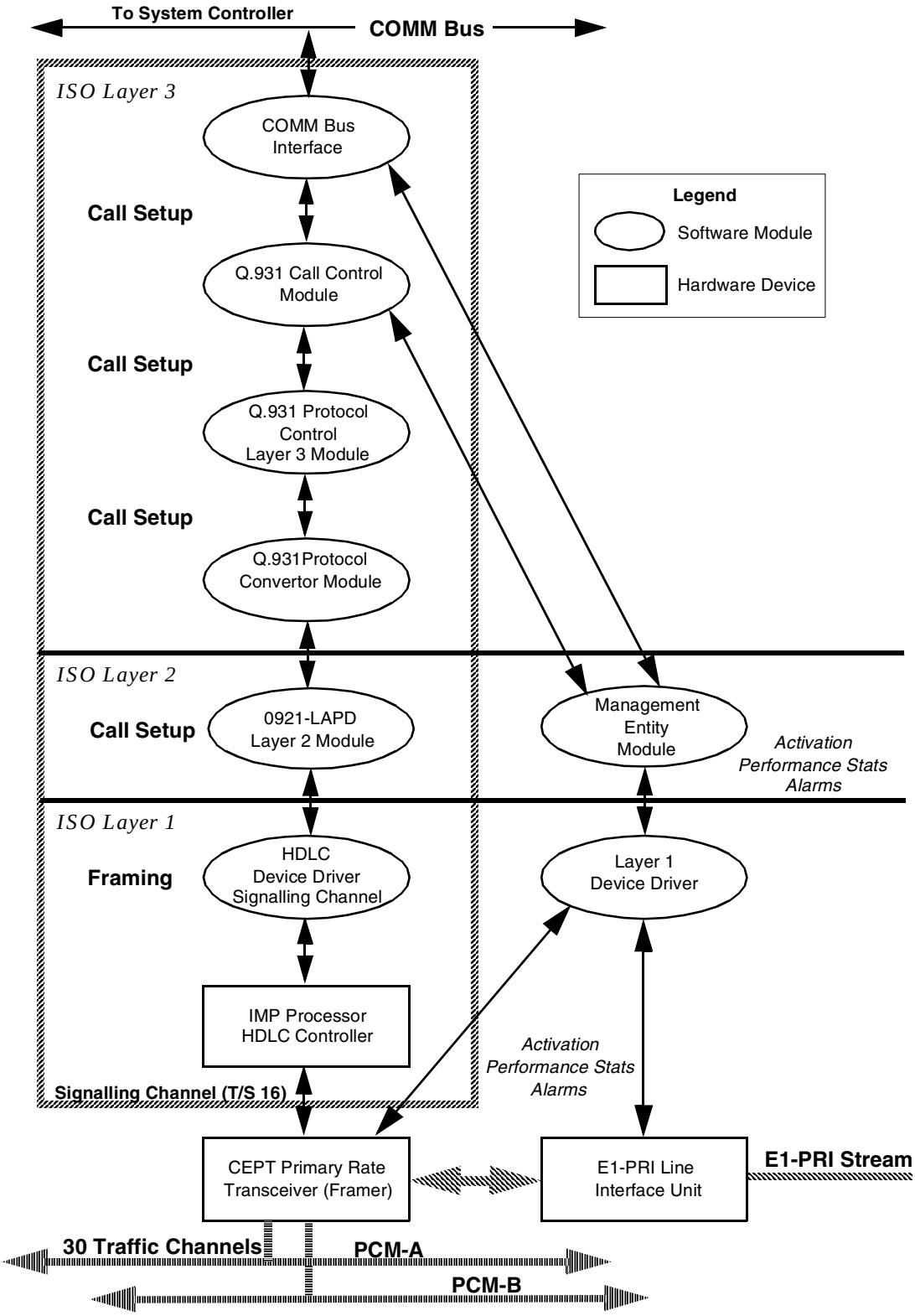


Figure 2: E1-PRI Card Hardware Devices & Software Modules

3.3.4 OSI LAYER 2 FUNCTIONS

The E1-PRI card utilizes one HDLC channel (SCC1) as the signaling channel. Signaling channel termination at Layer 2 requires implementation of Link Access Procedure – D-Channel Q.921, commonly referred to as LAPD. LAPD is downloaded to the E1-PRI card on power up/ card reset and run as a Link Layer task on the IMP processor.

LAP functions include:

- HDLC protocol communications
- Parameter negotiation
- Data link establishment
- Compelled frame transfer
- Error handling

3.3.5 OSI LAYER 3 FUNCTIONS

The signaling channel (D-Channel) termination at Layer 3 starts with a Q.931 converter task that translates the corresponding interface (DASS2, DPNSS, or DSS1) messages transmitted/received on the channel to their Q.931 equivalents. The Q.931 messages are passed through two modules, Protocol Control and Call Control, which perform the following functions:

- Data link establishment
- Call setup/teardown
- Call reference selection
- Application interface

Some call control tasks, such as traffic channel selection, are performed in the system controller. Messages received through Layer 3 are passed via the communication bus to higher layers implemented in the generic software and/or host application. Signaling and maintenance commands sent down from the system controller are transmitted over the communication bus and through Layer 3 and the lower layers for ultimate transmission on the D-Channel.

A management task runs parallel to the protocol tasks and collects link statistics. These statistics are sent via the communications bus for use by the generic software. The following statistics are monitored by the management task:

- Out-Of-Frame (OOFs) and slips
- Traffic channel in-service, out-of-service (OOS), and maintenance modes
- Signaling channel in-service and out-of-service modes
- Alarming (Yellow)

A multitasking executive acts as a scheduler for each of the tasks. It also provides the necessary mailbox interface for passing messages between different tasks.

3.4 CEPT PRIMARY RATE TRANSCEIVER (FRAMER)

The CEPT framer interfaces to an E1-PRI 2.048Mbps digital trunk through the LIU. It provides clear channel capability through appropriate zero suppression and signaling modes. System ones density is maintained through HDB3 (High Density Bipolar 3) coding. HDB3 coding is pseudo ternary with three states noted as B+, B_ and 0. Spaces in the binary signal are coded as spaces in the HDB3 signal. Violations of the rule for alternate mark inversion (AMI) are introduced when coding strings of four spaces.

The transmit framer/formatter circuits generate appropriate framing bits, supervise zero suppression, generate alarms and provide output clocks for data conditioning and decoding. The receiver/synchronizer circuits establish frame and multiframe boundaries, extract signaling data and report alarms and signaling formats.

3.5 LINE INTERFACE UNIT

The LIU employed on the E1-PRI card is a fully integrated transceiver designed for E1-PRI 2.048Mbps operation. It performs line driver, data recovery and clock recovery functions. The LIU supports full-duplex transmission of digital data over 75W unbalanced or 120W balanced installations in accordance with CCITT, G.703 interface specifications.

3.6 E1-PRI CARD LED STATES

Table 2 lists front panel LED states for E1-PRI cards and their meaning. Note that these states are unique to E1-PRI interface cards. The following general signaling conditions apply to each LED:

- *Red (top) LED* – illuminates continuously to signal a problem with an inward E1-PRI stream (carrier loss, OOF or signaling channel failure).
- *Yellow (center) LED* – illuminates to signal that a Yellow Alarm has been detected on the incoming E1-PRI stream (remote alarm), or that the card has not been polled for two seconds by the NBC-3.
- *Green (bottom) LED* – not used for alarming. Illuminates continuously until the base address of the card has been assigned by the system.

3.7 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 3 lists the pin assignments for J1 on the E1-PRI card.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.8 EXTERNAL INTERFACES

Connections to the incoming and outgoing E1-PRI digital data streams are made via the J3 connector. A VCO I/O module attaches to the J3 connector and allows external connection to the E1-PRI card via UG-1094 A/U type female coaxial connectors (one transmit + one receive connection per span). J3 connector pinouts are listed in Table 4. The J3 to coaxial connector pinouts are shown in Figure 3.

3.9 DIP SWITCH

Switch 7 and 8 of the eight-position DIP switch on the E1-PRI card is used to select the card's identity. Switch 6 is used to configure the card for NET5. The switch functions are listed in Table 1.

Table 1: E1-PRI Card Switch 6, 7 and 8 Functions

Type	SW6	SW 7	SW 8
DSS1	Open	Open	Open
NTDASS2	Open	Open	Closed
ETDASS2	Open	Closed	Open
DPNSS	Open	Closed	Closed
NET5	Closed	n/a	n/a

NOTE: The card defined in the system database must match the switch settings.

Table 2: E1-PRI Card LED States

PRI Card LEDs			System Alarm	Condition	Card State	Outward Action
Red	Yel	Grn				
OFF	OFF	OFF	None	Normal	Active	Call processing is occurring
OFF	ON	OFF	Minor (FRM286)	Remote Alarm	Maintenance	None
			Minor	COMM Bus Polling Failure	Normal	None
ON	OFF	OFF	Major (FRM285)	Loss of Carrier	Maintenance	Sending Yellow alarm
			Minor (FRM284)	OOF Error	Maintenance	Sending Yellow alarm
			None (FRM295)	D Channel Failure	Maintenance	None
			Major (FRM296)	T309 Timeout	Maintenance	None
ON	ON	OFF	Major	Following Card Reset	Maintenance	None
OFF	OFF	ON	Minor (FRM281)	Out-of-Service (OOS)	OOS	None

- If an Active E1-PRI card is placed into Maintenance via master console, any calls in progress are completed and no new calls are accepted. Calls are not torn down unless the individual port is taken out of service or there is a loss of carrier condition.
- If multiple conditions force a card into Maintenance state, the card is not activate until all error conditions are cleared.
- If the Manual Intervention for SLIP/OOFS flag is set to “N”, slips may be occurring even though the card is Active and no LEDS are illuminated. The maintenance threshold for OOFs is ignored and the E1-PRI card cycles in and out of Maintenance as the OOF condition is detected and cleared.
- Slip and OOF counters are automatically zeroed at midnight.

Table 3: E1-PRI Card J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND

Table 3: E1-PRI Card J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	–24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	Unused	Unused	Unused
30	AGND	Unused	AGND
31	AGND	Unused	AGND
32	DGND	Unused	DGND

Table 4: E1-PRI Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Digital Ground
2	Unused	Unused	Reserved
3	Unused	Unused	Rcv Line Tip [a]
4	Unused	Unused	Rcv Line Ring [a]
5	Unused	Unused	Xmt Line Tip [b]
6	Unused	Unused	Xmt Line Ring [b]
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Unused	Unused	Unused
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Unused	Unused	Unused
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Unused	Unused	Unused
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Unused	Unused	Unused
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Unused	Unused	Unused
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	GND

Table 4: E1-PRI Card J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
30	Unused	Unused	SCC3 UART Xmt
31	Unused	Unused	SCC3 UART Rcv
32	Unused	Unused	Unused

a. Signal to E1-PRI Card.

b. Signal from E1-PRI Card.

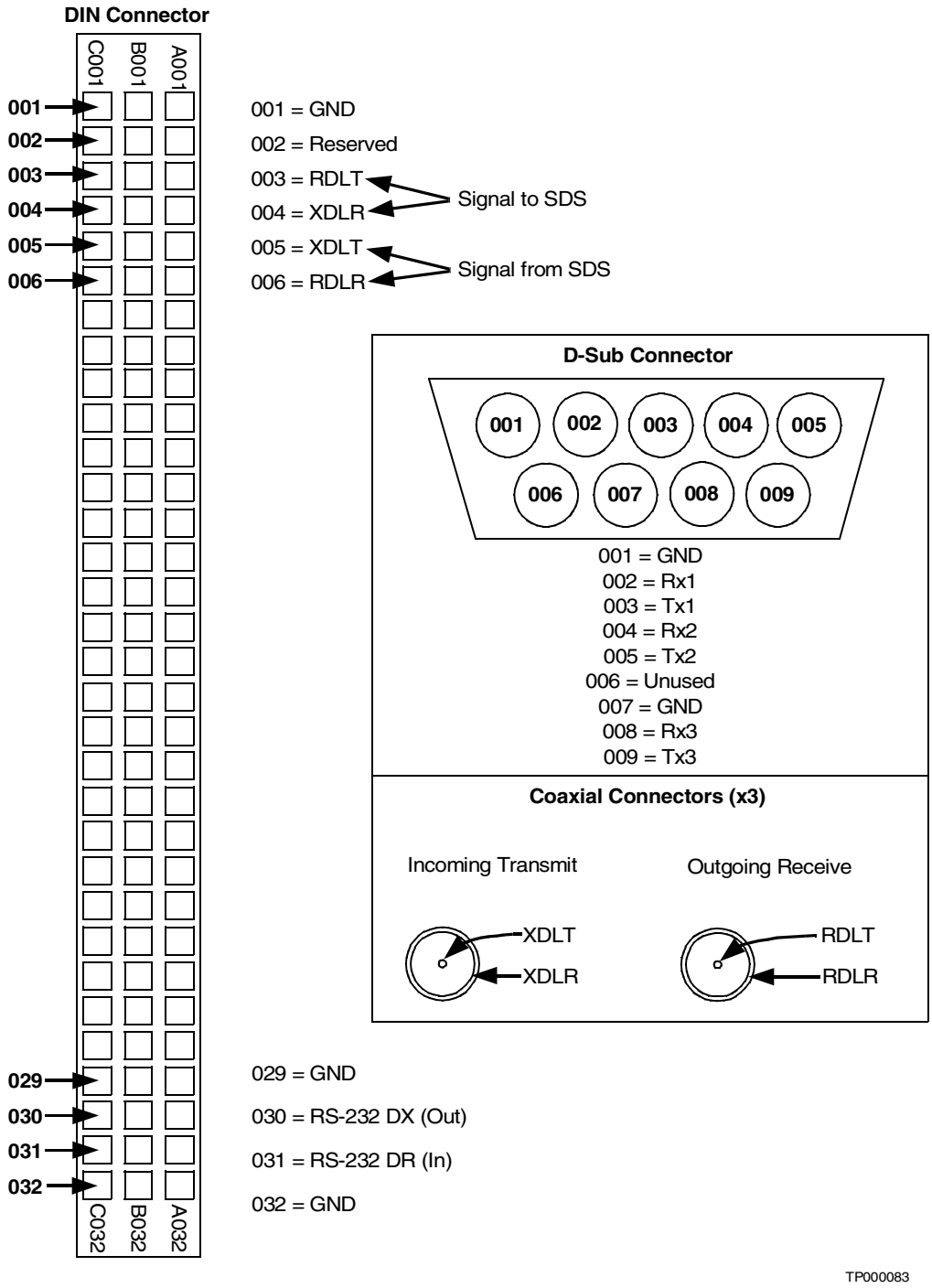


Figure 3: Pinout Diagram of E1/E1-PRI Adapters

4.0 CONFIGURATION NOTES

The E1-PRI card is manufactured by Cisco Systems, Inc. Figure 5 indicates the location of factory set jumpers. Refer to the jumper settings shown below and Figure 5 to verify configuration jumper settings prior to installing the E1-PRI card.

> *NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.*

If a card is improperly configured, it may fail to perform its interface function between external spans and the system. Therefore, great care must be taken to verify configuration settings, hardware jumpers and data base entries, before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base, including line equalization. If the port is improperly configured, the system may improperly interpret the incoming E1-PRI stream. For additional information on configuring a E1-PRI card in the system data base, refer to the *DASS 2, DPNSS, or ISDN Supplement*.

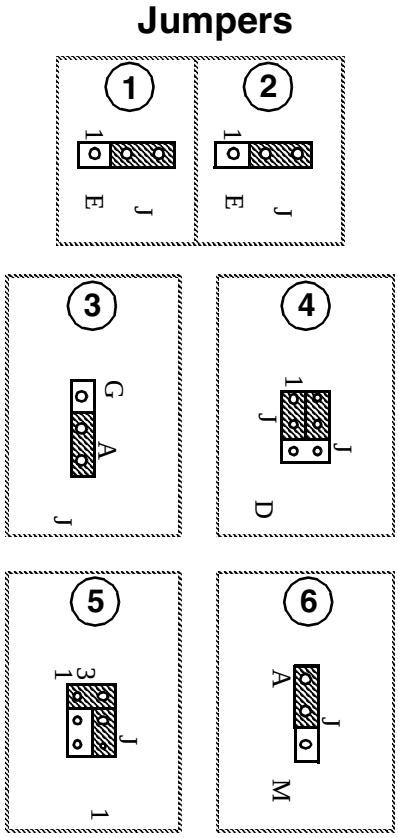


Figure 4: E1-PRI Card Jumper and PROM Listings

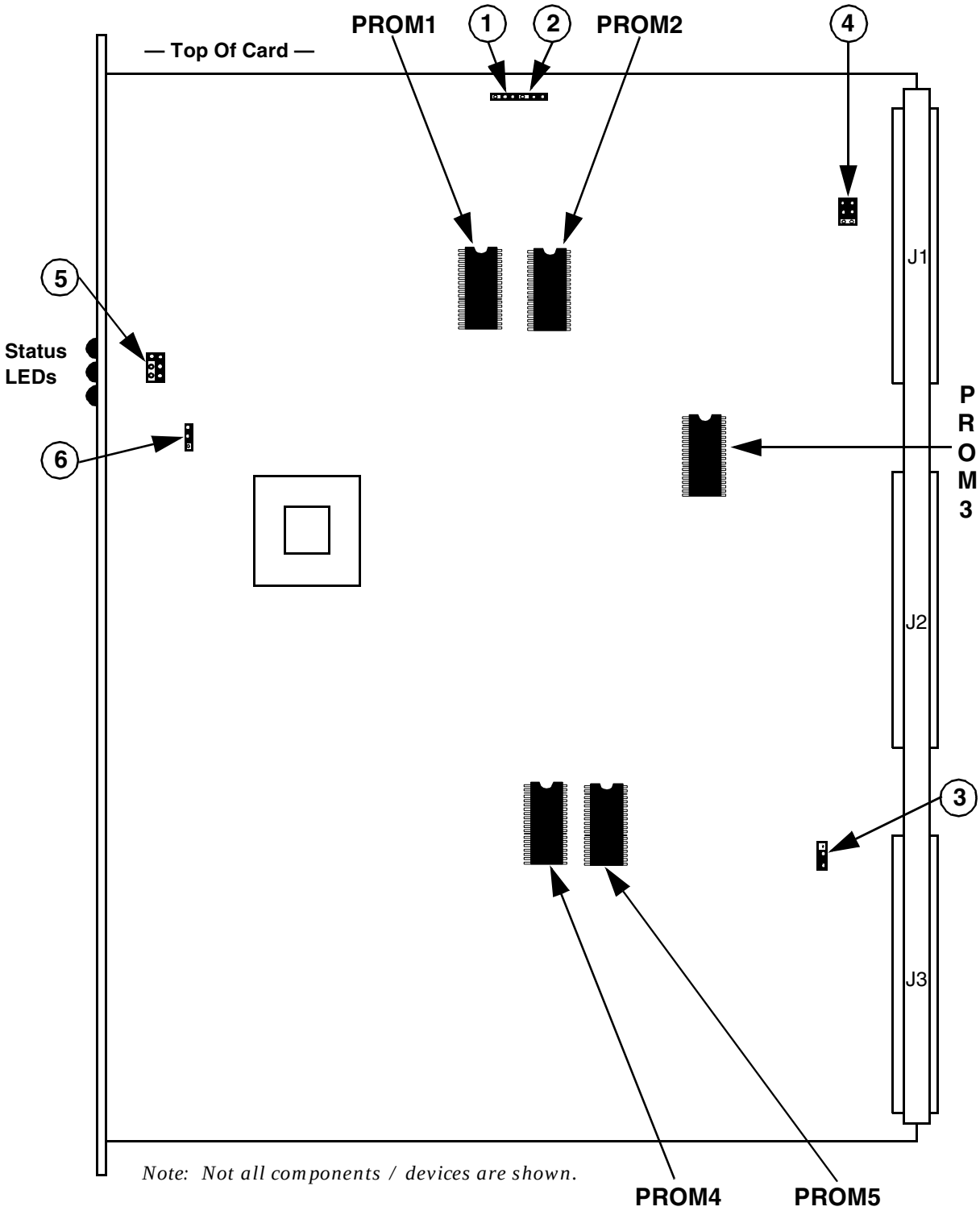


Figure 5: E1-PRI Card Jumper/PROM Locations

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the E1-PRI card, refer to the following publications:

- DASS2 Supplement
- VCO/4KSystem Administrator's Guide
- United Kingdom Supplement
- VCO/4K Installation Manual
- DPNSS Supplement
- VCO/4K ISDN Supplement

Four Span Programmable E1 Interface Card (4xE1)

1.0 GENERAL

The Four Span Programmable E1 Interface card is a standard port interface circuit card that can reside in any slot other than those reserved for the control system cards. It supports four spans of thirtytwo 64 Kbps voice and data channels, and complies with CCITT G.704 specifications for transmission at 2.048 Mbps. You can assign incoming, outgoing, and two-way service to 32 individual non-blocking channels on a span.

1.1 TIMING

You can synchronize system timing to an internal source (the NBC-3), an external clock (a clock cabled directly into the front of the NBC-3 card), or a designated incoming span. If you choose to synchronize to an incoming span, you can designate a primary and secondary timing link (incoming span). Refer to the *System Administrator's Guide* for information on the system administration screens used to synchronize timing.

If an external timing source fails, the system defaults to the internal source (NBC-3).

If the primary timing source fails, and secondary source is stable, the system defaults directly to the secondary source. In some cases, the system may temporarily default to the internal source (NBC-3) until it checks for, and detects the secondary source. When the secondary source is detected, the system then defaults to the secondary source.

2.0 SPECIFICATIONS

Microprocessor:	(4) MC68302 (1) MC68340
Memory:	256K per processor SRAM 64K/68302 EPROM 128K/68340 EPROM
Power Requirements:	17.5 Watts @ 5VDC
Input E1 Stream:	
Format:	CAS
Data Encoding:	Alternate Mark Inversion (AMI)
Data Transparency:	HDB3
Frequency:	2.048 MHz ± 100 Hz
Impedance:	75 ohms ± 7.5 ohms 120 ohms ± 12 ohms
Output E1 Stream:	
Format:	CAS
Frequency:	2.048 MHz ± 100 Hz
Impedance:	75 ohms ± 7.5 ohms 120 ohms ± 12 ohms
Drive Capability:	CCITT Recommendation G.703 for 75-ohm coax CCITT Recommendation G.703 for 120-ohm twisted pair

3.0 PROGRAMMABILITY

The application software is downloaded to each span controller, enabling independent provisioning of each span as well as each channel. For more information about provisioning spans or channels, refer to the *System Administrator's Guide.*

4.0 CIRCUIT DESCRIPTION

The Four Span E1 card has duplicate circuitry for each of the spans and the common interface to the system backplane, which includes an MC68340 communication controller.

Each span circuit consists of an MC68302 span controller, a framer, and a Line Interface Unit (LIU). The system controller passes internal commands to each span controller, which provisions the framer and LIU. The span controller monitors the framer and LIU for alarms or signaling transitions and reports these events back to the system controller.

The LIU terminates the E1 stream and passes it to the framer. Channel information is passed onto the PCM circuitry.

The system controller sets up and tears down circuit paths through the high-speed serial bus.

Figure 1 is a simplified block diagram of the Four Span E1 card. The components of the card are discussed in the following subsections.

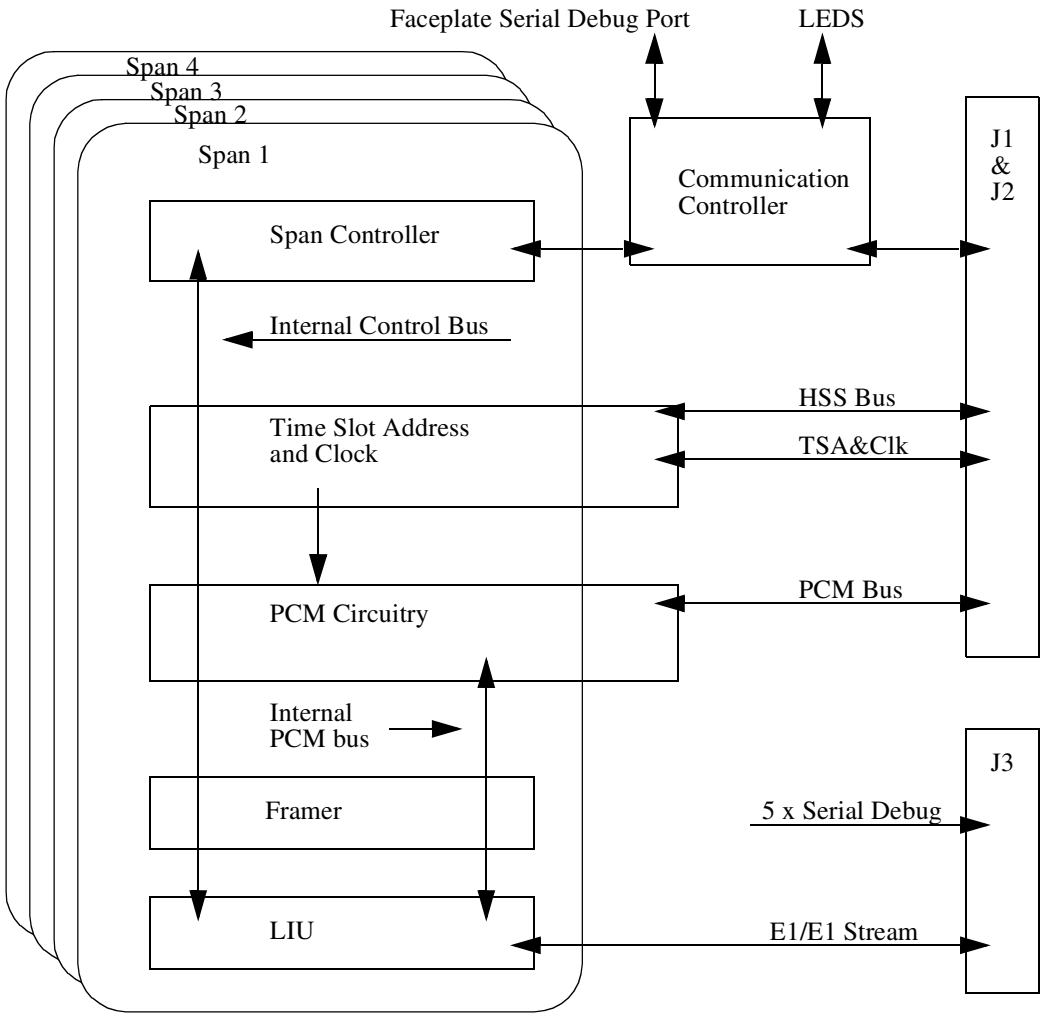


Figure 1: Block Diagram of the Four Span E1 Card

4.1 SHARED CIRCUITRY

The Four Span E1 card includes the following shared circuitry:

- Clock drivers
- PCM drivers
- Base address definition

4.2 INDIVIDUAL SPAN CIRCUITRY

The Four Span E1 card transmits and receives through four 2.048 MHz, 32-channel, bipolar E1 digital data streams. The J3 connector and a compliant connector configuration (BNC type) on the back of the system interfaces with the E1 stream. You can synchronize the NBC-3 with the receive clock. The Line Interface Unit (LIU) and the E1 framer provides electronically compliant signal levels.

The Four Span E1 card detects loss-of-carrier errors, framing errors, slips, and remote alarms on its incoming E1 stream. Send and receive slips occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus. The Four Span E1 card contains an elastic PCM data buffer to minimize slips caused by any Four Span E1 stream frequency jitter.

4.2.1 INTERNAL CONTROL BUS

The Span controller has a full functional memory mapped interface to the Framer and LIU. It also has a memory mapped interface to the Base Address Time Slot and Clock circuitry with which it sets the base address and chooses the system reference clock.

The PCM circuit interrupts the span controller on receive and transmit slip events.

4.2.2 FRAMER (PER SPAN)

The DS2143 framer interfaces to a Four Span E1, 2.048Mbps digital trunk through the LIU. The framer performs

- Alarm detection (Remote, All 1s, Carrier Lost, Loss of Sync)
- Alarm injection (Remote and All 1s alarms)
- Error counting (CRC4, frame events)
- Channel separation
- G703 framing and out-of-band channel associated signaling
- Out-of-band CAS signaling (A, B, C & D)
- Data transparency
- AMI, HDB3, data encoding

  NOTE: You can use HDB3 for E1 to maintain (1s) density (and timing) while providing data transparency.

4.2.3 LIU (PER SPAN)

The LIU on the Four Span E1 card (CS61575 or LXT305A) is a fully integrated transceiver designed for 1.544/2.048Mbps operation. The LIU supports full-duplex transmission of digital data over a 75 ohm (E1) balanced installation. A 120 Ω interface is also available. The LIU supports Stratum 4 clocking and also requires a transmit clock of 2.048 MHz ±100 Hz to maintain clock integrity (and therefore data integrity, i.e., 0 bit errors). The LIU performs

- Bipolar-to-TTL conversion on the transmit side
- Electrical wave shaping on the receive side
- Clock recovery
- Jitter attenuation—CCITT O.171
- Loopback and maintenance functions
- All 1s generation
- Signal monitoring (for loss of signal and quality transmission)

5.0 LED STATES

LED indicators appear on the front panel of the Four Span E1 card.

Table 1 lists the LED states on the Four Span E1 card.

Table 1: LED States on the Four Span T1 Care

Card Status	Controller	Green	Yellow	Red
Card Plugged In	68340	On	On	On
Self Test	68340	On	Blinking	Off
Receiving Download	68340	Blinking	Off	Off
Card Failure	68340	On	Off	On
Card OOS[a,b]	1) All	On	Off	Off
Major Alarm Table[a]	2) All	Off	Off	On
Minor Alarm[a]	3) All	Off	On	Off
Card Active	4) All	Off	Off	Off

a. If one span is OOS and another span has a major alarm, the OOS status takes precedence and the green LED illuminates.

b. If the span status is diagnostics, remote, or payload, the green LED is illuminated.

6.0 PIN ASSIGNMENTS

Table 2 lists the J1 pin assignments on the Four Span E1 card.

Table 2: J1 Pin Assignments on the Four Span E1 Card

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	-24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	Unused	Unused	Unused
30	AGND	Unused	AGND
31	AGND	Unused	AGND
32	DGND	Unused	DGND

Table 3 lists the J3 pin assignments on the Four Span E1 card.

Table 3: J3 Pin Assignments on the Four Span E1 Card

Pin	Row A	Row B	Row C
1	RX_RS232_340	Unused	TX_RS232_340
2	DGND	Unused	DGND
3	RX_RS232_302_1	Unused	TX_RS232_302_1
4	DGND	Unused	DGND
5	RX_RS232_302_2	Unused	TX_RS232_302_2
6	DGND	Unused	DGND
7	RX_RS232_302_3	Unused	TX_RS232_302_3
8	DGND	Unused	DGND
9	RX_RS232_302_4	Unused	TX_RS232_302_4
10	DGND	Unused	DGND
11	Reserved	Unused	Reserved
12	Reserved	Unused	Reserved
13	Reserved	Unused	Reserved
14	Reserved	Unused	Reserved
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Unused	Unused	Unused
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Rx Line Ring Span 1[a]	Unused	Tx Line Ring Span 1[b]
23	Rcv Line Tip Span 1[a]	Unused	Tx Line Tip Span 1[b]
24	Unused	Unused	Unused
25	Rx Line Ring Span 2[a]	Unused	Tx Line Ring Span 2[b]
26	Rcv Line Tip Span 2[a]	Unused	Tx Line Tip Span 2[b]
27	Unused	Unused	Unused
28	Rx Line Ring Span 3[a]	Unused	Tx Line Ring Span 3[b]
29	Rcv Line Tip Span 3[a]	Unused	Tx Line Tip Span 3[b]
30	Unused	Unused	Unused
31	Rx Line Ring Span 4[a]	Unused	Tx Line Ring Span 4[b]
32	Rcv Line Tip Span 4[a]	Unused	Tx Line Tip Span 4[b]

a. Signal to Four Span E1 Card

b. Signal from Four Span E1 Card

7.0 CONFIGURATION NOTES

The following subsections include configuration information for the E1 card, I/O modules for VCO/4K systems, and the jumper positions on the Four Span E1 card.

7.1 PLUG-IN ADAPTER

7.1.1 VCO/4K SYSTEMS

For VCO/4K systems, the following I/O modules are available:

- BNC for 75 ohm 4 span E1
- DB15/RJ45 for the 120 ohm 4 span E1

For more information about I/O modules for VCO/4K systems refer to the VCO/4K *I/O Modules Technical Description*.

The layout of the Four Span E1 card is shown in Figure 2.

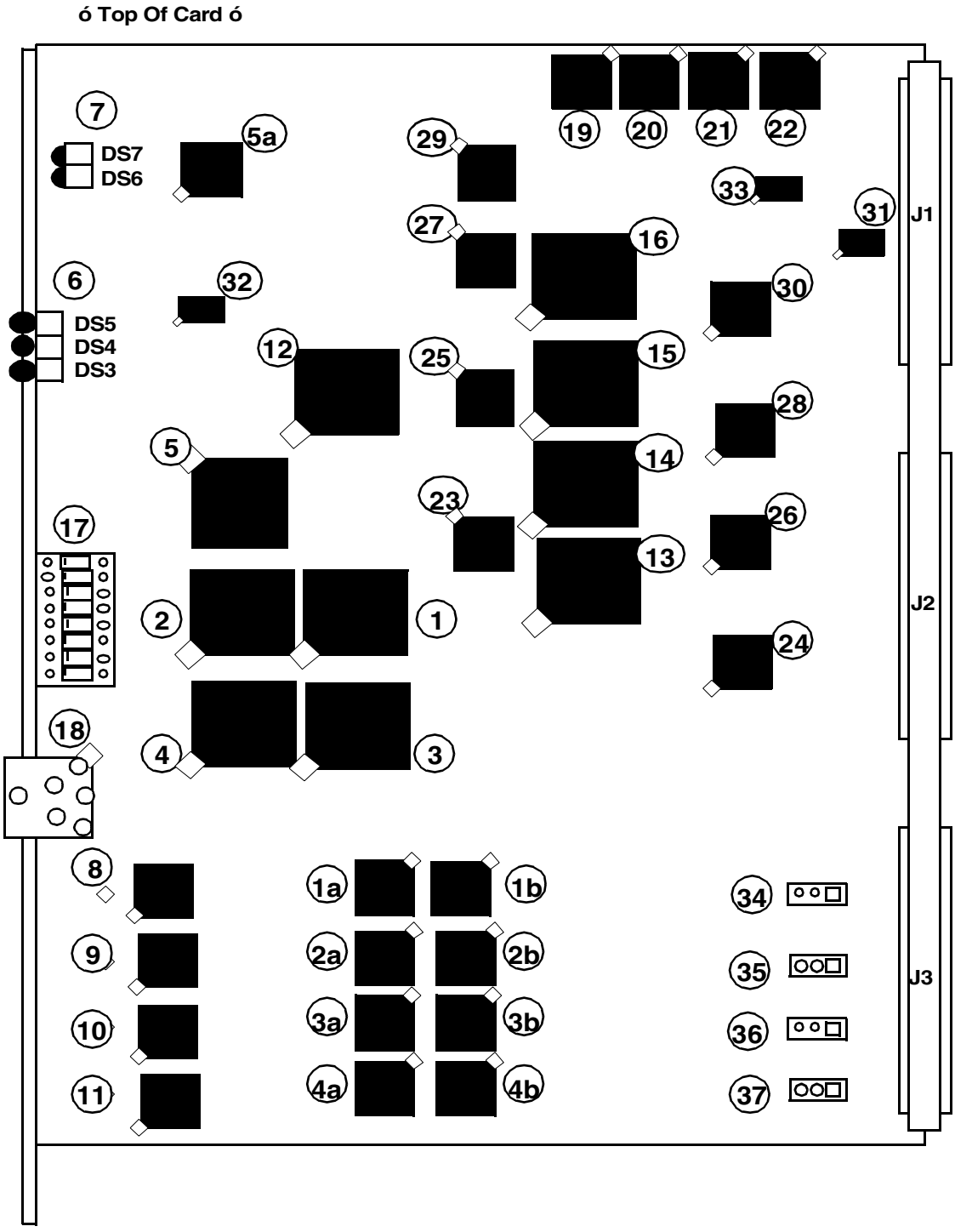


Figure 2: Four Span E1 interface Board Layout

NOTE: Not all components/devices are shown.

Table 4 lists the callouts in Figure 2.

Table 4: Four Span E1 Interface Board Callouts

Callout	Meaning
1	MC68302 Span 1 (U65)
1a	MC68302 Span 1 Even PROM (U48)
1b	MC68302 Span 1 Odd PROM (U49)
2	MC68302 Span 2 (U111)
2a	MC68302 Span 2 Even PROM (U94)
2b	MC68302 Span 2 Odd PROM (U93)
3	MC68302 Span 3 (U200)
3a	MC68302 Span 3 Even PROM (U186)
3b	MC68302 Span 3 Odd PROM (U185
4	MC68302 Span 4 (U155)
4a	MC68302 Span 4 Even PROM (U151)
4b	MC68302 Span 4 Odd PROM (U150)
5	MC68302 (U1)
5a	MC68302 PROM (U10)
6	Front Panel LEDs (D3-5)
7	MC68302 Status LEDs (D6, 7)
8	Span 1 FRAMER-INT PLD (LP92, U44)
9	Span 2 FRAMER-INT PLD (LP92, U91)
10	Span 3 FRAMER-INT PLD (LP92, U183)
11	Span 4 FRAMER-INT PLD (LP92, U135)
12	1XE1PCM PLD (LP96, U211)
13	SPAN 1 4XE1PCM PLD (LP95, UU43)
14	SPAN 2 4XE1PCM PLD (LP95, UU90)
15	SPAN 3 4XE1PCM PLD (LP95, UU182)
16	SPAN 4 4XE1PCM PLD (LP95, UU134)
17	8-Position Switch (S1)
18	Front Panel Diag Port (5V RS232)
19	Span 3 Path Setup PROM (U178)

Table 4: Four Span E1 Interface Board Callouts (Continued)

Callout	Meaning
20	Span 1 Path Setup PROM (U35)
21	Span 2 Path Setup PROM (U86)
22	Span 4 Path Setup PROM (U116)
23	Span 1 RX Gain/Law PROM (U28)
24	Span 1 TX Gain/Law PROM (U25
25	Span 2 RX Gain/Law PROM (U67)
26	Span 2 TX Gain/Law PROM (U78)
27	Span 3 RX Gain/Law PROM (U158)
28	Span 3 TX Gain/Law PROM (U170)
29	Span 4 RX Gain/Law PROM (U120)
30	Span 4 TX Gain/Law PROM (U131)
31	Comm Bus PLD (LP94, U14)
32	Virt Comm Bus PLD (LP93, U8)
33	Base Address PLD (LP89, U219)
34	Span 1 Transmit Line Match Selector JP1
35	Span 2 Transmit Line Match Selector JP2
36	Span 3 Transmit Line Match Selector JP4
37	Span 4 Transmit Line Match Selector JP3

7.2 JUMPER POSITIONS

The following subsection includes configuration information for jumper positions JP1 through JP4 on the Four Span E1 card. For the location of these jumpers, refer to callouts 34 through 37 in Figure 2.

7.2.1 75/120 OHM E1 LINE INTERFACE SELECTION

Pin settings in jumpers JP1 through JP4 are set for the 75 ¾ or the 120 ¾ interface.

> *NOTE: The 75 ohm card is the standard Four Span E1 card. The 120 ohm card can be ordered; P/N 50234050300 . The 75 ohm card should not be configured for 120 ohm, and the 120 ohm card should not be configured for 75 ohm.*

Figure 3 shows the correct pin settings for the JP1 through JP4 jumpers.

Interface	Pin Setting
75 ohm	2 and 3
120 ohm	1 and 2

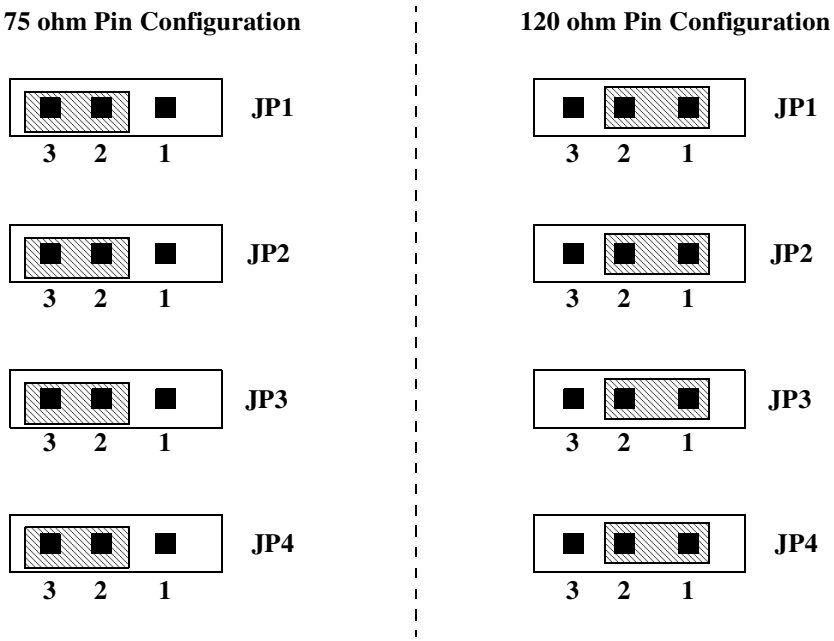


Figure 3: JP1 through JP4 Jumper Positions

7.2.2 EIGHT POSITION DIP SWITCH FOR LAW SETTINGS

An 8-position dip switch (S1) provides law configuration on a per span basis. Table 5 lists the A- and MU-law settings for S1. For information about the S1 dipswitch location, see callout 17 in Figure 2. Verify that Switch S1 positions 1 through 4 are set to the A law default.

Table 5: Law Settings

Switch Setting	MU law	A law
One	Open	Closed
Two	Open	Closed
Three	Open	Closed
Four	Open	Closed

NOTE: Switch selections 5 through 8 are not used.

The on-board switches match the PCM law of the VCO/4K switch. To provision the PCM law of the E1 stream, refer to the VCO/4K System Administrator's Guide.

Figure 4 shows an S1 switch configured for Mu-Law. The shaded areas signify that the switch is pushed in.

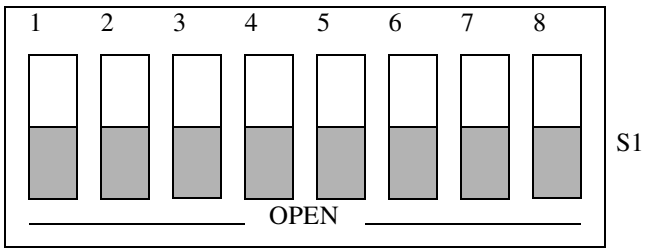


Figure 4: S1 A/MU Law Configuration Switch

Interface Controller Card E1 I/O Module

1.0 GENERAL

The VCO/4K System uses active I/O modules in conjunction with the ICC card to connect to the network. Each I/O Module uses one slot on the backplane and supports one ICC card. The I/O Module is located at the back of the switch and must be aligned with the ICC card. A block diagram for the ICC I/O Module is shown at the bottom of Figure 1.

The E1 I/O Module is a specialized backplane card that provides E1 network connection to the ICC card. It is available in three configurations supporting 4, 8, or 16 E1 spans. The ICC card is inserted in the VCO/4K switch from the front of the system. The I/O Module, inserted at the rear of the system (before ICC insertion), aligns with each ICC card.

The E1 I/O module supports a 120-ohm network interface for E1 and includes active circuitry such as E1 framers.

> *NOTE: The E1 I/O Module also supports a 75-ohm network interface when optional Balun impedance matching devices are used.*

For information on the ICC card, refer to the Interface Controller Card (ICC) technical description.

2.0 SPECIFICATIONS

2.1 COMPLIANCE WITH STANDARDS

The ICC I/O Module is in compliance with all applicable U.S. and international standards. See Table 1.

Table 1: Standards Compliance

Category	Standard
Safety	EN-60950 IEC-950
Jitter	ITU G.823
EMI/EMC	EN55022 (Europe) EN50082-1 (Europe)
PCB Manufacture	IPC
Clocking/Framing	ITU G.703 ITU G.704
Lightning/Power Cross	EN-60950 IEC-950
Telecom	European country-specific

2.2 I/O MODULE SPECIFICATIONS

Power Requirements (Maximum)	5 Volts (from the ICC card)
	4 Span E1 – 1.16 A
	8 Span E1 – 1.42 A
	16 Span E1 – 1.95 A

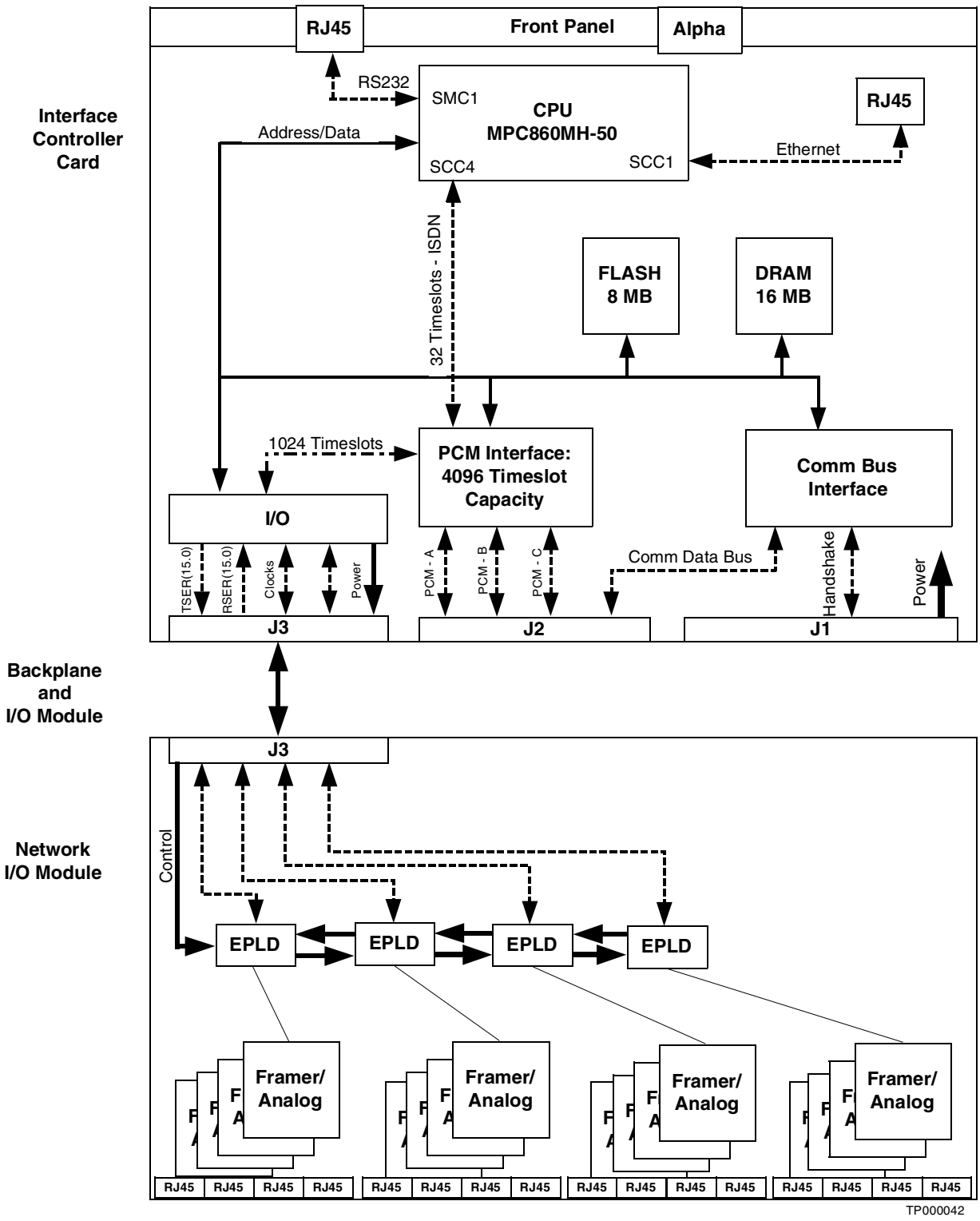
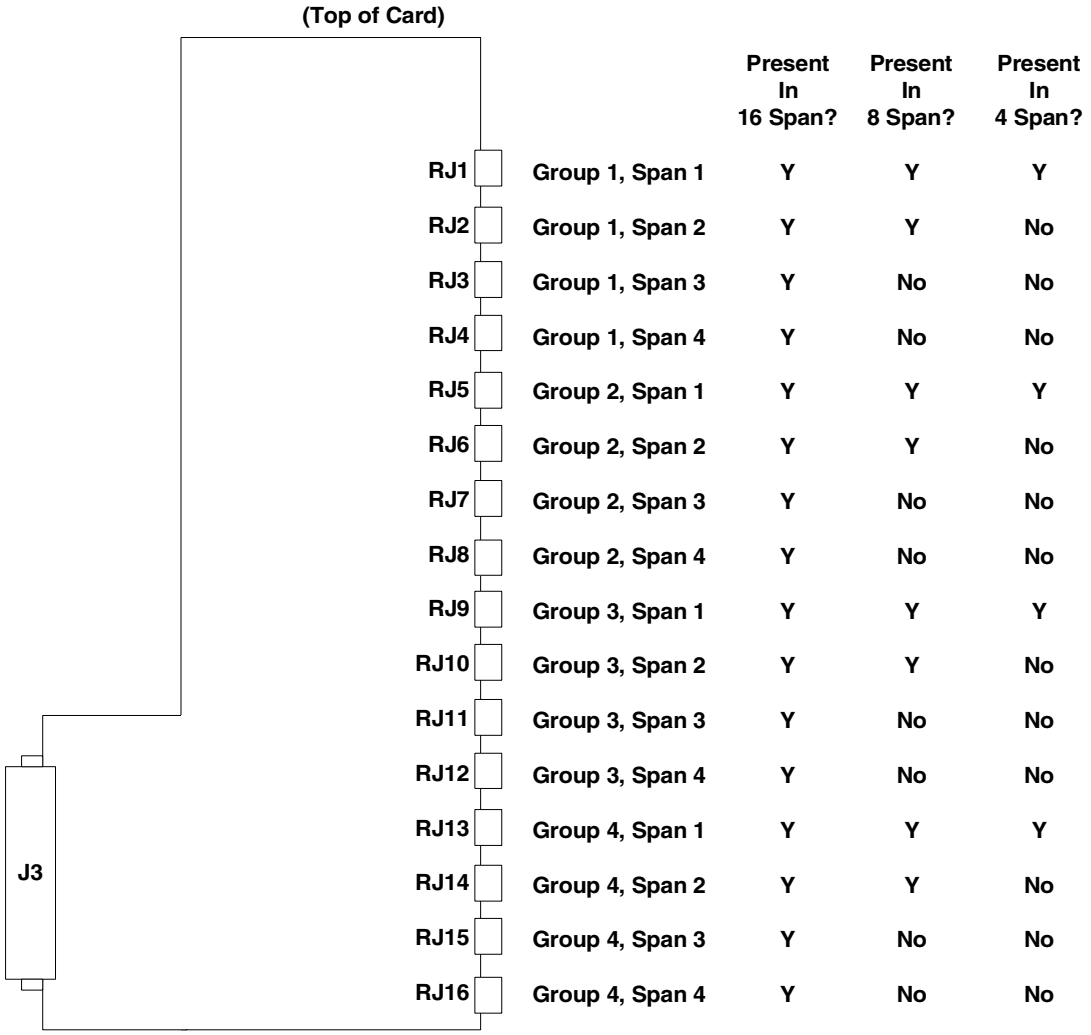


Figure 1: ICC Card and I/O Module Architecture



		Present In 16 Span?	Present In 8 Span?	Present In 4 Span?
RJ1	Group 1, Span 1	Y	Y	Y
RJ2	Group 1, Span 2	Y	Y	No
RJ3	Group 1, Span 3	Y	No	No
RJ4	Group 1, Span 4	Y	No	No
RJ5	Group 2, Span 1	Y	Y	Y
RJ6	Group 2, Span 2	Y	Y	No
RJ7	Group 2, Span 3	Y	No	No
RJ8	Group 2, Span 4	Y	No	No
RJ9	Group 3, Span 1	Y	Y	Y
RJ10	Group 3, Span 2	Y	Y	No
RJ11	Group 3, Span 3	Y	No	No
RJ12	Group 3, Span 4	Y	No	No
RJ13	Group 4, Span 1	Y	Y	Y
RJ14	Group 4, Span 2	Y	Y	No
RJ15	Group 4, Span 3	Y	No	No
RJ16	Group 4, Span 4	Y	No	No

Figure 2: I/O Module Card Layout (16-Span, Circuit Side)

NOTE: Not all components are shown.

2.2.1 EXTERNAL INTERFACES

Table 2 lists the external interfaces for the I/O Module.

Table 2: I/O Module External Interfaces

Interface	Connections
I/O Module to Network	RJ45 Connector with the following pinout: Pin 1 Tx Ring Pin 8 Tx Tip Pin 4 Rx Ring Pin 5 Rx Tip

3.0 PROGRAMMABILITY

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

The ICC card supports a number of programmable parameters which allow card customization:

- E1 programmable protocol
- Line build-out
- Gain control
- Timing for system synchronization
- Transmitted timing source
- Line coding
- Frame control

Cisco Systems can assist in creating your desired parameters on a floppy diskette which you load into the VCO/4K.

3.1 I/O INTERFACE

The J3 connector is the interface between the I/O Module and the ICC card. This includes the following functions:

- Signal buffering
- Transmit clock configuration (per Framer)
- Reference clock selection
- Framer host interface and interrupt control

4.0 I/O MODULE DESCRIPTION

The E1 I/O module supports a 120-ohm network interface for E1.

> *NOTE: The E1 I/O Module also supports a 75-ohm network interface when optional Balun impedance matching devices are used.*
> *(See Technical Bulletin # 63102750100.)*

The I/O Module interfaces the VCO/4K system with 4, 8, or 16 E1 digital data carrier streams. Each stream consists of a 2.048 Mbps, 32-channel, bipolar digital data stream (E1). VCO/4K system synchronization may be set to the receive clock of any E1 span on the I/O Module (the Master Timing Link).

The I/O module's Framers are segmented into groups of four called Framer Groups. This design approach reduces the chance of a single point of failure on the card. A hardware failure on the I/O Module normally affects only a group (1, 2 or 4 spans) and not the entire I/O Module. Figure 3 illustrates the span grouping architecture of the I/O Module.

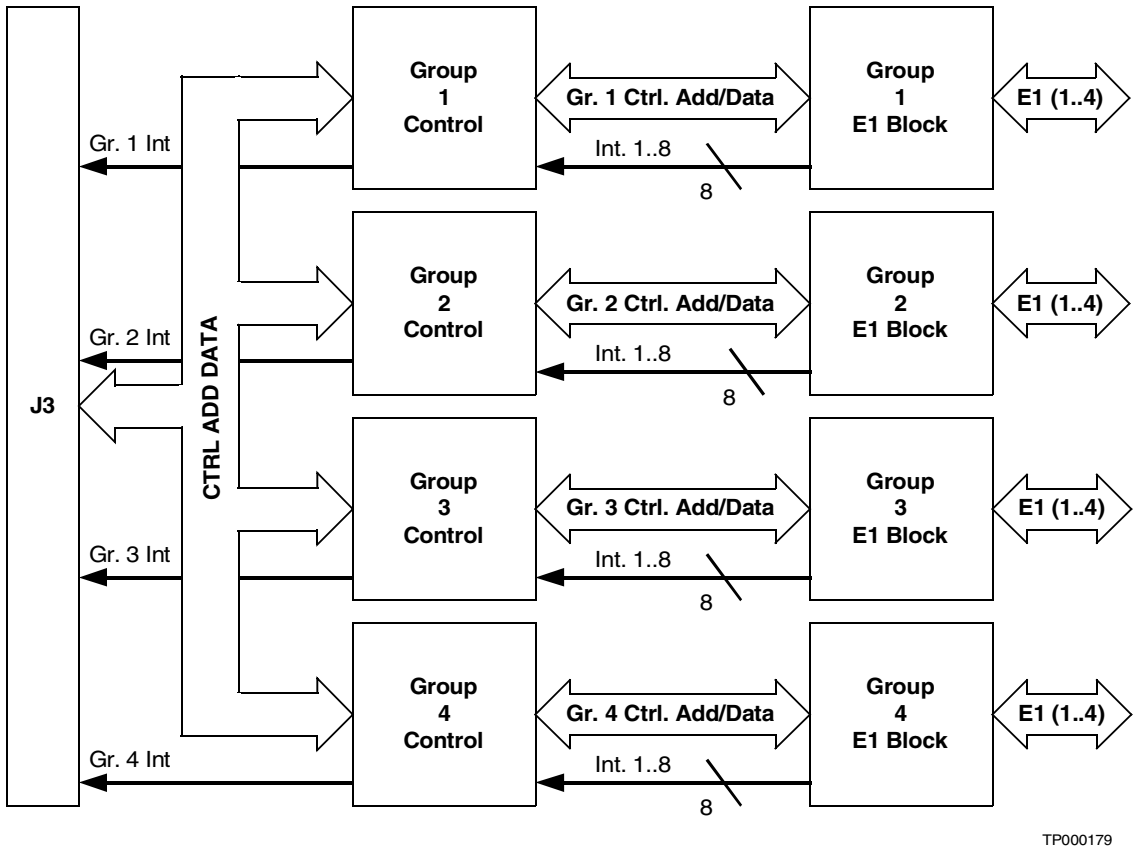


Figure 3: 16-Span I/O Module Span Grouping

The E1 Framer (Figure 4) contains a Line Interface Unit (LIU). The LIU contains three sections: 1) the receiver which handles clock and data recovery, 2) the transmitter which wave shapes and drives the E1 line, and 3) the jitter attenuator.

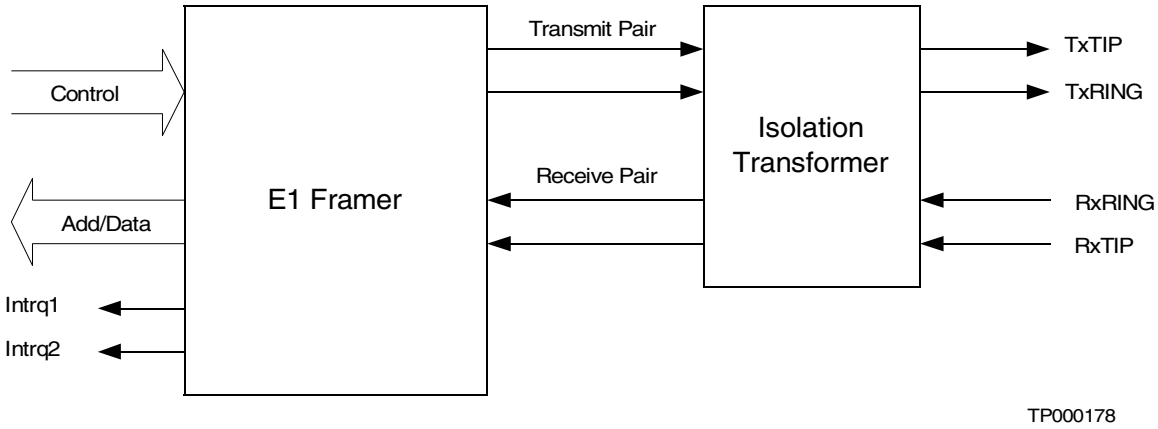


Figure 4: Framer Block Diagram

The LIU adjusts to the E1 signal being received and can handle E1 transmit line lengths to 1.5km as configured from the Port Configuration screen (See the *System Administrators Guide*).

Circuitry on the I/O card detects loss of carrier errors, framing errors, and remote alarms on its incoming E1 stream. It also detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop-timed configurations. The ICC card contains elastic PCM data buffers to minimize slips caused the E1 stream frequency jitter.

Table 3 details the E1 I/O Module's input and output stream specifications.

Table 3: E1 Stream Specifications

Input Stream	
Format	CAS, Clear Channel, or NET5 ISDN
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Frequency	2.048 Mbps +/- 50bps
Impedance	120 Ohms +/- 10%

Table 3: E1 Stream Specifications (Continued)

Output Stream	
Format	CAS, Clear Channel, or NET5 ISDN
Data transparency	Alternate Mark Inversion (AMI), Bipolar with 8 zero substitution (B8ZS), Bit 7 zero stuff, none.
Line Equalization (Drive)	CCITT G.703
Frequency	2.048 Mbps +/- 50bps
Impedance	120 Ohms +/- 10%

The combined Framer/LIU performs:

- Alarm detection (Remote, All 1s, Carrier Lost, Loss of Sync)
- Alarm injection (Remote and All 1s alarms)
- Error counting (CRC4, frame events)
- Channel separation
- G703 framing and out-of-band channel associated signaling
- Out-of-band CAS signaling (A, B, C & D)
- Data transparency
- AMI, HDB3, data encoding

  NOTE: You can use HDB3 for E1 to maintain (1s) density (and timing) while providing data transparency.
- Bipolar-to-TTL conversion on the transmit side
- Electrical wave shaping on the receive side
- Clock recovery
- Jitter attenuation, tolerance, and transfer per G.823
- Loopback and maintenance functions
- Signal monitoring (for loss of signal and quality transmission)

5.0 CONFIGURATION NOTES

There are no jumpers or replaceable PROMs on the I/O Module.

6.0 RELATED DOCUMENTS

For additional information see the ICC card technical description.

Interface Controller Card J1 I/O Module

1.0 GENERAL

The VCO/4K System uses active I/O modules in conjunction with the ICC card to connect to the network. Each I/O Module uses one slot on the backplane and supports one ICC card. The I/O Module is located at the back of the switch and must be aligned with the ICC card. A block diagram for the ICC I/O Module is shown at the bottom of Figure 5.

The J1 I/O Module is a specialized backplane card that provides Japanese 2 Mb network connection to the ICC card. It supports eight spans. The ICC card is inserted in the VCO/4K switch from the front of the system. The I/O Module, inserted at the rear of the system (before ICC insertion), aligns with each ICC card.

The J1 I/O module supports a 110-ohm network interface for PCM and includes active circuitry such as 2 Mb CMI framers.

For information on the ICC card, refer to the Interface Controller Card (ICC) technical description.

2.0 SPECIFICATIONS

2.1 COMPLIANCE WITH STANDARDS

The ICC I/O Module complies with applicable U.S. and international standards. See Table 4.

Table 4: Standards Compliance

Category	Standard
Safety	EN-60950 IEC-950
Jitter	ITU G.823
EMI/EMC	EN55022 (Europe) EN50082-1 (Europe)
PCB Manufacture	IPC
Clocking/Framing	ITU G.703 ITU G.704
Lightning/Power Cross	EN-60950 IEC-950
Telecom	Japan

2.2 I/O MODULE SPECIFICATIONS

Power Requirements (Maximum)	5 Volts (from the ICC card) 8 Span J1 – 1.42 A

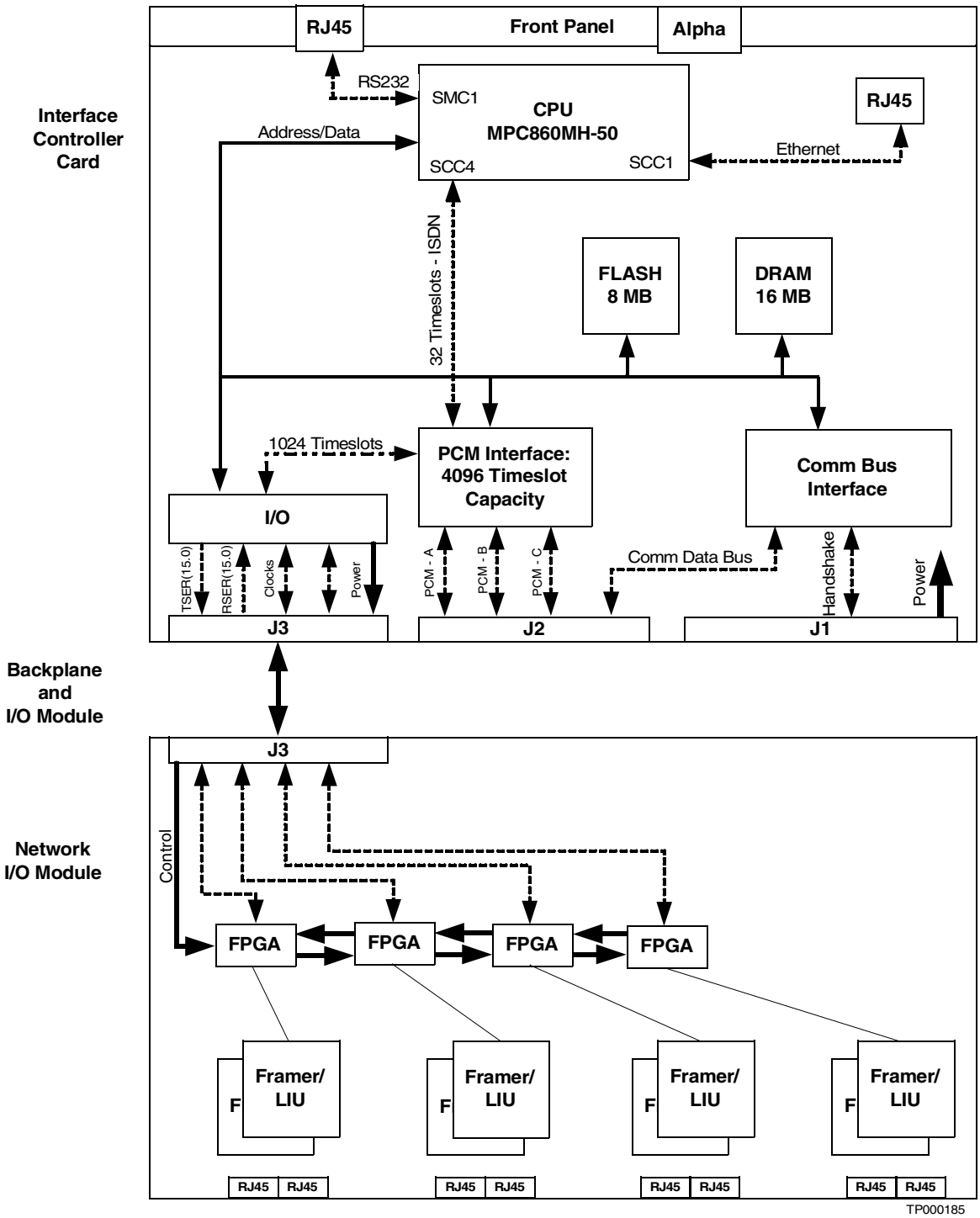


Figure 5: ICC and J1 I/O Module Architecture

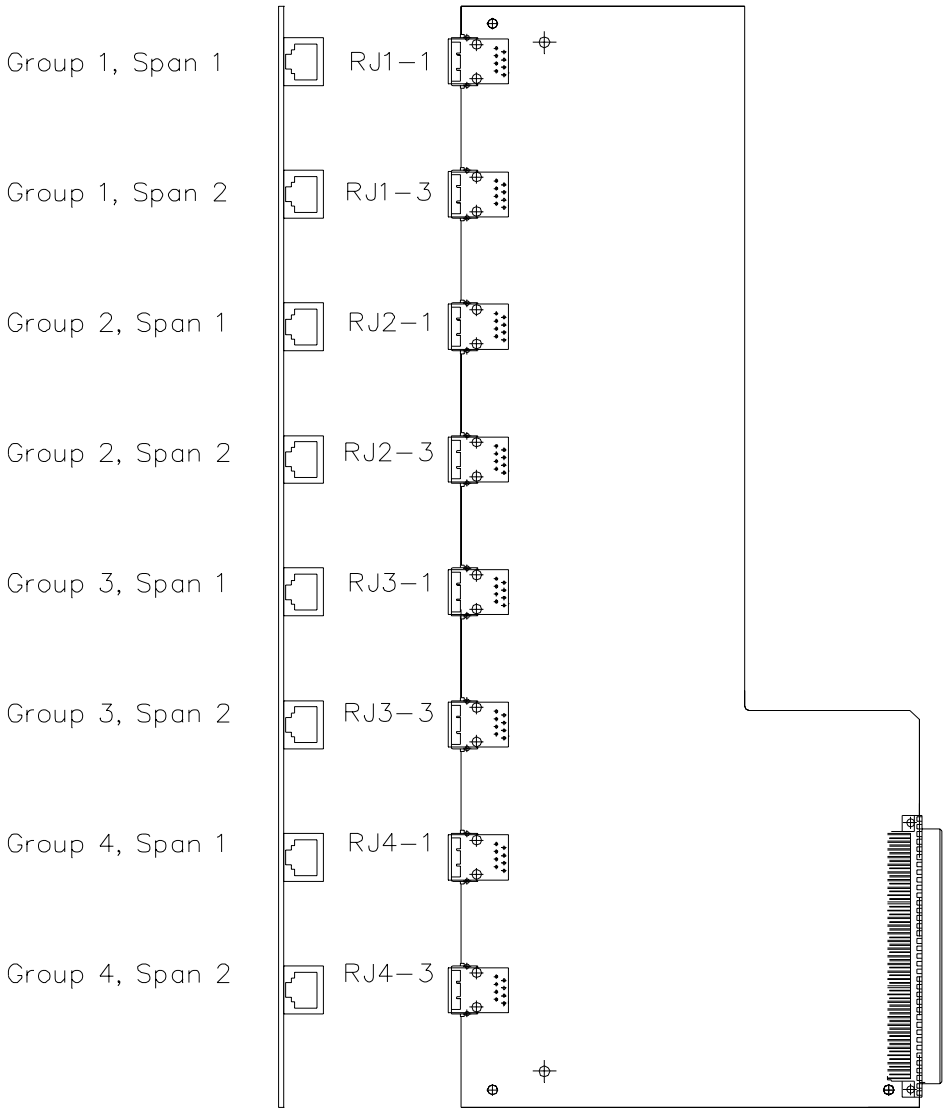


Figure 6: I/O Module Card Layout (8-Span, Circuit Side)

NOTE: Not all components are shown.

2.2.1 EXTERNAL INTERFACES

Table 5 lists the external interfaces for the I/O Module.

Table 5: I/O Module External Interfaces

Interface	Connections
I/O Module to Network	RJ45 Connector with the following pinout: Pin 1 Tx Ring Pin 8 Tx Tip Pin 4 Rx Ring Pin 5 Rx Tip

3.0 PROGRAMMABILITY

You download the application software to each span controller, enabling independent provisioning of each span as well as each channel.

3.1 I/O INTERFACE

The J3 connector is the interface between the I/O Module and the ICC card. This includes the following functions:

- Signal buffering
- Transmit clock configuration (per Framer)
- Reference clock selection
- Framer host interface and interrupt control

4.0 I/O MODULE DESCRIPTION

The J1 I/O module supports a 110-ohm network interface for 2 Mb PCM.

The I/O Module interfaces the VCO/4K system with eight 2 Mb PCM digital data carrier streams. Each stream consists of a 2.048 Mbps, 32-channel, CMI digital data stream. VCO/4K system synchronization may be set to the receive clock of any span on the I/O Module (the Master Timing Link).

The I/O module's Framers are segmented into groups of four called Framer Groups. This design approach reduces the chance of a single point of failure on the card. A hardware failure on the I/O Module normally affects only a group (2 spans) and not the entire I/O Module. Figure 7 illustrates the span grouping architecture of the I/O Module.

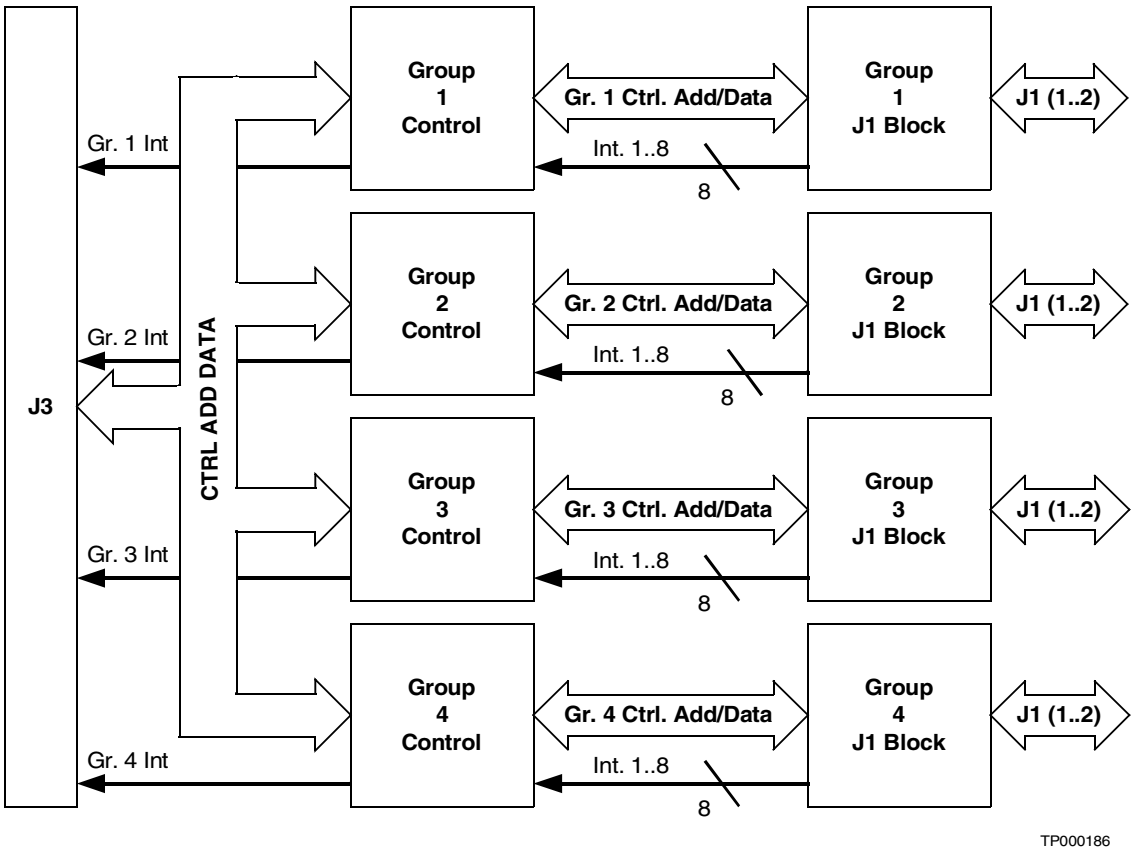


Figure 7: 8-Span I/O Module Span Grouping

The J1 Framer (Figure 8) contains a Line Interface Unit (LIU). The LIU contains three sections: 1) the receiver which handles clock and data recovery, 2) the transmitter which wave shapes and drives the J1 line, and 3) the jitter attenuator.

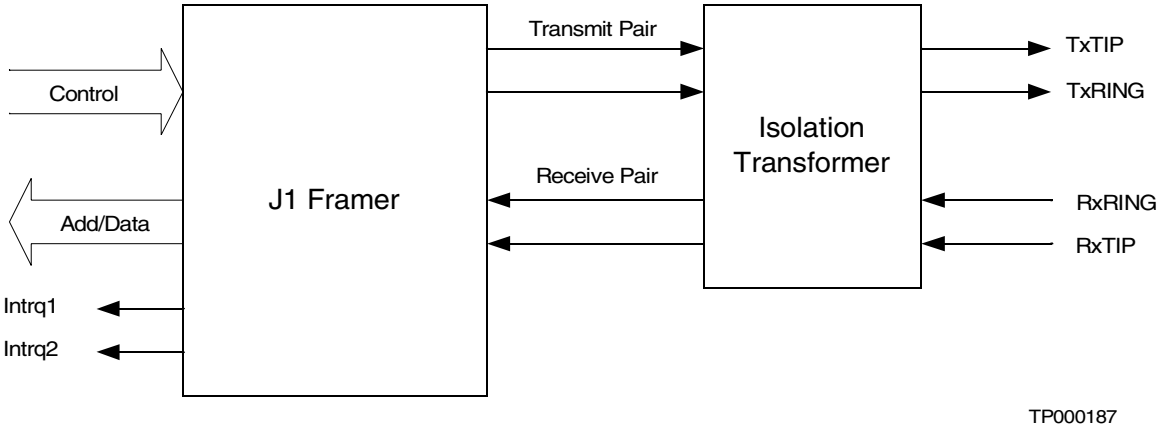


Figure 8: Framer Block Diagram

The LIU adjusts to the signal being received and can handle transmit line lengths to 1.5km as configured from the Port Configuration screen (See the *System Administrators Guide*).

Circuitry on the I/O card detects loss of carrier errors, framing errors, and remote alarms on its incoming stream. It also detects receive/transmit *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop-timed configurations.

Table 6 details the J1 I/O Module's input and output stream specifications.

Table 6: 2 Mb Stream Specifications

Input Stream	
Format	Modified Dipulse
Input level	0.51-3.75 Vp-p
Frequency	2.048 Mhz +/- 100Hz
Impedance	110 Ohms +/- 10%
Output Stream	
Format	Modified Dipulse
Output level	3.0 Vp-p (typical)
Line Equalization (Drive)	CCITT G.703
Frequency	2.048 Mhz +/- 100Hz
Impedance	110 Ohms +/- 10%

The combined Framer/LIU performs:

- Alarm detection (Remote, All 1s, Carrier Lost, Loss of Sync)
- Alarm injection (All 1s alarms)
- Error counting (frame events)
- Channel separation
- Data transparency
- Modified dipulse encoding
- Bipolar-to-TTL conversion on the transmit side
- Electrical wave shaping on the receive side
- Clock recovery
- Jitter attenuation, tolerance, and transfer per G.823
- Loopback and maintenance functions
- Signal monitoring (for loss of signal and quality transmission)

5.0 CONFIGURATION NOTES

There are no jumpers on the I/O Module.

6.0 RELATED DOCUMENTS

For additional information see the ICC card technical description.

Multifrequency R2 Transceiver Card (MFC-R2)

1.0 GENERAL

The MFC-R2 Transceiver Card is a standard service circuit card that can reside in any slot other than those reserved for the control system cards. It includes eight Multifrequency (MF) transceiver circuits that are available for assignment to calls requiring CCITT R2 forward/backward signaling. MFC-R2 ports are allocated and released during a call as specified by the call processing application.

The MFC-R2 is intended for use in switching environments requiring the use of R2 signaling as described in CCITT, Q.440, Q.441, Q.450 through Q.458. Forward and backward signaling is controlled by a state machine running in the on-board packet processor.

The number and type of MFC-R2 cards required by a system is based on anticipated traffic and the call scenario. MFC-R2s are microprocessor-based, firmware controlled, and incorporate standard internal control and digital switch interfaces.

2.0 SPECIFICATIONS

Microprocessor:	8031 (12 MHz)
Memory:	8K Bytes EPROM 2K Bytes RAM
Power Requirements:	Typical
Transmitter (CCITT, Q.454):	
Frequency tolerance	± 1Hz from nominal
Twist (high/low)	0.5dB
Output	-11.5dBmo, ± 1dB
Receiver (CCITT, Q.455):	
Detection range	-35 to -5dBm0
Frequency offset	± 10Hz
Allowable twist	± 6dB
Minimum tone duration	7ms
Transmitted/Detected Tones:	
Forward Signals	Group I and Group II
Backward Signals	Group A and Group B

Refer to Tables 1 through 4

Table 1: CCITT, Q.441-R2 Signaling Group I Forward Signals

Comb.	Desig.	Frequencies	Meaning *Note1*	Meaning *Note 2*
1	I-1	1380 + 1500Hz	Language Digit: French	Digit 1
2	I-2	1380 + 1620Hz	Language Digit: English	Digit 2
3	I-3	1500 + 1620Hz	Language Digit: German	Digit 3
4	I-4	1380 + 1740Hz	Language Digit: Russian	Digit 4
5	I-5	1500 + 1740Hz	Language Digit: Spanish	Digit 5
6	I-6	1620 + 1740Hz	Language Digit: (Spare)	Digit 6
7	I-7	1380 + 1860Hz	Language Digit: (Spare)	Digit 7
8	I-8	1500 + 1860Hz	Language Digit: (Spare)	Digit 8
9	I-9	1620 + 1860Hz	Spare: (Discriminating Digit)	Digit 9
10	I-10	1740 + 1860Hz	Discriminating Digit	Digit 0
11	I-11	1380 + 1980Hz	Country Code Indicator, outgoing half-echo suppressor required	Access to incoming operator (Code 11)
12	I-12	1500 + 1980Hz	Country Code Indicator, no echo suppressor required	a) Access to delay operator (Code 12) b) Request not accepted
13	I-13	1620 + 1980Hz	Test Call Indicator (Call by automatic test equipment)	a) Access to test equipment (Code 13) b) Satellite link not included
14	I-14	1749 + 1980Hz	Country Code Indicator, outgoing half-echo suppressor required	a) Incoming half-echo suppressor required b) Satellite link included
15	I-15	1860 + 1980Hz	Not used	a) End-of-pulsing (Code 15) b) End of identification

Note 1: When signal is the first transmitted on an international link terminating in the destination country of the call.

Note 2: When signal is other than the first signal on an international link.

Table 2: CCITT, Q,441-R2 Signaling Group II Forward Signals

Comb.	Designation	Frequencies	Meaning	Notes
1	II-1	1380 + 1500Hz	Subscriber without priority	National Use Only
2	II-2	1380 + 1620Hz	Subscriber with priority	
3	II-3	1500 + 1620Hz	Maintenance equipment	
4	II-4	1380 + 1740Hz	Spare	
5	II-5	1500 + 1740Hz	Operator	
6	II-6	1620 + 1740Hz	Data transmission	
7	II-7	1380 + 1860Hz	Subscriber (or operator w/o forward transfer facility	International Use Only
8	II-8	1500 + 1860Hz	Data transmission	
9	II-9	1620 + 1860Hz	Subscriber without priority	
10	II-10	1740 + 1860Hz	Operator with forward transfer facility	
11	II-11	1380 + 1980Hz	Spare for National Use	
12	II-12	1500 + 1980Hz		
13	II-13	1620 + 1980Hz		
14	II-14	1749 + 1980Hz		
15	II-15	1860 + 1980Hz		

Table 3: CCITT, Q.441-R2 Signaling Group A Backward Signals

Comb.	Designation	Frequencies	Meaning
1	A-1	1140 + 1020Hz	Send next digit (*n*+1)
2	A-2	1140 + 900Hz	Send last but one digit (*n*-1)
3	A-3	1020 + 900Hz	Address-complete, changeover to reception of Group B signals
4	A-4	1140 + 780 Hz	Congestion in the national network
5	A-5	1020 + 780Hz	Send calling party's category
6	A-6	900 + 780Hz	Address-complete, charge, setup speech conditions
7	A-7	1140 + 660Hz	Send last but two digit (*n*-2)
8	A-8	1020 + 660Hz	Send last but three digit (*n*-3)
9	A-9	900 + 660Hz	Spare (*for national use*)
10	A-10	780 + 660Hz	Spare (*for national use*)
11	A-11	1140 + 540Hz	Send country code indicator
12	A-12	1020 + 540Hz	Send language or discriminating digit
13	A-13	900 + 540Hz	Send nature of circuit
14	A-14	780 + 540Hz	Request for information on use of echo suppressor (Is an incoming half-echo suppressor required?)
15	A-15	660 + 540Hz	Congestion in an international exchange or at its output

Table 4: CCITT, Q.441-R2 Signaling Group B Backward Signals

Comb.	Designation	Frequencies	Meaning
1	B-1	1140 + 1020Hz	Spare *(for national use)*
2	B-2	1140 + 900Hz	Send special information tone
3	B-3	1020 + 900Hz	Subscriber line busy
4	B-4	1140 + 780Hz	Congestion (encountered after changeover from Group A to Group B signals)
5	B-5	1020 + 780Hz	Unallocated number
6	B-6	900 + 780Hz	Subscriber's line free, charge
7	B-7	1140 + 660Hz	Subscriber's line free, no charge
8	B-8	1020 + 660Hz	Subscriber's line out of order
9	B-9	900 + 600Hz	Spare *(for national use)*
10	B-10	780 + 660Hz	
11	B-11	1140 + 540Hz	
12	B-12	1020 + 540Hz	
13	B-13	900 + 540Hz	
14	B-14	780 + 540Hz	
15	B-15	660 + 540Hz	

3.0 CIRCUIT DESCRIPTION

The MFC-R2 provides VCO/4K systems with eight MFC transceivers. These transceivers are typically used when compelled MF (R2) signaling must be decoded on E1 digital trunks.

Each MFC-R2 port can independently listen to any time slot on either PCM data bus. For a typical call setup, an MFC transceiver port is assigned by software to listen to the output of a E1 card and report any signaling tones that are received. A state machine in the Packet Processor autonomously determines when forward/backward signaling is required based on the contents of an Outpulse Rule. When the MFC transceiver port is released when the call is cut through for completion.

Figure 1 shows a simplified block diagram of the MFC-R2.

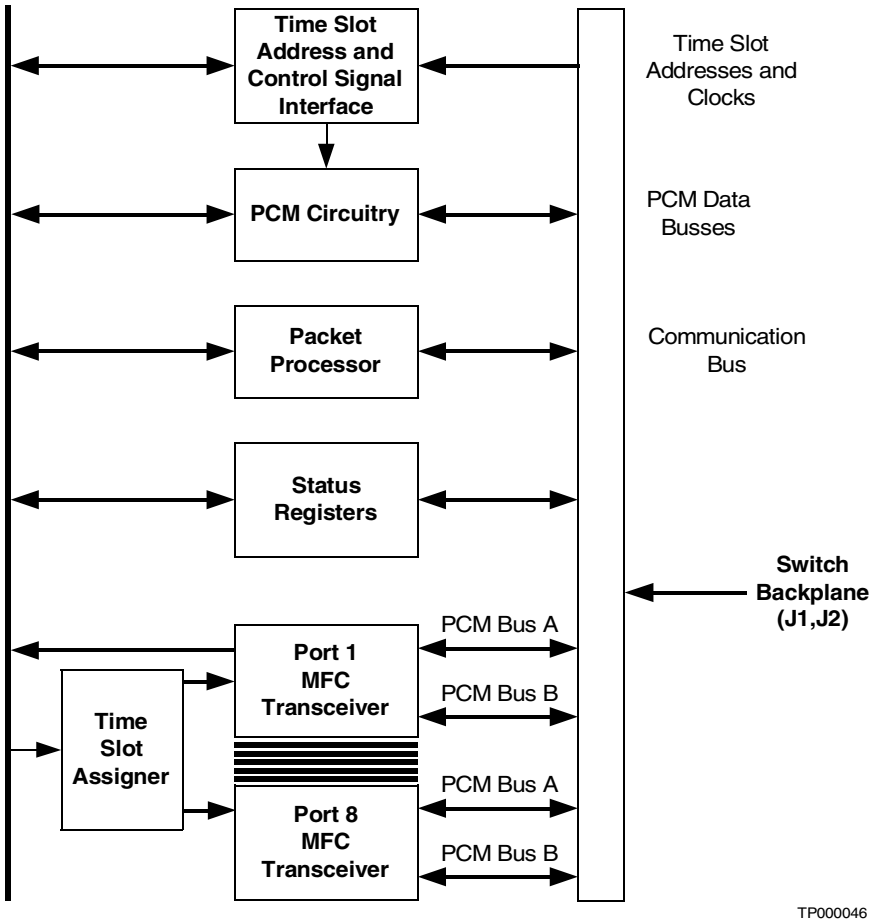


Figure 1: Block Diagram of MFC-R2

3.1 MFC TRANSCEIVERS

Each MFC-R2 card is equipped with four dual channel MFC transceivers. These transceivers contain all the logic necessary to transmit and receive CCITT R2 forward and backward MF signals. The transceivers accept direct A-Law PCM with 2.048Mbps clocking.

Each dual channel transceiver interfaces with two digital PCM interfaces (4 transceivers X 2 PCM interfaces = 8 transceiver ports per MFC-R2 card.) The transceivers are controlled through an interface with the on-board Packet Processor. Figure 2 shows a block diagram of the MFC transceiver interfaces.

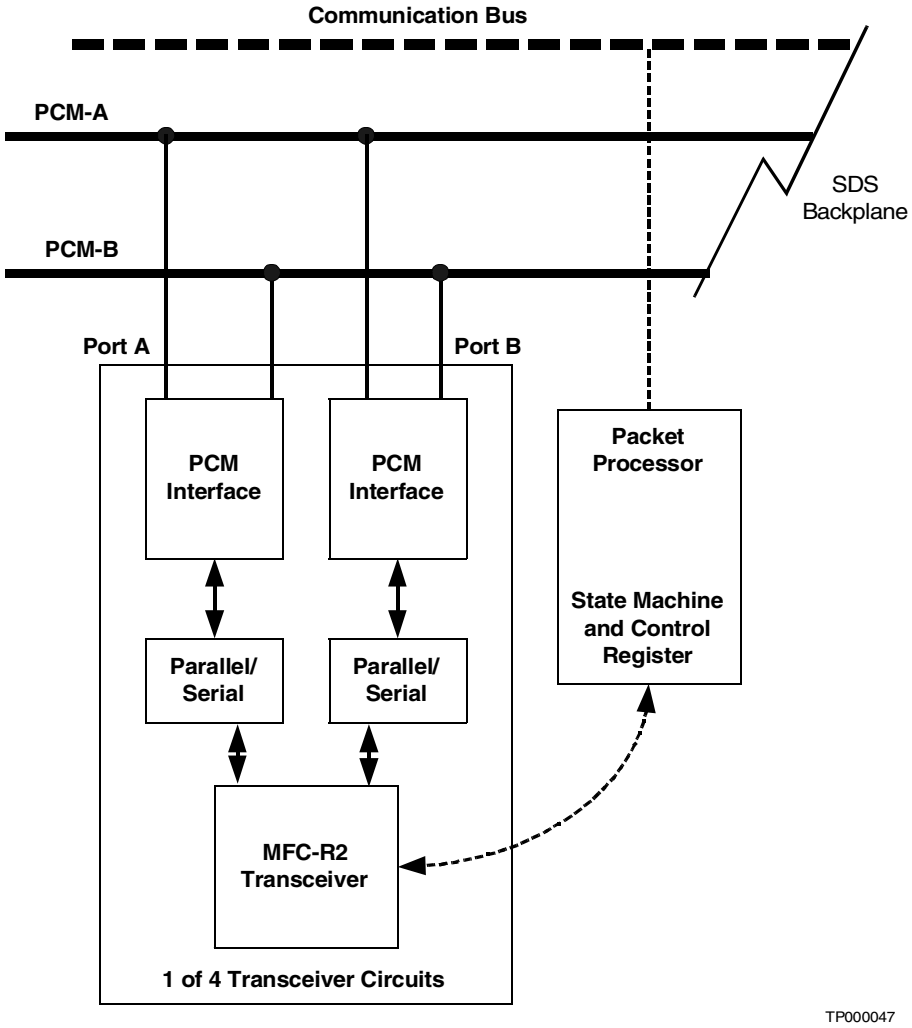


Figure 2: Block Diagram of MFC Transceiver Interfaces

For outdialling, the R2F frequencies (Groups I & II Forward) are transmitted and the R2B frequencies (Groups A & B Backward) are received. When collecting incoming R2 signals, R2B frequencies are transmitted and R2F frequencies are received. In automatic mode these transceivers perform compelled signaling handshakes autonomously. Figure 3 shows a flowchart of MFC-R2 Transceiver functions.

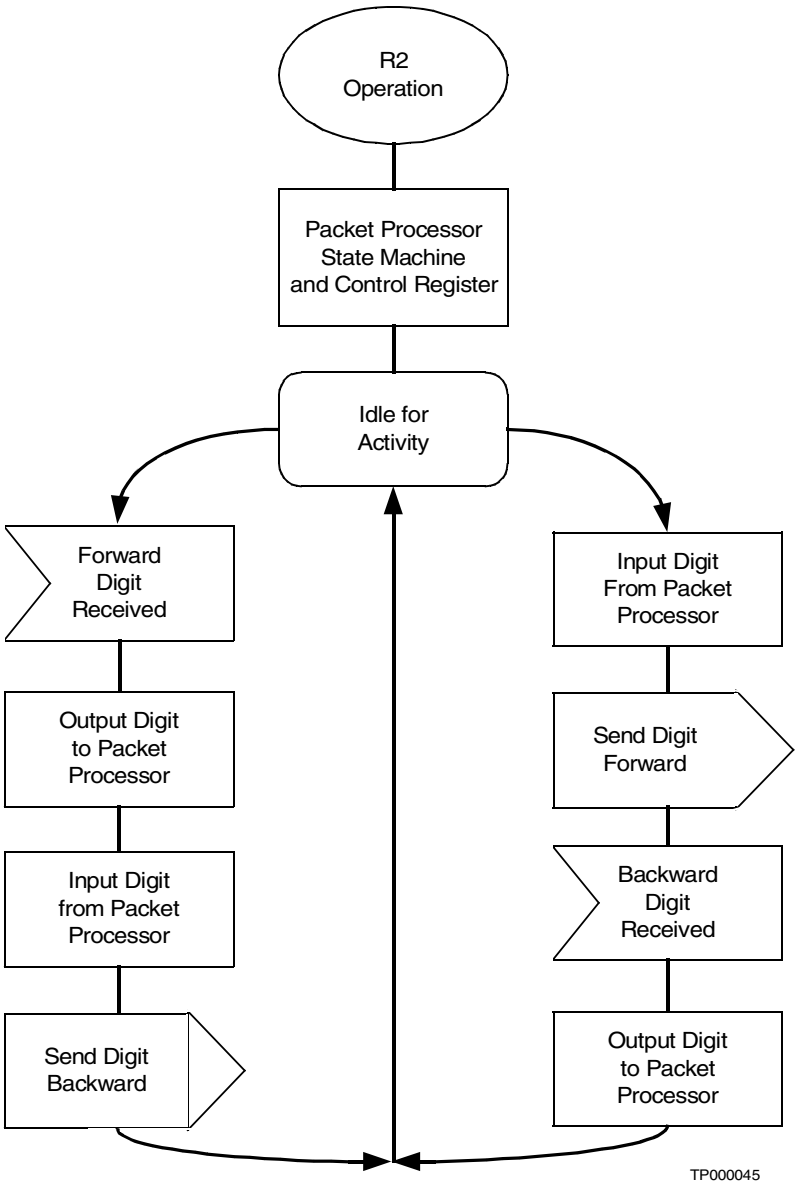


Figure 3: Flowchart of MFC-R2 Transceiver Functions

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within the system is encoded and transmitted as Pulse Code Modulated (PCM) data. Each MFC transceiver directly interfaces with PCM, A-law data delivered from the system backplane. The MFC-R2 interfaces to the PCM timeslot bus structure with bus interface circuitry common to port cards.

Wen a MFC-R2 is plugged into the system, it is automatically assigned a set of eight consecutive port addresses. The PCM data and timeslot bus interfaces control the capture of the correct PCM data for reception by each MFC transceiver port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which timeslot and bus a given port listens and transmits.

3.3 PACKET PROCESSOR

The MFC-R2 contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the system with the exception of the Network Bus Controller-3 (NBC-3).

The Packet Processor consists of the 8031 microcomputer, program and data memory, the Communication Bus Interface, an asynchronous serial port, and the LED register. It is via the Communication Bus that the NBC issues commands to the MFC-R2 in the form of data "packets". The MFC-R2 reports the status of its MFC transceivers over the same bus using the data packet protocol. When polled by the NBC, the Packet Processor reports any status change.

On MFC-R2 cards, the Packet Processor also runs a state machine that reads the incoming packet and controls send/receive operations over individual transceiver ports. This arrangement minimizes traffic over the Communication Bus. The Packet Processor also maintains a register of signaling events and collected digits. This register is accessed during sending operations and may be used to send MF digit reports to a host computer.

The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's J3 connector. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

3.4 MFC-R2 STATUS LEDS

A red, a yellow, and a green LED are visible through the MFC-R2's front panel to indicate the status of the card. Each LED is turned on when the software generic sets a bit low in an external memory register. Typically an illuminated red LED indicates a major card failure, an illuminated yellow LED indicates a minor card failure, and an illuminated green LED indicates the card is in standby or diagnostic mode (refer to *Section 6.01*).

3.5 GAIN CONTROL AND COMPANDING TYPES

The forward and backward signal levels can be controlled using two DIP switches located on the MFC-R2 board. Refer to *Section 4.0* for specific gain control settings.

3.6 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 5 lists the pin assignments for J1 on the MFC-R2.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.7 PCM BUS INTERFACES - J3 PIN ASSIGNMENTS

Table 6 lists the pin assignments for J3 on the MFC-R2.

Table 5: MFC-R2 J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V

Table 5: MFC-R2 J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 6: MRF-R2 Pin Assignments

Pin	Row A	Row B	Row C
1 through 28	Unused	Unused	Unused
29	Unused	Unused	DGND
30	Unused	Unused	RS-232 DX (Out)
31	Unused	Unused	RS-232 DR (In)
32	Unused	Unused	DGND

4.0 CONFIGURATION NOTES

The MFC-R2 is manufactured by Cisco Systems, Inc. Jumper plugs on the MFC-R2 are factory set for use in VCO/4K systems. Figure 5 indicates the location of DIP switches and PROMs on a MFC-R2 based on the card's PCB revision level. Use this information to verify the card's configuration prior to installing it

NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.

If you improperly configure a card, it may fail to operate. Therefore, take great care to verify configuration settings before installing a replacement service circuit card in the system.

4.0.1 PROM

The 2764 PROM in location U2 contains firmware appropriate to MFC-R2 polling and call processing requirements.

4.0.2 DIP SWITCHES

This card can be configured to provide register signaling services compatible with Mu-Law and A-Law PCM companding types and supports customer selection of tone output levels. The two DIP switches labelled SW2 and SW3 control the forward/backward signal level gains.

The factory default settings are designed to be compatible with most installation requirements using A-Law DTG cards

NOTE: Switch positions 4 and 5 must be set according to your system's configuration. When using a Mu-Law tone card, the switches must reflect the DTG Type Mu setting. The switches should always indicate the Device Type A unless changed by the factory.

Table 7: SW2 Factory Default Settings

Position	Meaning CLOSED	Meaning OPEN	Factory
1	reserved	reserved	closed
2	reserved	reserved	closed
3	reserved	reserved	closed
4	DTG Type Mu	DTG Type A	open
5	Device Type Mu	Device Type A	open

Table 8: SW3 Factory Default Settings

Position	Meaning CLOSED	Meaning OPEN	Factory
1	Gain-0 Disabled	Gain-0 Enabled	closed
2	Gain-1 Disabled	Gain-1 Enabled	closed
3	Gain-2 Disabled	Gain-2 Enabled	closed
4	Device Type Mu	Device Type A	open
5	DTG Type Mu	DTG Type A	open

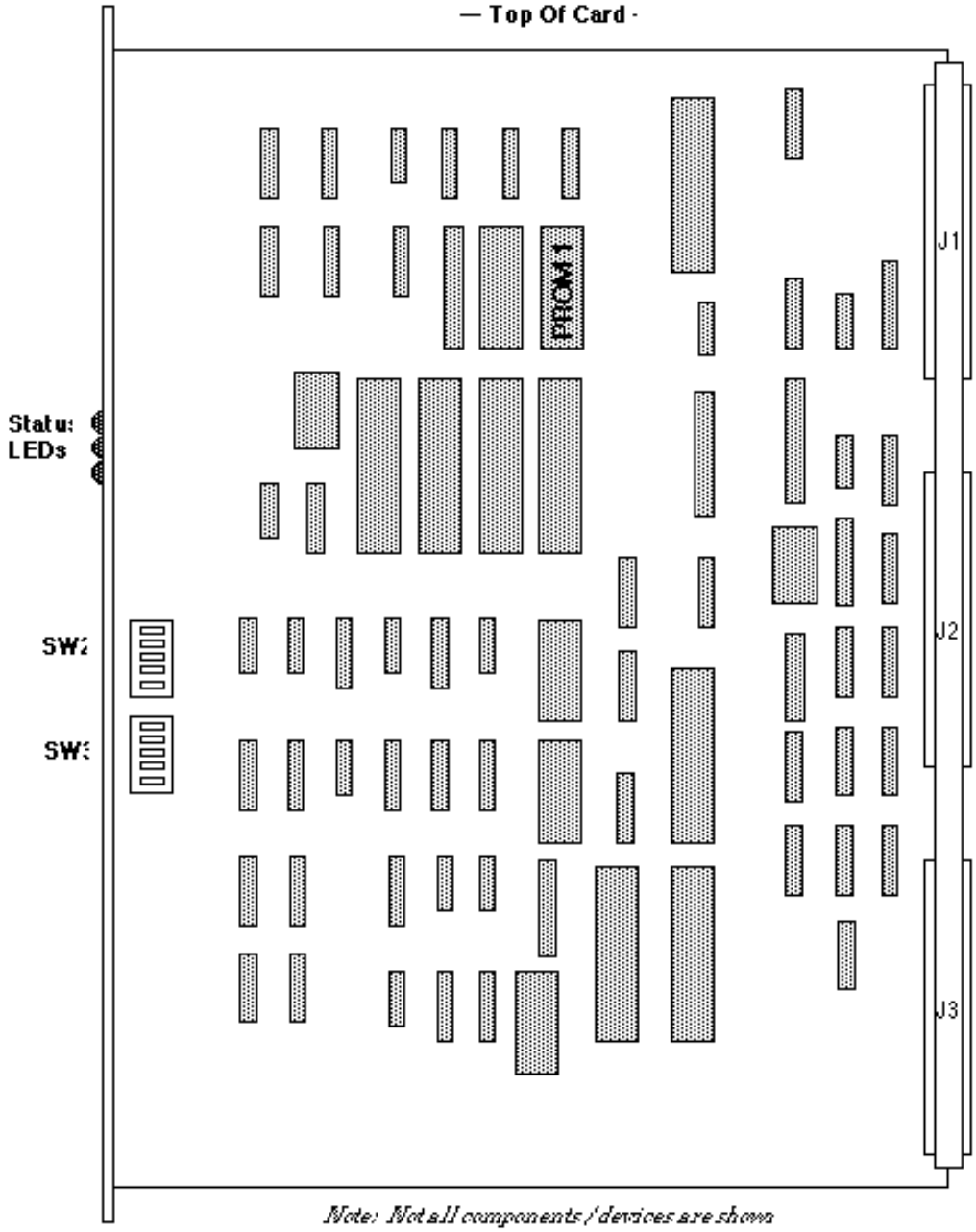


Figure 4: MFC-R2 PROM Location

5.0 RELATED DOCUMENTS

For additional information, refer to the following publications:

- New Zealand Supplement
- VCO/4K System Administrator's Guide
- VCO/4K Standard or Extended Programming Reference

Subscriber Line Interface Card for International (SLIC-INT)

1.0 GENERAL

The Subscriber Line Interface Card for International (SLIC-INT) is a standard port interface circuit card that can reside in any slot other than those reserved for the control system cards. The SLIC-INT provides interface to eight incoming or outgoing 1AS 2-wire lines connected directly to telephones, each with a dedicated DTMF receiver and dial pulse detection. It also supports dry loop, dial-up connections from the PSTN to the VCO/4K, such as. OPX; the SLIC-INT supplies battery. The A and B leads are fused.

Terminating connections to directly connected stations are supported when a ring generator is connected to the system. A maximum of four ringers can be supported by SLIC-INT circuits.

> *NOTE: SLIC-INT ports may be connected to cabling which must be equipped with over-voltage protection to comply with BS6701 Part 1: 1986. Verify that all external cabling complies with BSI standards before connecting lines to* VCO/4K *SLIC-INT interface ports.*

2.0 SPECIFICATIONS

Microprocessor:		8031 (12 MHz)	
Memory:		8K Bytes EPROM	
		2K Bytes RAM	
Power Requirements:		Typical	Maximum
	+5 Volts:	500mA	900mA
	+15 Volts:	120 mA	210mA
	-15 Volts:	125mA	230mA
	+24 Volts:	25mA	29 mA
	-48 Volts:	38mA nominal	
	*per-port current requirements		
	Trunk Specifications:		
Input Level:		-3 dB ± 0.5 dBm	
Output Level:		-3 dB ± 0.5 dBm	
Crosstalk Attenuation:		68 dB minimum	
Idle Circuit Noise:		23 dBrnc maximum	
Line Impedance:		OTR-001 Complex Termination	

Echo Return Loss:	18 dB minimum
	(-2 dBm input)
	Singing Return Loss:
Low (200 - 500 Hz):	12 dB minimum
High (2500 - 3200 Hz):	15 dB minimum
Cable Return Loss:	0 dB minimum
	2 dB maximum
	Frequency Response:
	(Signal levels relative to 1004 Hz with C Message Filter)
	60 Hz: -20 dB maximum
	300 Hz: -3.0 + 0.5 dB
	600 to 2400 Hz: -3.0 + 0.5 dB
	3200 Hz: -3.0 + 0.5 dB
	Longitudinal Balance:
	200-1000 Hz: 60 dB minimum
	1000-4000 Hz: 50 dB minimum
Loop Current:	38 mA nominal (constant current source)
	DTMF Receiver:
Detectable input level:	-25 dBm minimum
	1 dBm maximum
Acceptable twist:	10 dB maximum
Tone or quiet duration:	40 mS minimum

3.0 CIRCUIT DESCRIPTION

Figure 1 shows a simplified block diagram of the SLIC-INT. The five major elements of the SLIC-INT are:

- Per Port Circuitry
- PCM Time Slot Bus Interface
- Packet Processor
- Control & Status Registers
- Protective Devices

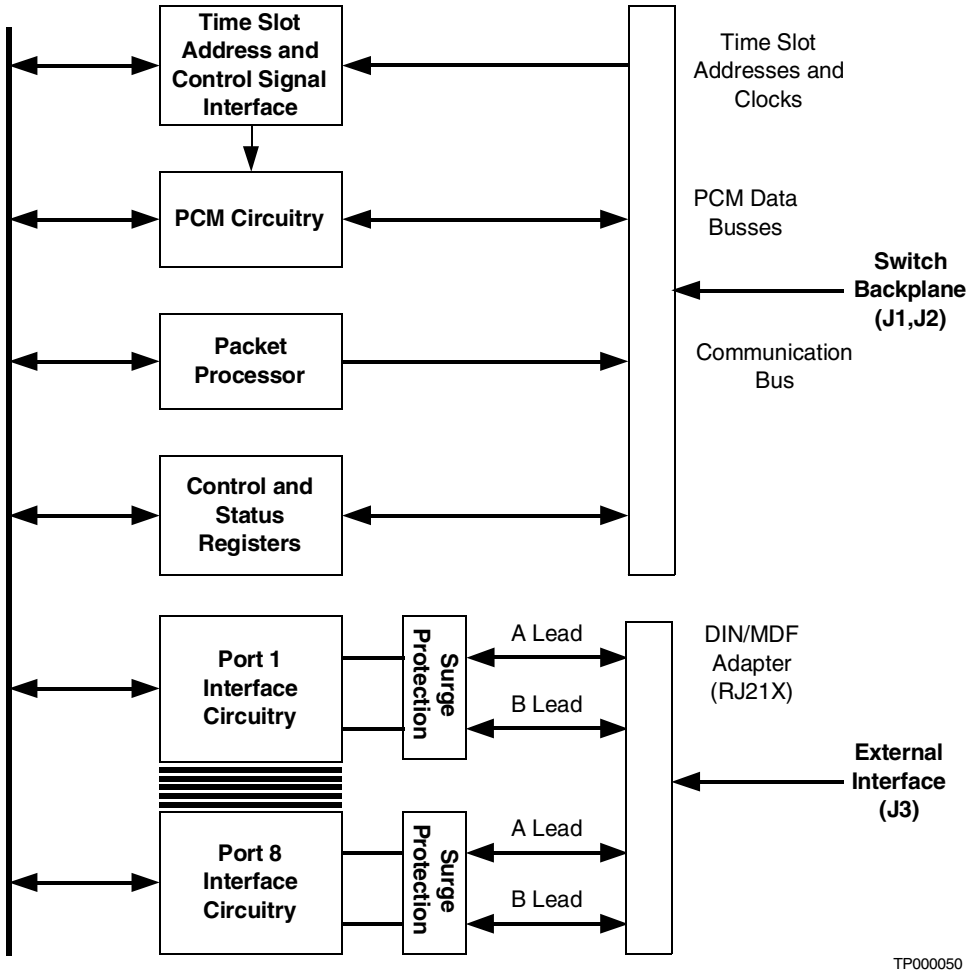


Figure 1: Block Diagram of SLIC-INT

3.1 PER PORT CIRCUITRY

Each of the eight ports on a SLIC-INT includes the following:

- DTMF Digit Receiver
- Analog to Digital Encoding and Decoding
- Hybrid 2-wire to 4-wire conversion circuit
- On/Off hook detection
- Relay to attach ring voltage to a line
- Automatic ring relay trip on off-hook
- Surge protection across A and B leads.

3.1.1 DTMF DIGIT RECEIVER

A DTMF digit receiver integrated circuit (I.C.) is provided for each SLIC-INT port. The receiver is connected to the incoming analog signal and can identify DTMF digits 0 through 9, A, B, C, D, #, and *.

3.1.2 ANALOG TO DIGITAL ENCODING & DECODING

A 2913 codec provides digital-to-analog and analog-to-digital signal conversion. A codec semi-custom interface I.C. performs parallel-to-serial and serial-to-parallel conversion of the PCM data transferred between itself and the codec.

Data received from both PCM busses is latched into parallel in/serial out shift registers internal to the codec interface I.C. The codec semi-custom interface I.C. supplies the data by selecting the output of one of the two internal parallel-to-serial shift registers. Selection is based on the state of a bus select signal.

The codec can operate at clock frequencies of 1.544 MHz or 2.048 MHz and can encode/decode A-law or µ-law PCM data. Two jumper areas on the SLIC-INT allow selection of the clock frequency and PCM encoding rule for all eight codecs.

3.1.3 ANALOG INTERFACE

The analog interface consists of the circuitry from the A and B leads to the codec. An AMSþ2006 Subscriber Line Interface Circuit Hybrid performs the 2-wire to 4-wire conversion, provides internal lightning protection, and drives battery onto the A and B leads. The hybrid also monitors the current on the A and B leads to determine port on/off hook status, and outputs an on/off hook status bit. When a port is not terminated (on hook), the balance network is unbalanced. When this condition exists, an analog signal driven from the codec's receive amplifier into the hybrid is driven back to the input of the codec's transmit amplifier. Jumper area Jx01 is provided to allow analog signal outgoing gain selection of 0 or -3 dB.

A DTMF digit receiver I.C. is connected to the analog signal output by the hybrid and input by the codec's transmit amplifier. A 3.5795 MHz crystal oscillator is provided to generate the clock signal required by the DTMF digit receivers.

3.1.4 CONTROL RELAY

A relay is provided for each SLIC-INT port. When energized, this relay connects ring voltage from the backplane to the port's B lead, ringing a telephone connected to the port. When the telephone goes off hook, the firmware automatically de-energizes and disables the ring relay to stop the ringing and prevent ring voltage from reconnecting when the telephone goes onhook.

3.1.5 A & B LEAD PROTECTIVE DEVICES

The A and B leads of the eight circuits on the SLIC-INT are protected from overvoltage and overload conditions as shown in Figure 2 below.

The SIDACtor™ on each port provides transient surge protection from lightning, line transients and other damaging voltage spikes. This single package device protects against A lead to B lead, A lead to Ground, and B lead to Ground transients. When the monitored voltage exceeds 235 Vac, the SIDACtor switches on through a negative resistance region to a low on-state voltage in nanoseconds. It continues to conduct until the current is interrupted or drops below the minimum holding current of the device.

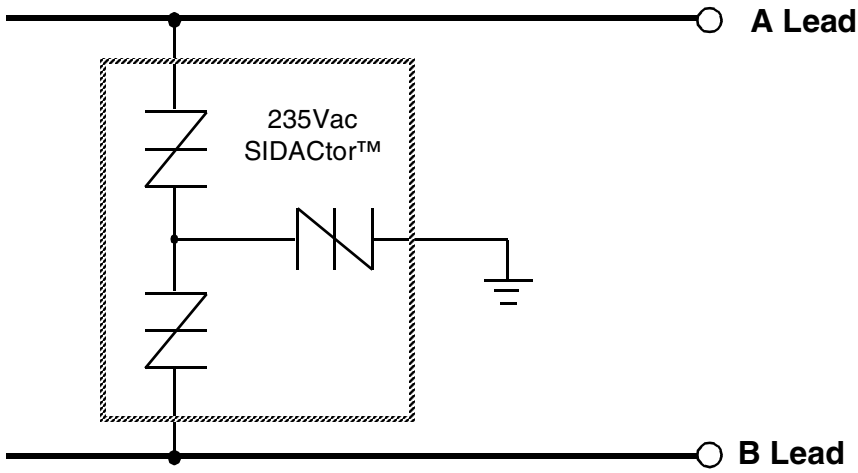


Figure 2: Schematic Diagram of A & B Lead Protective Devices

3.2 PCM TIME SLOT BUS INTERFACE

All voice data within a VCO/4K is encoded and transmitted as Pulse Code Modulated (PCM) data. The per port codec on the SLIC-INT translates outgoing voice data from PCM digital data to an analog signal and translates incoming voice data from an analog signal to PCM encoded digital data. The SLIC-INT interfaces to the dual PCM time slot busses with bus interface circuitry common to several VCO/4K port-oriented circuit cards. Each of the eight port interfaces on the SLIC-INT can “listen to” any time slot on either PCM data bus.

A SLIC-INT is automatically assigned a set of eight consecutive port addresses when it is entered into the data base. The PCM data and time slot bus interfaces control the transmission of PCM data onto the appropriate PCM bus during the correct eight consecutive time slots. They also control the capture of the correct PCM data for transmission by a particular SLIC-INT port.

The two PCM busses are functionally equivalent. The transmit time slot and PCM data bus for a particular port is also used to identify the port when selecting to which time slot and bus a given port listens.

3.3 PACKET PROCESSOR

The SLIC-INT contains an 8031-based Packet Processor that interfaces to the Communication Bus. A Packet Processor is part of all cards in the system, with the exception of the Network Bus Controller-3 (NBC-3). The Packet Processor polls each of the eight line/trunk connections looking for an event (i.e. off hook detection or valid DTMF digit reception). When polled by the NBC-3, the Packet Processor reports any status change. The Packet Processor supports a diagnostic serial port connected to a signal line on the backplane. The Packet Processor also controls three status LEDs (red, yellow, and green) which are visible through the card’s front panel.

The Packet Processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry; the Communication Bus Interface; an asynchronous serial port; and the LED register. The 8031 provides the intelligence for the Packet Processor and, therefore, for the SLIC-INT.

The Communication Bus is the path by which the Packet Processor receives commands from and sends status to the Network Bus Controller.

3.4 PCM BUS INTERFACES – J1 PIN ASSIGNMENTS

Table 1 lists the pin assignments for J1 on the SLIC-INT.

NOTE: J2 Pin Assignments are proprietary and are, therefore, not documented for customer use.

3.5 EXTERNAL INTERFACES

The connections to the A and B leads of the eight line/trunk interfaces on the SLIC-INT are made via the J3 connector. An I/O module for VCO/4K systems attaches to J3 and terminates the A/B connections of up to three SLIC-INTs to a standard RJ21X, 25-pair connector. It is expected that dry line/trunk connections be made via the RJ21X connector to the A and B leads of the individual lines/trunks (SLIC-INT provides battery). The J3 pin assignments for each SLIC-INT card are provided as Table 2. J3 to RJ21X pinouts are shown in Table 3 and Figure 4.

Table 1: J1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Ring Voltage
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	+24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0

Table 1: J1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	CTV	Unused	CTT
30	GND	Unused	GND
31	GND	Unused	GND
32	DGND	Unused	DGND

Table 2: SLIC-INT J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Unused
2	Trunk 1 – A Lead	Unused	Trunk 1 – B Lead
3	Unused	Unused	Unused
4	Unused	Unused	Unused
5	Unused	Unused	Unused
6	Trunk 2 – A Lead	Unused	Trunk 2 – B Lead
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Trunk 3 – A Lead	Unused	Trunk 3 – B Lead
11	Unused	Unused	Unused
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Trunk 4 – A Lead	Unused	Trunk 4 – B Lead
15	Unused	Unused	Unused

Table 2: SLIC-INT J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Trunk 5 – A Lead	Unused	Trunk 5 – B Lead
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Trunk 6 – A Lead	Unused	Trunk 6 – B Lead
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Trunk 7 – A Lead	Unused	Trunk 7 – B Lead
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Trunk 8 – A Lead	Unused	Trunk 8 – B Lead
31	Unused	Unused	Unused
32	Unused	Unused	Unused

Table 3: J3 To RJ21X Pinouts

Card	Trunk	A Lead	B Lead
1	1	J3-2A to RJ21X-26	J3-2C to RJ21X-1
1	2	J3-6A to RJ21X-27	J3-6C to RJ21X-2
1	3	J3-10A to RJ21X-28	J3-10C to RJ21X-3
1	4	J3-14A to RJ21X-29	J3-14C to RJ21X-4
1	5	J3-18A to RJ21X-30	J3-18C to RJ21X-5
1	6	J3-22A to RJ21X-31	J3-22C to RJ21X-6
1	7	J3-26A to RJ21X-32	J3-26C to RJ21X-7
1	8	J3-30A to RJ21X-33	J3-30C to RJ21X-8

Table 3: J3 To RJ21X Pinouts (Continued)

Card	Trunk	A Lead	B Lead
2	1	J3-2A to RJ21X-34	J3-2C to RJ21X-9
2	2	J3-6A to RJ21X-35	J3-6C to RJ21X-10
2	3	J3-10A to RJ21X-36	J3-10C to RJ21X-11
2	4	J3-14A to RJ21X-37	J3-14C to RJ21X-12
2	5	J3-18A to RJ21X-38	J3-18C to RJ21X-13
2	6	J3-22A to RJ21X-39	J3-22C to RJ21X-14
2	7	J3-26A to RJ21X-40	J3-26C to RJ21X-15
2	8	J3-30A to RJ21X-41	J3-30C to RJ21X-16
3	1	J3-2A to RJ21X-42	J3-2C to RJ21X-17
3	2	J3-6A to RJ21X-43	J3-6C to RJ21X-18
3	3	J3-10A to RJ21X-44	J3-10C to RJ21X-19
3	4	J3-14A to RJ21X-45	J3-14C to RJ21X-20
3	5	J3-18A to RJ21X-46	J3-18C to RJ21X-21
3	6	J3-22A to RJ21X-47	J3-22C to RJ21X-22
3	7	J3-26A to RJ21X-48	J3-26C to RJ21X-23
3	8	J3-30A to RJ21X-49	J3-30C to RJ21X-24

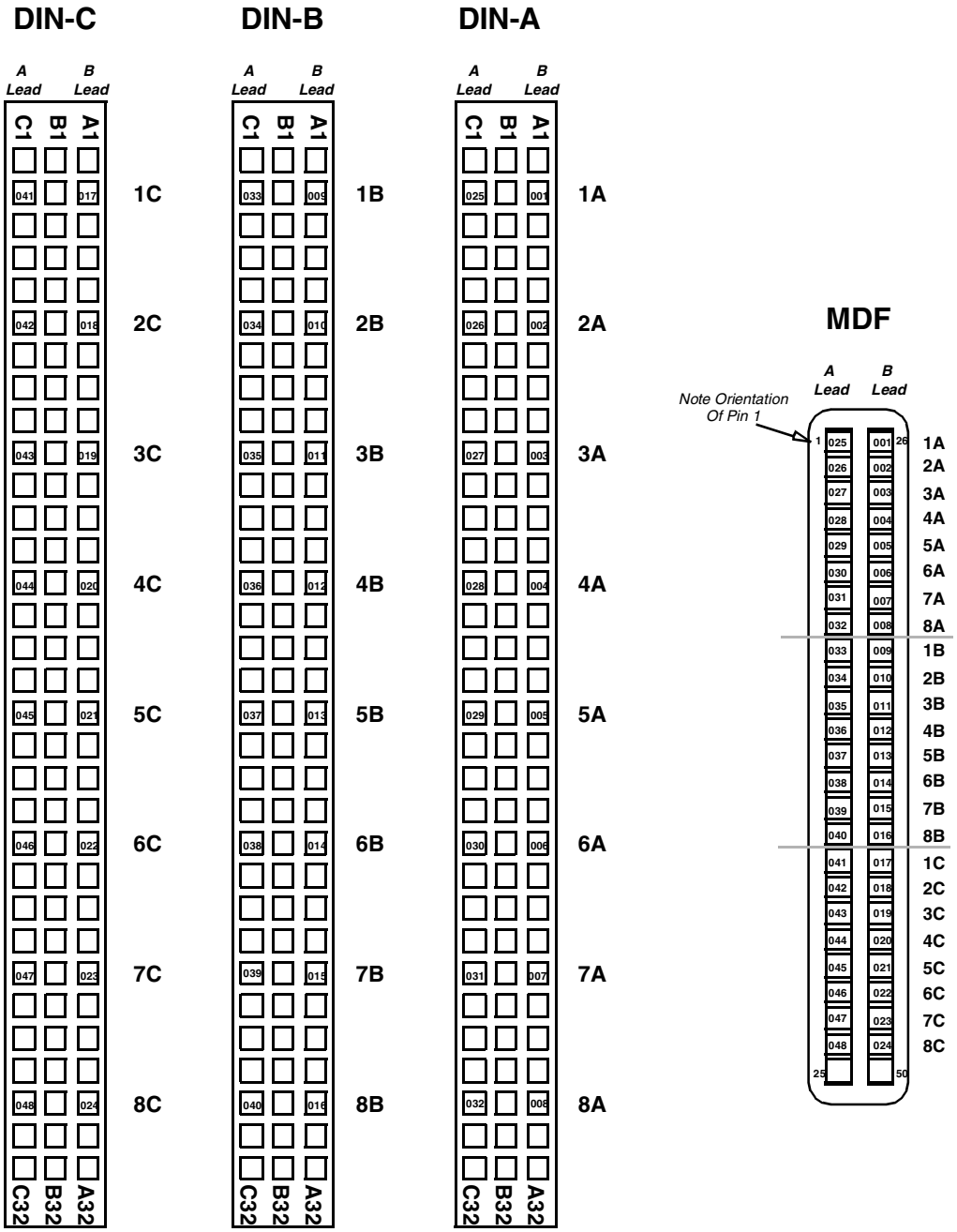


Figure 3: Pin-Out Diagram of DIN–RJ21X MDF Adapter

4.0 CONFIGURATION NOTES

The SLIC-INT is manufactured by Cisco Systems, Inc. Jumper plugs on the SLIC-INT are factory set for use in VCO/4K systems. Figure 4 indicates the location and correct installation of jumper plugs on a SLIC-INT based on the card's PCB revision level. Use this information to verify or reset jumpers on an interface card prior to installing it.

> *NOTE: The artwork revision level for the PCB itself (unpopulated) is etched on the solder side of the board near the front panel. The circuit card assembly part number, revision level and serial number appear on the component side of the PCB near the card front panel. The assembly part number includes four characters indicating the revision level. The first three characters are the actual revision level. The final letter "R" indicates that the PCB is at Release level. For example, a revision level A0L card is marked as Rev. "A0LR".*

If a card is improperly configured, it may fail to perform its interface function between external lines/trunks and the system. Therefore, great care must be taken to verify configuration settings before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base. If the port is improperly configured the system may interpret seizures as disconnects or not see them at all. For additional information on configuring a SLIC-INT in the system data base, refer to the *System Administrator's Guide.*

Class of Service (COS) also greatly affects operation of the card. A COS of "T","2" or "A2" sees inward seizures as call originations. A COS of "O" interprets inward seizures as the port being busied out by the far end. If calls are not being properly processed, check the COS.

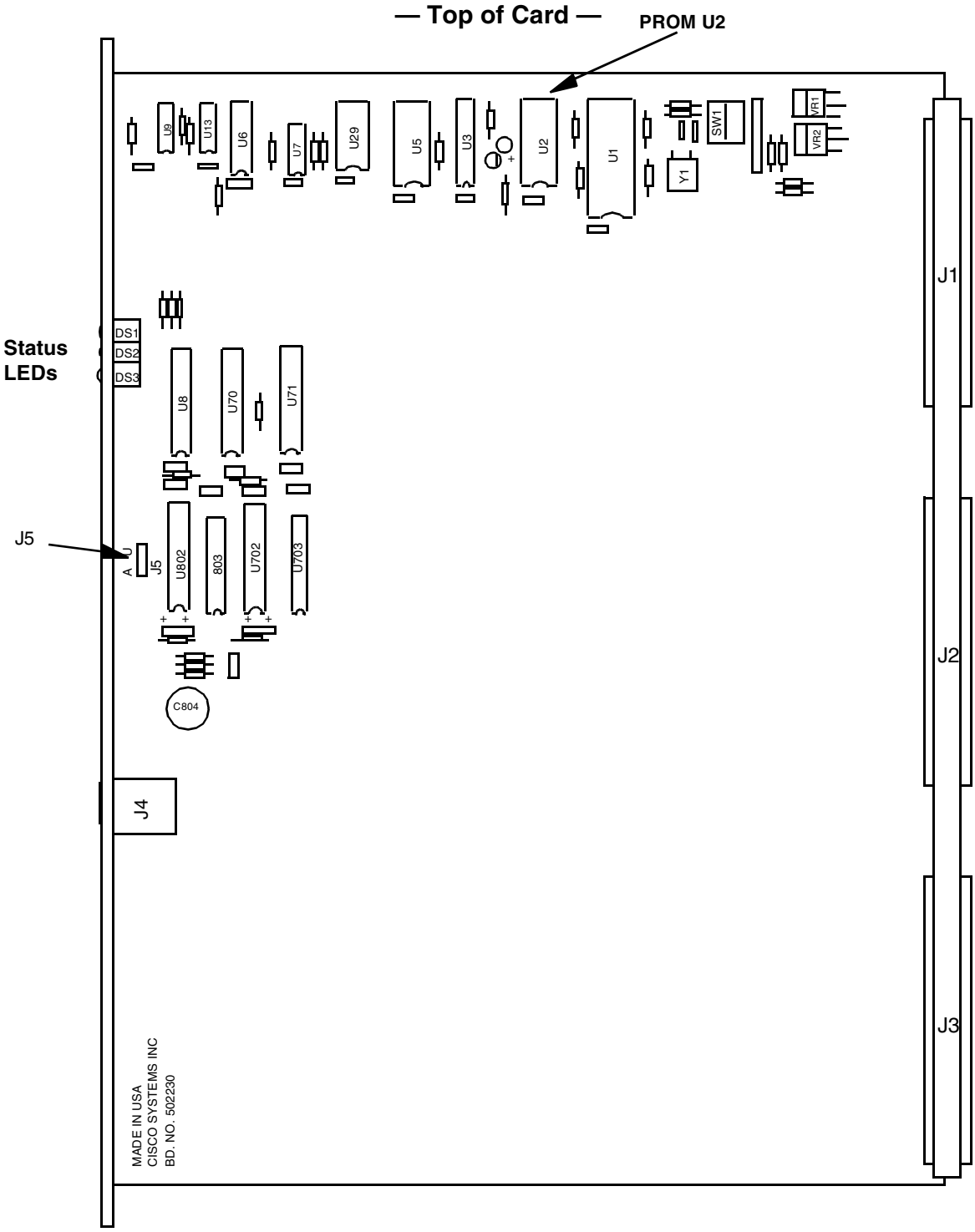


Figure 4: SLIC-INT J5 Jumper & U2 PROM Locations

4.1 SUBSCRIBER LINE INTERFACE CARD - INTERNATIONAL (SLIC-INT)

Assembly P/N 5022308124

J5 Jumper Location

NOTE 1

- Install jumper plug at J5 in the “U” position for codec µlaw operation (North American standard).
- Install jumper plug at J5 in the “A” position for codec A-law operation (European standard).
  Position “A” (A law) is the factory default setting for J5.

PROM

The 2764 PROM in location U2 contains firmware appropriate to SLIC-INT signaling interface requirements.

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the SLIC-INT, refer to the following publications:

- United Kingdom Supplement
- VCO/4K System Administrator’s Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual

T1-E Interface Card (T1-E)

1.0 GENERAL

The T1-E Interface card is a standard port interface circuit card that can reside in any slot other than those reserved for the control system cards. It operates at 1.544 Mbps (24 X 64 kHz channels). The T1-E card supports both µ-law and A-law PCM coding, and supports channel associated signalling (CAS).

Electrical interface to the T1-E complies with CCITT G.703 standards using the T1 interface adapter. The 1.544 Mpbs data rate and channel signalling comply with Bellcore recommendations for PCM switching interfaces.

System timing can be synchronized to an internal reference, a selected digital trunk, or an external reference. System software allows administrators to designate primary and secondary master timing links to which the system is synchronized. If both links fail or the external reference signal is lost, the system defaults to its internal reference clock.

2.0 SPECIFICATIONS

Microprocessor:	Intel 8031 (12 MHz)	
Memory:	8K Bytes EPROM	
	8K Bytes SRAM	
Power Requirements:		Typical
	+5 Volts:	1500 mA

Input Stream Specifications:

Format: D4 or ESF
Data Transparency: B8ZS or Bit 7 Stuffing
Frequency: 1.544 MHz ± 200 Hz
Impedance: 100 ohms ± 10 ohms
Framing Time: 10mS maximum
Yellow Alarm: Bit 2 (D4 and ESF)

Output Stream Specifications:

Format: D4 or ESF
Data Transparency: B8ZS or Bit 7 Stuffing
Drive Capability: 0 - 655 Feet
Impedance: 100 ohms +/- 10 ohm
Yellow Alarm: Bit 2 (D4 and ESF)

3.0 CIRCUIT DESCRIPTION

The T1-E card interfaces a VCO/4K system with a T1-E digital data carrier stream. The T1-E card transmits a D4 or ESF format, 1.544 MHz, 24-channel, bipolar digital data stream. The output stream is synchronized with the system clocks or loop timed. The T1-E card receives a data stream of frequency 1.544 MHz ±200 Hz and drives a reference clock onto the switch backplane which the network bus controller (NBC-3) uses as an input to its system synchronization circuitry.

The T1-E card detects loss of carrier errors, framing errors, and remote alarms on its incoming T1-E stream. It detects *slips* which occur when the rate at which data is sent on the incoming stream is different from the rate at which data is transmitted onto a PCM data bus, or when data from the PCM data bus is transmitted at a different rate, such as in loop timed configurations. The T1-E card contains elastic PCM data buffers to minimize slips caused by T1-E stream frequency jitter.

Figure 1 is a simplified block diagram of the T1-E card.

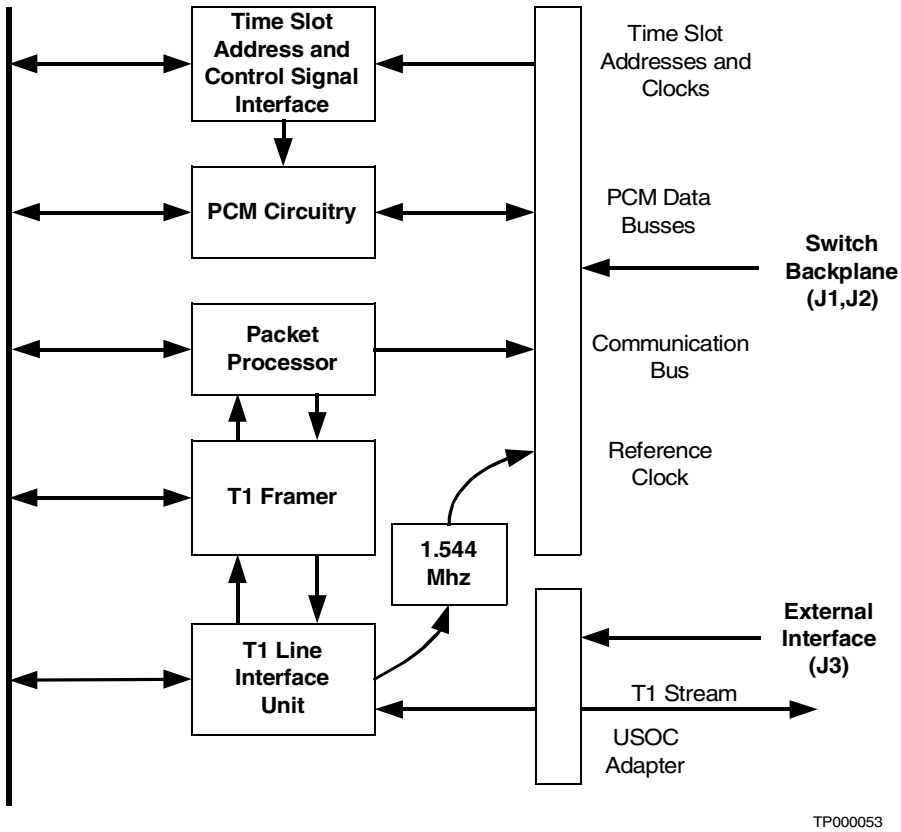


Figure 1: Block Diagram of T1-E Card

3.1 OVERVIEW OF CIRCUIT OPERATION

The T1-E card interfaces with a T1 carrier. It then frames incoming and outgoing PCM data in accordance with the D4 or ESF requirements. The framing method is firmware dependent. All framing is synchronized to internal or external clock sources as selected in the system data base.

Physical interface to the T1-E stream is accomplished via a screw-in adapter (proprietary wiring) or an ISO compliant plug-in adapter that mounts on the rear of the system. The plug-in adapter supports ISO 4903, DA-15S as well as 8-pin modular jack connections to J3 of the T1-E card.

3.2 PHYSICAL INTERFACE

Physical interface with the T1-E stream is accomplished through a line interface unit (LIU) and a T1-E framer. The link layer task controls and maintains the operation of the LIU and T1-E framer.

The LIU performs the following functions:

- Lightening and short circuit protection
- Clock recovery
- Jitter attenuation
- Bipolar to TTL conversion
- Wave shaping
- Line build-out selection
- Loopback and maintenance functions
- All ones (1s) generation

The T1-E card supports Extended Super Frame (ESF) or D4 mode.

Framing functions are implemented under microprocessor control via the framer. The framer performs the following functions

- Alarm detection
- Alarm mode selection
- Channel separation
- Data transparency

Data Transparency is provided by the B8ZS method which requires end-to-end support, or B7 stuffing.

3.3 AUXILIARY PROCESSOR

The T1 contains an auxiliary 8031 processor (auxiliary processor) to recover the channel associated signalling bits from the T1 receiver and report the signalling bit states to the packet processor. The auxiliary processor is required to load the packet processor's data buffer whenever a valid change in a channel's signalling bit states occur.

The channel associated signalling bits from the incoming T1 data stream are loaded into shift registers every master frame and are read before they are overwritten by the signalling bits from the next master frame. In addition, a moving average of the signalling bit values for each of the 24 T1 channels is performed to minimize the effects of an incorrect signalling bit transition caused by noise on the T1 data stream. The auxiliary processor performs this function, and interfaces to the packet processor to supply it information about valid signalling bit transitions.

3.4 PACKET PROCESSOR

The T1 card contains an 8031-based packet processor that interfaces to the communication bus. A packet processor is part of all cards in the system, with the exception of the NBC-3. The packet processor polls the T1 framer and LIU looking for an event (i.e., error condition or signalling bit transition). When polled by the NBC-3, the packet processor reports any status change. The packet processor supports a diagnostic serial port connected to a signal line on the backplane or accessed via a jack on the card's front panel. The packet processor also controls three status LEDs (red, yellow, and green) which are visible through the card's front panel.

The packet processor consists of the 8031 microcomputer and associated RAM, EPROM, and address decode circuitry, the communication bus interface, an asynchronous serial port, and the LED register. The 8031 provides the intelligence for the packet processor, and therefore for the T1 Interface Card.

The communication bus is the path by which the packet processor receives commands from, and sends status to, the NBC-3.

3.5 T1-E FRAMER

The DS2180A framer interfaces to a DS1, 1.544Mbps digital trunk through the LIU. It supports the D4 and ESF extended superframe standards and provides clear channel capability through appropriate zero suppression and signalling modes. System ones density is maintained through B8ZS (bipolar eight zero substitution) coding or B7 stuffing. B8ZS coding replaces eight consecutive outgoing zeros with a B8ZS code word.

The transmit framer/formatter circuits generate appropriate framing bits, supervise zero suppression, generate alarms and provide output clocks for data conditioning and decoding. The receiver/synchronizer circuits establish frame and multiframe boundaries, extract signalling data and report alarms and signalling formats.

3.6 LINE INTERFACE UNIT

The LIU employed on the T1-E card (CS61575 or LXT305A) is a fully integrated transceiver designed for North American, T1 (1.544Mbps) operation. It performs line driver, data recovery and clock recovery functions. The LIU supports full-duplex transmission of digital data over twisted-pair installations. Equalization is switch selected for line length of 0 to 655 feet (0 to 200 meters).

3.7 T1-E CARD LED STATES

Table 1 lists front panel LED states for T1-E cards and their meanings. The following general signalling conditions apply to each LED.

- *Red (top) LED* – illuminates continuously to signal a problem with an inward T1-E stream (carrier loss or Out-of-Frame (OOF) alarm).
- *Yellow (center) LED* – illuminates to signal that a Yellow Alarm is detected on the incoming T1-E stream (remote alarm), or that the card is not polled for two seconds by the NBC-3.
- *Green (bottom) LED* – not used for alarming. Illuminates continuously until the base address of the card is assigned by the system.

Table 1: T1-E Card LED State

T1-ESF LEDs			System Alarm	Condition	Card State	Outward Action
Red	Yel	Grn				
OFF	OFF	OFF	None	Normal	Active	Call processing is occurring
OFF	ON	OFF	Minor (FRM113)	Remote Alarm	Maintenance	None
			Minor	COMM Bus Polling Failure	Normal	None
ON	OFF	OFF	Major (FRM112)	Loss of Carrier	Maintenance	Sending Yellow alarm
			Minor (FRM120)	OOF Error	Maintenance	Sending Yellow alarm
ON	ON	OFF	Major	Following Card Reset	Maintenance	None
OFF	OFF	ON	Minor (FRM096)	Out-Of-Service (OOS)	OOS	None

- If multiple conditions force a card into Maintenance state, the card is not activated until all error conditions are cleared.
- If the Manual Intervention for SLIP/OOFS flag is set to N, slips may be occurring even though the card is Active and no LEDS are illuminated. The maintenance threshold for OOFs is ignored and the T1-E card cycles in and out of Maintenance as the OOF condition is detected and cleared.
- Slip and OOF counters are automatically zeroed at midnight.

3.8 PCM BUS INTERFACES - J1 PIN ASSIGNMENTS

Table 2 lists the pin assignments for J1 on the T1-E card.

Table 2: T1-E j1 Pin Assignments

Pin	Row A	Row B	Row C
1	DGND	Unused	DGND
2	DGND	Unused	DGND
3	DGND	Unused	DGND
4	DGND	Unused	DGND
5	Battery Return	Unused	Battery Return
6	Battery Return	Unused	Battery Return
7	Battery Return	Unused	Battery Return
8	Unused	Unused	Unused
9	Ring Voltage	Unused	Unused
10	Unused	Unused	Unused
11	Digital +5V	Unused	Digital +5V
12	Digital +5V	Unused	Digital +5V
13	Digital +5V	Unused	Digital +5V
14	-24V	Unused	+24V
15	Battery (-48V)	Unused	Battery (-48V)
16	Battery (-48V)	Unused	Battery (-48V)
17	Battery (-48V)	Unused	Battery (-48V)
18	Analog -15V	Unused	Analog -15V
19	Analog -15V	Unused	Analog -15V
20	Analog +15V	Unused	Analog +15V
21	Analog +15V	Unused	Analog +15V
22	Card Addr. Bit 1	Unused	Card Addr. Bit 0

Table 2: T1-E j1 Pin Assignments (Continued)

Pin	Row A	Row B	Row C
23	Card Addr. Bit 3	Unused	Card Addr. Bit 2
24	Card Addr. Bit 5	Unused	Card Addr. Bit 4
25	Card Addr. Bit 7	Unused	Card Addr. Bit 6
26	SRV	Unused	AB1
27	DID	Unused	AB2
28	RST	Unused	Serial Bus
29	Unused	Unused	Unused
30	AGND	Unused	AGND
31	AGND	Unused	AGND
32	DGND	Unused	DGND

3.9 EXTERNAL INTERFACES

The J3 connector completes the connections to the incoming and outgoing T1-E digital data streams. A DIN to MDF adapter attaches to the J3 connector and allows external connection to the T1-E card via a 15-position, Sub-D type connector or an RJ45. A male Sub-D type connector is provided on the MDF Adapter.

J3 connector pinouts are listed in Table 3.

Table 3: T1-E Card J3 Pinouts

Pin	Row A	Row B	Row C
1	Unused	Unused	Digital Ground
2	Unused	Unused	Reserved
3	Unused	Unused	Rev Line Tip[a]
4	Unused	Unused	Rev Line Ring[a]
5	Unused	Unused	Xmt Line Tip[b]
6	Unused	Unused	Xmt Line Ring[b]
7	Unused	Unused	Unused
8	Unused	Unused	Unused
9	Unused	Unused	Unused
10	Unused	Unused	Unused
11	Unused	Unused	Unused

Table 3: T1-E Card J3 Pinouts (Continued)

Pin	Row A	Row B	Row C
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Unused	Unused	Unused
15	Unused	Unused	Unused
16	Unused	Unused	Unused
17	Unused	Unused	Unused
18	Unused	Unused	Unused
19	Unused	Unused	Unused
20	Unused	Unused	Unused
21	Unused	Unused	Unused
22	Unused	Unused	Unused
23	Unused	Unused	Unused
24	Unused	Unused	Unused
25	Unused	Unused	Unused
26	Unused	Unused	Unused
27	Unused	Unused	Unused
28	Unused	Unused	Unused
29	Unused	Unused	GND
30	Unused	Unused	SCC3 UART Xmt
31	Unused	Unused	SCC3 UART Rev
32	Unused	Unused	Unused

a. Signal to T1-E Card.

b. Signal from T1-E card.

NOTE: J2 Pin Assignments are proprietary and are therefore not documented for customer use.

The J3 to D connector pinouts are shown in Figure 2 and Table 4.

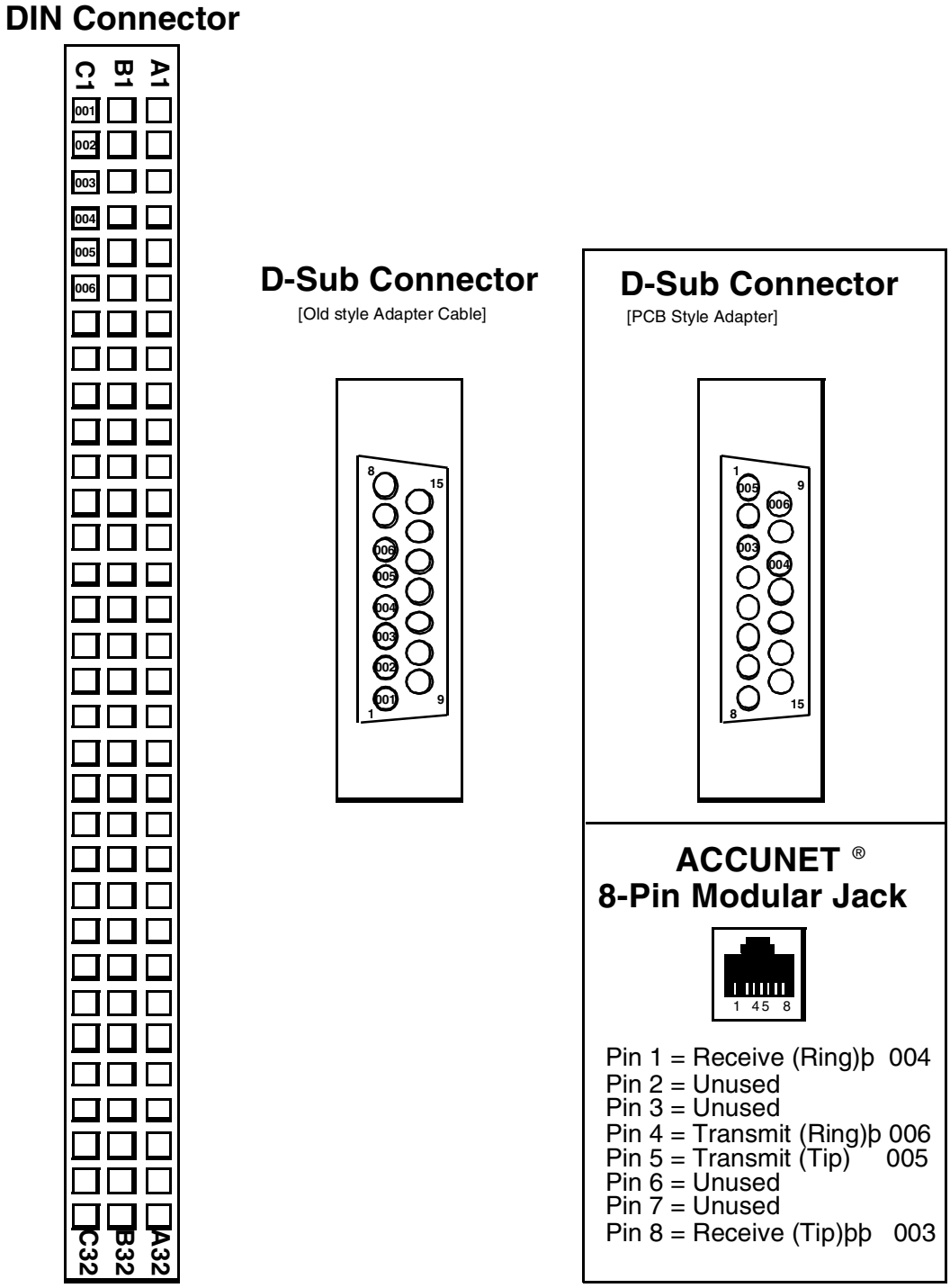


Figure 3: Pin Out Diagram of T1/T1-E Adapters

NOTE: 20115850100 is the part number for the entire PCB Style Adapter assembly. A different number (50191050100) may be etched on the Adapter's PCB. The etched number is the part number for the PCB only. Use the assembly number when ordering a new Adapter.

Table 4: T1-E Card J3 to D-Connector/Modular Jack Pinouts: Plug-In T1/T1-E Adaptor

J3 Pin	D-Connector Pin [a]	Modular Jack	Signal Name
1C	Not Connected	Not Connected	Digital Ground
2C	Not Connected	Not Connected	Reserved
3C	1	8	Receive Line Tip (to card)
4C	9	1	Receive Line Ring (to card)
5C	3	5	Transmit Line Tip (from card)
6C	11	4	Transmit Line Ring (from card)

a. DA-15S, ISO 4903.

3.10 LINE EQUALIZATION

The T1-E card provides a selectable pre-emphasis equalizer to balance its transmit stream according to the length of the cable being driven. The equalization factors apply to ABAM cable comprised of two individually shielded twisted pairs, 22AWG conductors.

3.11 DIP SWITCH SETTINGS

Jumper JP20 on each T1-E card indicates the PCM companding law switched over the system backplane. If JP20 indicates a companding law different from that indicated by the DIP switch, companding law conversion is performed. Law conversion occurs in both directions and on all timeslots. CAS signalling bit integrity is preserved. Table 5 lists the T1-E dip switch settings.

NOTE: Be sure that JP20 and the DIP switch are set correctly for your application before powering up the system. It is important that JP20 correspond to the companding law used by your DTG card.

Table 5: T1-E DIP Switch Settings

POS	ON/CLOSED	OFF/OPEN	FACTORY DEFAULT
1	B8ZS	B7	OFF
2	CAS Disabled	CAS Enabled [a]	OFF
3	D4	ESF	ON
4	0db PCM Attenuation Factor	-9db PCM Attenuation Factor	ON
5	μ-Law Trunk	A-Law Trunk	ON
6	Drive-0 Disabled	Drive-0 Enabled	OFF
7	Drive-1 Disabled	Drive-1 Enabled	OFF
8	Drive-2 Disabled	Drive-2 Enabled	ON

a. For D4 framing only. CAS signalling is not supported in ESF framing mode.

NOTE: PCM gain attenuation is applied to all timeslots on the incoming PCM stream. Cisco Systems can implement variations to the gain map to achieve other desired gain levels or level limiting. Please refer to Appendix A of this document for other firmware-specific options.

The five supported build-out options are shown in Table 6. Other options are reserved.

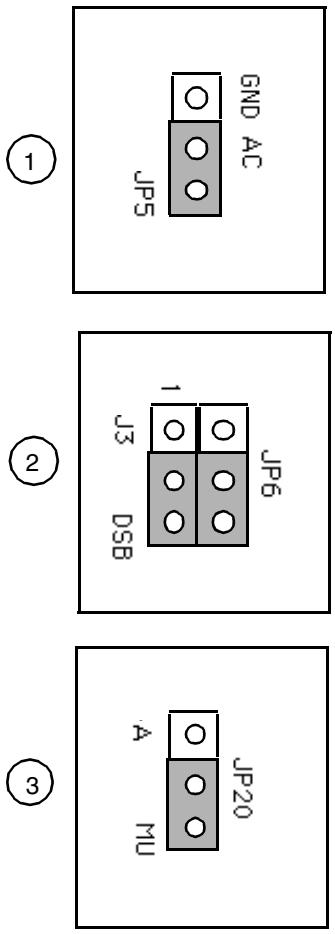
Table 6: Build-Out Options

POS-6	POS-7	POS-8	Build-Out Length
Open	Open	Closed	0-133 Ft.
Closed	Closed	Open	133-266 Ft.
Open	Closed	Open	266-399 Ft.
Closed	Open	Open	399-533 Ft.
Open	Open	Open	533-655 Ft.

4.0 CONFIGURATION NOTES

The T1-E card is manufactured by Cisco Systems, Inc. Figure 2 indicates the location of factory set jumpers. Refer to these jumper settings and Figure 3 to verify configuration jumper settings prior to installing the T1-E card.

NOTE: Artwork revision levels for individual printed circuit boards (PCBs) are etched on the solder side of the PCB near the front panel of each card.



PROM Listing

PROM 1
T1/ESF FIRMWARE

PROM 2
AUXILIARY CAS
PROCESSOR FIRMWARE

PROM 3
32-CH PATH
SETUP

PROM 4
TX PCM
GAIN/CONVERSION

PROM 5
RX PCM
GAIN/CONVERSION

Figure 2: T1-E Card Jumper Locations

If a card is improperly configured, it may fail to perform its interface function between external spans and the system. Therefore, great care must be taken to verify configuration settings, hardware jumpers and data base entries, before installing a replacement interface card in the system.

Port Configuration refers to the process of specifying appropriate data for each port in the system data base, including line equalization. If the port is improperly configured, the system may improperly interpret the incoming T1-E stream.

Figure 3 shows the jumper/PROM locations on the T1-E card.

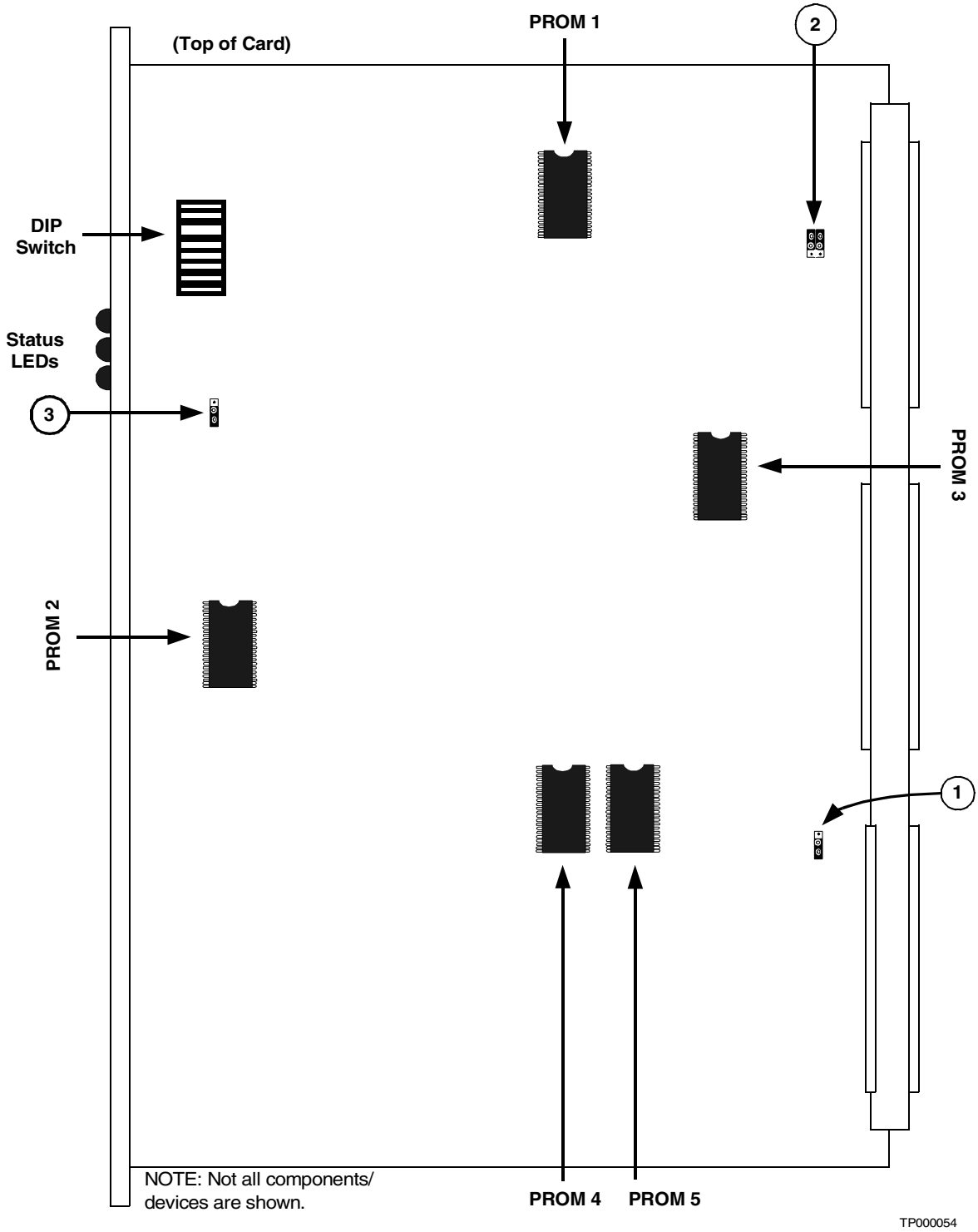


Figure 3: T1-E Card Jumper/PROM Locations

5.0 RELATED DOCUMENTS

For additional information regarding the operation, application, installation and maintenance of the T1-E card, refer to the following documents:

- VCO/4K System Administrator's Guide
- VCO/4K Hardware Planning Guide
- VCO/4K Installation Manual
- VCO/4K System Maintenance Manual

6.0 DIP SWITCH SETTINGS FOR FIRMWARE, VERSION 9 (JAPAN)

Table 7 shows the dip switch settings for Firmware, Version 9.

Table 7: DIP Switch Settings for Firmware, Version 9

POS	ON/CLOSED	OFF/OPEN	FACTORY DEFAULT
1	B8ZS	B7	OFF
2	CAS Disabled	CAS Enabled	OFF
3	GAIN-0 Disabled	GAIN-0 Enabled	ON
4	GAIN-1 Disabled	GAIN-1 Enabled	ON
5	μ-Law Trunk	A-Law Trunk	ON
6	Drive-0 Disabled	Drive-0 Enabled	OFF
7	Drive-1 Disabled	Drive-1 Enabled	OFF
8	Drive-2 Disabled	Drive-2 Enabled	ON

Four levels of gain control are achieved, which correspond toTable 8. PCM attenuation is applied to all 24 timeslots on the incoming PCM stream.

NOTE: Only D4 framing is supported.

Table 8: Gain Control

POS-4	POS-3	GAIN/ATT (db)
Closed	Closed	0
Closed	Open	-6
Open	Closed	-9
Open	Open	-12